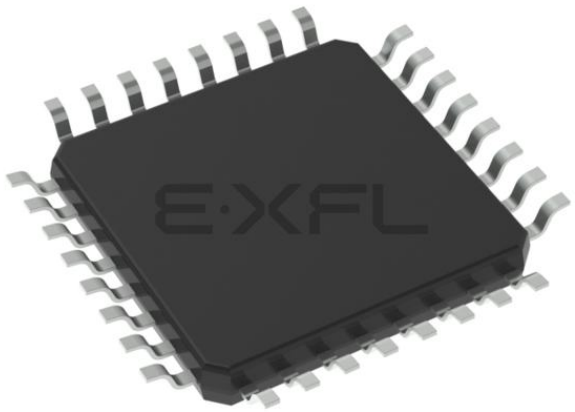

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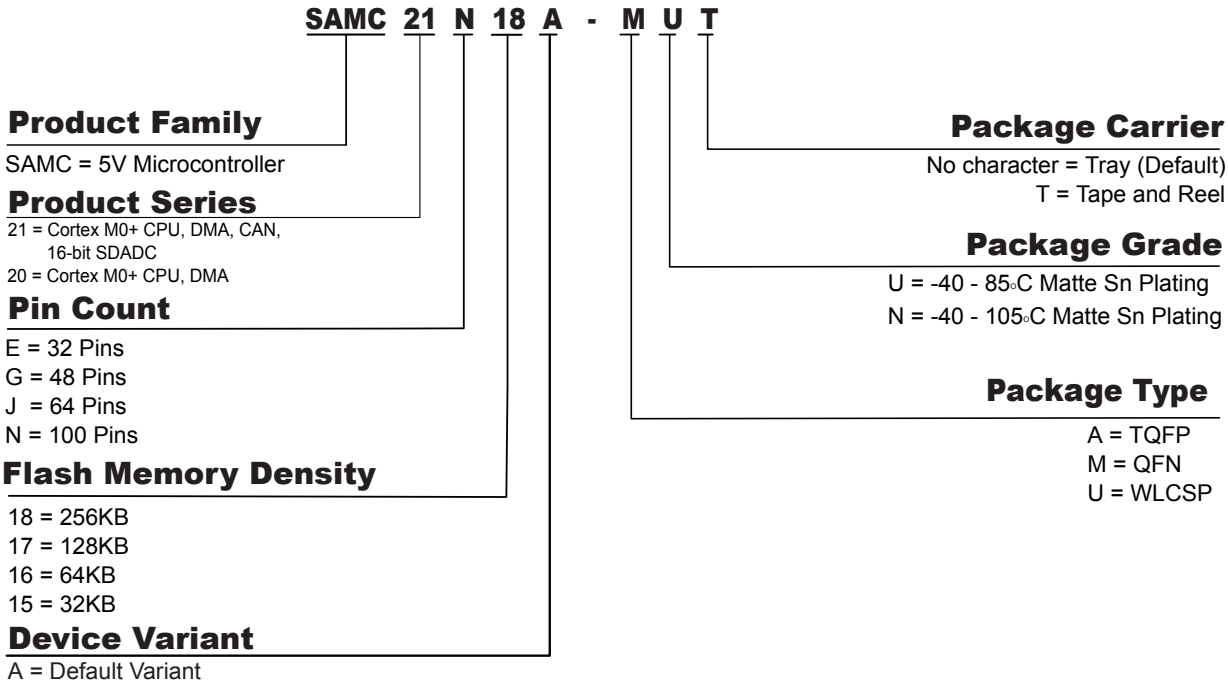
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, WDT
Number of I/O	26
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-TQFP
Supplier Device Package	32-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamc20e17a-ant

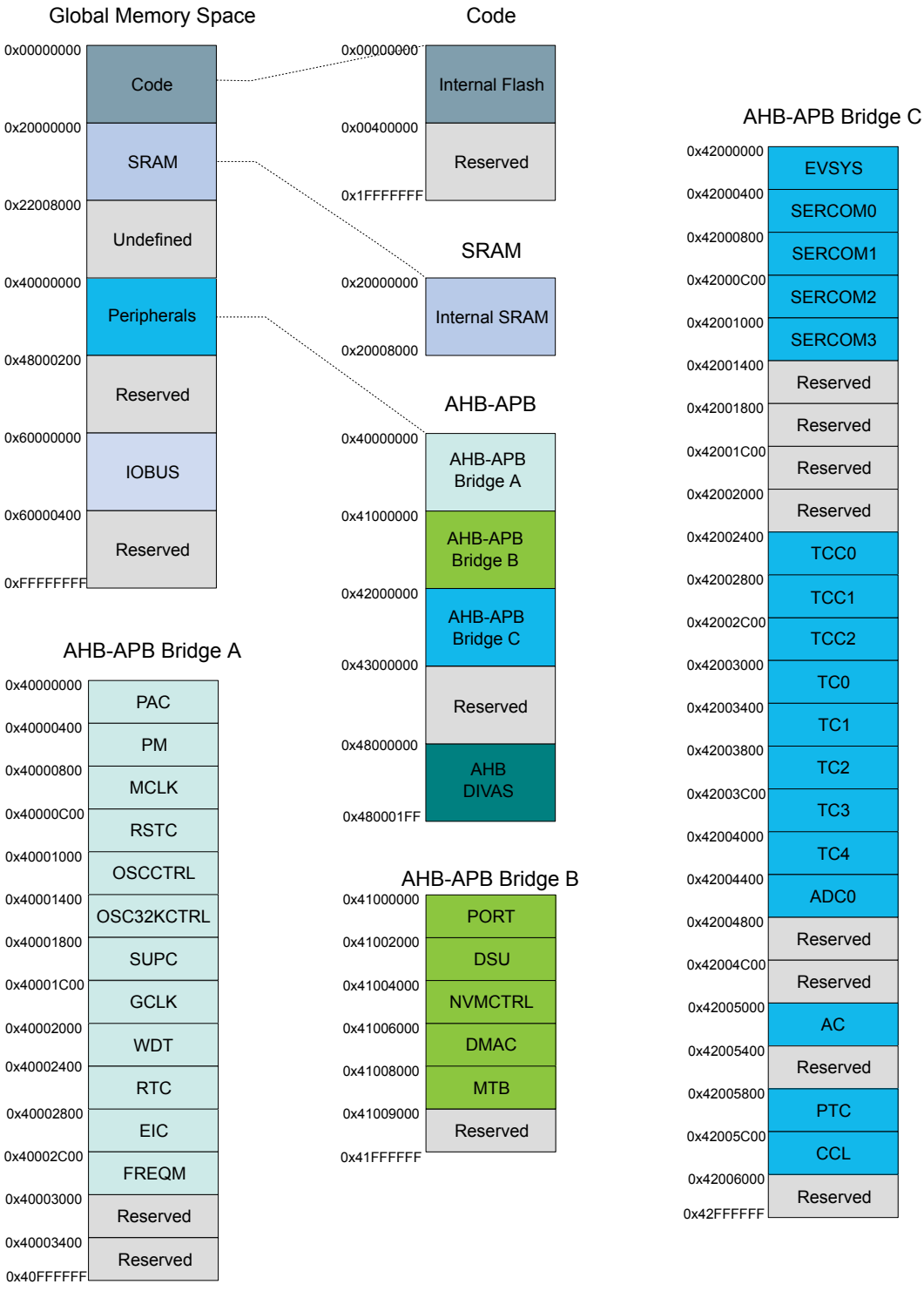
2. Ordering Information



Note: Not all combinations are valid. The available ordering numbers are listed in the Configuration Summary.

Package	Cluster	GPIO	Supplies Pin connected to the cluster	
	3	PA25 PA24 PA23 PA22 PA21 PA20 PB21 PB20 PB19 PB18 PB17 PB16	VDDIO(63+77)	GND(62+76)
	4	PC21 PC20 PC19 PC18 PC17 PC16 PA19 PA18 PA17 PA16	VDDIO(51+63)	GND(50+62)
	5	PA15 PA14 PA13 PA12 PC14 PC13 PC12 PC11 PC10 PC09 PC08	VDDIO(36+51)	GND(37+50)
	6	PB15 PB13 PB12 PB11 PB10 PA11 PA10 PA09 PA08	VDDIO(25+36)	GND(24+37)
	7	PC07 PC06 PC05 PA07 PA06 PA05 PA04 PB09 PB05 PB04 PA03 PA02 PC02 PC01 PC00 PA01 PA00 PB03 PB02 PB01 PB00	VDDANA (12)	GNDANA (11)
	8	PC15	VDDIO(25)	GND(37+50)
	9	PB14	VDDIO(25)	GND(24+37)
	10	PB08 PB07 PB06 PC03	VDDIO(25)	GNDANA (11)
64 pins	1	PB31 PB30 PA31 PA30 PA28 PA27	VDDIN (56)	GND (54)
	2	PB23 PB22	VDDIO (48)	GND (54+47)
	3	PA25 PA24 PA23 PA22 PA21 PA20 PB17 PB16 PA19 PA18 PA17 PA16	VDDIO (48+34)	GND (47+33)
	4	PA15 PA14 PA13 PA12 PB15 PB14 PB13 PB12 PB11 PB10	VDDIO (34+21)	GND (33+22)
	5	PA11 PA10 PA08 PA09	VDDIO (21)	GND (22)
	6	PA07 PA06 PA05 PA04 PB09 PB08 PB07 PB06 PB05 PB04 PA03 PA02 PA01 PA00 PB03 PB02 PB01 PB00	VDDANA (8)	GNDANA (7)
48 pins	1	PA31 PA30 PA28 PA27	VDDIN (44)	GND (42)
	2	PB23 PB22	VDDIO (36)	GND (42+35)
	3	PA25 PA24 PA23 PA22 PA21 PA20 PA19 PA18 PA17 PA16 PA15 PA14 PA13 PA12 PB11 PB10	VDDIO (36+17)	GND (35+18)
	4	PA11 PA10 PA08 PA09	VDDIO (17)	GND (18)
	5	PA07 PA06 PA05 PA04 PB09 PB08 PA03 PA02 PA01 PA00 PB03 PB02	VDDANA (6)	GNDANA (5)
32 pins	1	PA31 PA30 PA28 PA27	VDDIN (30)	GND (28)
	2	PA25 PA24 PA23 PA22 PA19 PA18 PA17 PA16 PA15 PA14 PA11 PA10 PA08 PA09	VDDIO (9)	GND (28+10)
	3	PA07 PA06 PA05 PA04 PA03 PA02 PA01 PA00	VDDANA (9)	GND (28+10)

Figure 8-4. SAM C20 E/G/J Product Mapping



Bit	31	30	29	28	27	26	25	24
	END[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	END[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	END[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	END[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – END[31:0]: End Marker
Indicates the end of the CoreSight ROM table entries.

13.13.13 CoreSight ROM Table Memory Type

Name: MEMTYPE
Offset: 0x1FCC
Reset: 0x0000000x
Property: -

Name: DIVIDEND
Offset: 0x08
Reset: 0x0000
Property: -

Bit	31	30	29	28	27	26	25	24
	DIVIDEND[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DIVIDEND[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DIVIDEND[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DIVIDEND[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DIVIDEND[31:0]: Dividend Value
Holds the 32-bit dividend for the divide operation. If the Signed bit in Control A register (CTRLA.SIGNED) is zero, DIVIDEND is unsigned. If CTRLA.SIGNED = 1, DIVIDEND is signed two's complement. Refer to Performing Division, Operand Size and Signed Division.

14.8.4 Divisor

Name: DIVISOR
Offset: 0x0C
Reset: 0x0000
Property: -

Bit	7	6	5	4	3	2	1	0
								CKRDY
Access								R/W
Reset								0

Bit 0 – CKRDY: Clock Ready Interrupt Enable
Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the Clock Ready Interrupt Enable bit and enable the Clock Ready interrupt.

Value	Description
0	The Clock Ready interrupt is disabled.
1	The Clock Ready interrupt is enabled.

17.8.4 Interrupt Flag Status and Clear

Name: INTFLAG
Offset: 0x03
Reset: 0x01
Property: –

Bit	7	6	5	4	3	2	1	0
								CKRDY
Access								R/W
Reset								1

Bit 0 – CKRDY: Clock Ready
This flag is cleared by writing a '1' to the flag.

This flag is set when the synchronous CPU, APBx, and AHBx clocks have frequencies as indicated in the CLKCFG registers and will generate an interrupt if INTENCLR/SET.CKRDY is '1'.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the Clock Ready interrupt flag.

17.8.5 CPU Clock Division

Name: CPUDIV
Offset: 0x05 [ID-00001086]
Reset: 0x01
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
	CPUDIV[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	1

Bits 7:0 – CPUDIV[7:0]: CPU Clock Division Factor
These bits define the division ratio of the main clock prescaler related to the CPU clock domain.

24.5.9 Analog Connections

A 32.768kHz crystal can be connected to the XIN32 and XOUT32 pins, along with any required load capacitors. See Electrical Characteristics for details on recommended crystal characteristics and load capacitors.

24.6 Functional Description

24.6.1 Principle of Operation

The RTC keeps track of time in the system and enables periodic events, as well as interrupts and events at a specified time. The RTC consists of a 10-bit prescaler that feeds a 32-bit counter. The actual format of the 32-bit counter depends on the RTC operating mode.

The RTC can function in one of these modes:

- Mode 0 - COUNT32: RTC serves as 32-bit counter
- Mode 1 - COUNT16: RTC serves as 16-bit counter
- Mode 2 - CLOCK: RTC serves as clock/calendar with alarm functionality

24.6.2 Basic Operation

24.6.2.1 Initialization

The following bits are enable-protected, meaning that they can only be written when the RTC is disabled (CTRLA.ENABLE=0):

- Operating Mode bits in the Control A register (CTRLA.MODE)
- Prescaler bits in the Control A register (CTRLA.PRESCALER)
- Clear on Match bit in the Control A register (CTRLA.MATCHCLR)
- Clock Representation bit in the Control A register (CTRLA.CLKREP)

The following registers are enable-protected:

- Event Control register (EVCTRL)

Enable-protected bits and registers can be changed only when the RTC is disabled (CTRLA.ENABLE=0). If the RTC is enabled (CTRLA.ENABLE=1), these operations are necessary: first write CTRLA.ENABLE=0 and check whether the write synchronization has finished, then change the desired bit field value. Enable-protected bits in CTRLA register can be written at the same time as CTRLA.ENABLE is written to '1', but not at the same time as CTRLA.ENABLE is written to '0'.

Enable-protection is denoted by the "Enable-Protected" property in the register description.

The RTC prescaler divides the source clock for the RTC counter.

Note: In Clock/Calendar mode, the prescaler must be configured to provide a 1Hz clock to the counter for correct operation.

The frequency of the RTC clock (CLK_RTC_CNT) is given by the following formula:

$$f_{\mathrm{CLK\_RTC\_CNT}} = \frac{f_{\mathrm{CLK\_RTC\_OSC}}}{2^{\mathrm{PRESCALER}}}$$

The frequency of the oscillator clock, CLK_RTC_OSC, is given by $f_{CLK\_RTC\_OSC}$, and $f_{CLK\_RTC\_CNT}$ is the frequency of the internal prescaled RTC clock, CLK_RTC_CNT.

26. EIC – External Interrupt Controller

26.1 Overview

The External Interrupt Controller (EIC) allows external pins to be configured as interrupt lines. Each interrupt line can be individually masked and can generate an interrupt on rising, falling, or both edges, or on high or low levels. Each external pin has a configurable filter to remove spikes. Each external pin can also be configured to be asynchronous in order to wake up the device from sleep modes where all clocks have been disabled. External pins can also generate an event.

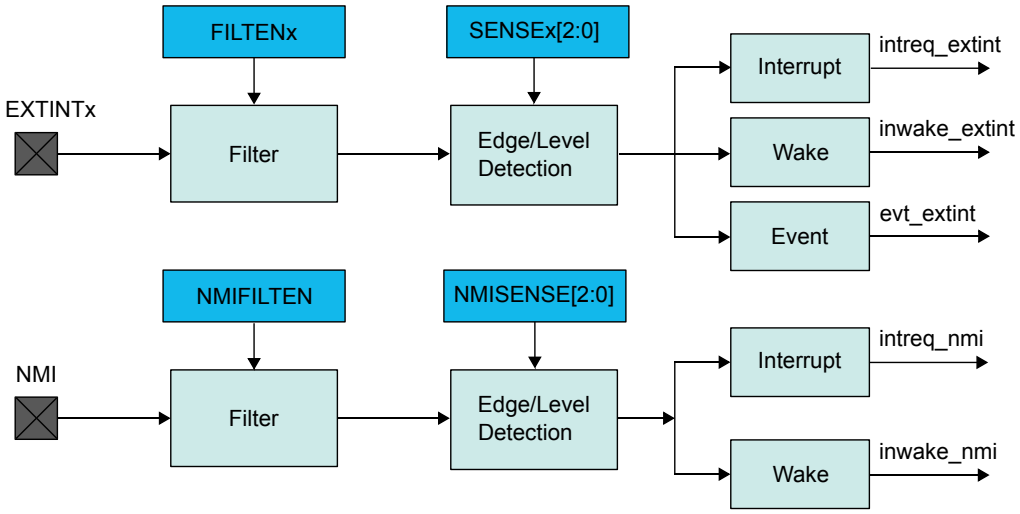
A separate non-maskable interrupt (NMI) is also supported. It has properties similar to the other external interrupts, but is connected to the NMI request of the CPU, enabling it to interrupt any other interrupt mode.

26.2 Features

- Up to 32 external pins (EXTINTx), plus one non-maskable pin (NMI)
- Dedicated, individually maskable interrupt for each pin
- Interrupt on rising, falling, or both edges
- Synchronous or asynchronous edge detection mode
- Interrupt pin debouncing
- Interrupt on high or low levels
- Asynchronous interrupts for sleep modes without clock
- Filtering of external pins
- Event generation from EXTINTx

26.3 Block Diagram

Figure 26-1. EIC Block Diagram



CMD[1:0]	DIR	Action
0x3	Used in response to an address interrupt (AMATCH)	
	0 (Master write)	Execute acknowledge action succeeded by reception of next byte
	1 (Master read)	Execute acknowledge action succeeded by slave data interrupt
	Used in response to a data interrupt (DRDY)	
	0 (Master write)	Execute acknowledge action succeeded by reception of next byte
	1 (Master read)	Execute a byte read operation followed by ACK/NACK reception

Bits 15:14 – AMODE[1:0]: Address Mode
These bits set the addressing mode.

These bits are not write-synchronized.

Value	Name	Description
0x0	MASK	The slave responds to the address written in ADDR.ADDR masked by the value in ADDR.ADDRMASK. See *SERCOM – Serial Communication Interface* for additional information.
0x1	2_ADDRS	The slave responds to the two unique addresses in ADDR.ADDR and ADDR.ADDRMASK.
0x2	RANGE	The slave responds to the range of addresses between and including ADDR.ADDR and ADDR.ADDRMASK. ADDR.ADDR is the upper limit.
0x3	-	Reserved.

Bit 10 – AACKEN: Automatic Acknowledge Enable
This bit enables the address to be automatically acknowledged if there is an address match.

This bit is not write-synchronized.

Value	Description
0	Automatic acknowledge is disabled.
1	Automatic acknowledge is enabled.

Bit 9 – GCMD: PMBus Group Command
This bit enables PMBus group command support. When enabled, the Stop Recived interrupt flag (INTFLAG.PREC) will be set when a STOP condition is detected if the slave has been addressed since the last STOP condition on the bus.

This bit is not write-synchronized.

Value	Description
0	Group command is disabled.
1	Group command is enabled.

Bit 8 – SMEN: Smart Mode Enable
When smart mode is enabled, data is acknowledged automatically when DATA.DATA is read.

This bit is not write-synchronized.

Value	Description
0	Smart mode is disabled.
1	Smart mode is enabled.

Value	Description
0	The Stop Received interrupt is disabled.
1	The Stop Received interrupt is enabled.

33.8.5 Interrupt Flag Status and Clear

Name: INTFLAG
Offset: 0x18 [ID-00001bb3]
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
	ERROR					DRDY	AMATCH	PREC
Access	R/W					R/W	R/W	R/W
Reset	0					0	0	0

Bit 7 – ERROR: Error
This bit is set when any error is detected. Errors that will set this flag have corresponding status flags in the STATUS register. The corresponding bits in STATUS are SEXTTOUT, LOWTOUT, COLL, and BUSERR.

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the flag.

Bit 2 – DRDY: Data Ready
This flag is set when a I^2C slave byte transmission is successfully completed.

The flag is cleared by hardware when either:

- Writing to the DATA register.
- Reading the DATA register with smart mode enabled.
- Writing a valid command to the CMD register.

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the Data Ready interrupt flag.

Bit 1 – AMATCH: Address Match
This flag is set when the I^2C slave address match logic detects that a valid address has been received.

The flag is cleared by hardware when CTRL.CMD is written.

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the Address Match interrupt flag. When cleared, an ACK/NACK will be sent according to CTRLB.ACKACT.

Bit 0 – PREC: Stop Received
This flag is set when a stop condition is detected for a transaction being processed. A stop condition detected between a bus master and another slave will not set this flag, unless the PMBus Group Command is enabled in the Control B register (CTRLB.GCMD=1).

This flag is cleared by hardware after a command is issued on the next address match.

Bit	7	6	5	4	3	2	1	0
	ERROR						SB	MB
Access	R/W						R/W	R/W
Reset	0						0	0

Bit 7 – ERROR: Error Interrupt Enable
Writing '0' to this bit has no effect.

Writing '1' to this bit will set the Error Interrupt Enable bit, which enables the Error interrupt.

Value	Description
0	Error interrupt is disabled.
1	Error interrupt is enabled.

Bit 1 – SB: Slave on Bus Interrupt Enable
Writing '0' to this bit has no effect.

Writing '1' to this bit will set the Slave on Bus Interrupt Enable bit, which enables the Slave on Bus interrupt.

Value	Description
0	The Slave on Bus interrupt is disabled.
1	The Slave on Bus interrupt is enabled.

Bit 0 – MB: Master on Bus Interrupt Enable
Writing '0' to this bit has no effect.

Writing '1' to this bit will set the Master on Bus Interrupt Enable bit, which enables the Master on Bus interrupt.

Value	Description
0	The Master on Bus interrupt is disabled.
1	The Master on Bus interrupt is enabled.

33.10.6 Interrupt Flag Status and Clear

Name: INTFLAG
Offset: 0x18 [ID-00001bb3]
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
	ERROR						SB	MB
Access	R/W						R/W	R/W
Reset	0						0	0

Bit 7 – ERROR: Error
This flag is cleared by writing '1' to it.

This bit is set when any error is detected. Errors that will set this flag have corresponding status bits in the STATUS register. These status bits are LENERR, SEXTTOUT, MEXTTOUT, LOWTOUT, ARBLOST, and BUSERR.

34.7 Register Summary

Offset	Name	Bit Pos.								
0x00	CREL	7:0								
0x01		15:8								
0x02		23:16	SUBSTEP[3:0]							
0x03		31:24	REL[3:0]				STEP[3:0]			
0x04	ENDN	7:0	ETV[7:0]							
0x05		15:8	ETV[15:8]							
0x06		23:16	ETV[23:16]							
0x07		31:24	ETV[31:24]							
0x08	MRCFG	7:0							DQOS[1:0]	
0x09		15:8								
0x0A		23:16								
0x0B		31:24								
0x0C	DBTP	7:0	DTSEG2[3:0]				DSJW[3:0]			
0x0D		15:8				DTSEG1[4:0]				
0x0E		23:16	TDC			DBRP[4:0]				
0x0F		31:24								
0x10	TEST	7:0	RX	TX[1:0]		LBCK				
0x11		15:8								
0x12		23:16								
0x13		31:24								
0x14	RWD	7:0	WDC[7:0]							
0x15		15:8	WDV[7:0]							
0x16		23:16								
0x17		31:24								
0x18	CCCR	7:0	TEST	DAR	MON	CSR	CSA	ASM	CCE	INIT
0x19		15:8		TXP	EFBI	PXHD			BRSE	FDOE
0x1A		23:16								
0x1B		31:24								
0x1C	NBTP	7:0		NTSEG2[6:0]						
0x1D		15:8	NTSEG1[7:0]							
0x1E		23:16	NBRP[7:0]							
0x1F		31:24	NSJW[6:0]							NBRP[8:8]
0x20	TSCC	7:0							TSS[1:0]	
0x21		15:8								
0x22		23:16					TCP[3:0]			
0x23		31:24								
0x24	TSCV	7:0	TSC[7:0]							
0x25		15:8		TSC[14:8]						
0x26		23:16								
0x27		31:24								
0x28	TOCC	7:0						TOS[1:0]		ETOC
0x29		15:8								
0x2A		23:16	TOP[7:0]							
0x2B		31:24	TOP[15:8]							

Offset	Name	Bit Pos.								
0xB6		23:16			F1PI[5:0]					
0xB7		31:24	DMS[1:0]						RF1L	F1F
0xB8	RXF1A	7:0			F1AI[5:0]					
0xB9		15:8								
0xBA		23:16								
0xBB		31:24								
0xBC	RXESC	7:0		F1DS[2:0]				F0DS[2:0]		
0xBD		15:8						RBDS[2:0]		
0xBE		23:16								
0xBF		31:24								
0xC0	TXBC	7:0	TBSA[7:0]							
0xC1		15:8	TBSA[15:8]							
0xC2		23:16			NDTB[5:0]					
0xC3		31:24		TFQM	TFQS[5:0]					
0xC4	TXFQS	7:0			TFFL[5:0]					
0xC5		15:8				TFGI[4:0]				
0xC6		23:16			TFQF	TFQPI[4:0]				
0xC7		31:24								
0xC8	TXESC	7:0						TBDS[2:0]		
0xC9		15:8								
0xCA		23:16								
0xCB		31:24								
0xCC	TXBRP	7:0	TRPn	TRPn	TRPn	TRPn	TRPn	TRPn	TRPn	TRPn
0xCD		15:8	TRPn	TRPn	TRPn	TRPn	TRPn	TRPn	TRPn	TRPn
0xCE		23:16	TRPn	TRPn	TRPn	TRPn	TRPn	TRPn	TRPn	TRPn
0xCF		31:24	TRPn	TRPn	TRPn	TRPn	TRPn	TRPn	TRPn	TRPn
0xD0	TXBAR	7:0	ARn	ARn	ARn	ARn	ARn	ARn	ARn	ARn
0xD1		15:8	ARn	ARn	ARn	ARn	ARn	ARn	ARn	ARn
0xD2		23:16	ARn	ARn	ARn	ARn	ARn	ARn	ARn	ARn
0xD3		31:24	ARn	ARn	ARn	ARn	ARn	ARn	ARn	ARn
0xD4	TXBCR	7:0	CRn	CRn	CRn	CRn	CRn	CRn	CRn	CRn
0xD5		15:8	CRn	CRn	CRn	CRn	CRn	CRn	CRn	CRn
0xD6		23:16	CRn	CRn	CRn	CRn	CRn	CRn	CRn	CRn
0xD7		31:24	CRn	CRn	CRn	CRn	CRn	CRn	CRn	CRn
0xD8	TXBTO	7:0	TOn	TOn	TOn	TOn	TOn	TOn	TOn	TOn
0xD9		15:8	TOn	TOn	TOn	TOn	TOn	TOn	TOn	TOn
0xDA		23:16	TOn	TOn	TOn	TOn	TOn	TOn	TOn	TOn
0xDB		31:24	TOn	TOn	TOn	TOn	TOn	TOn	TOn	TOn
0xDC	TXBCF	7:0	CFn	CFn	CFn	CFn	CFn	CFn	CFn	CFn
0xDD		15:8	CFn	CFn	CFn	CFn	CFn	CFn	CFn	CFn
0xDE		23:16	CFn	CFn	CFn	CFn	CFn	CFn	CFn	CFn
0xDF		31:24	CFn	CFn	CFn	CFn	CFn	CFn	CFn	CFn
0xE0	TXBTIE	7:0	TIEn	TIEn	TIEn	TIEn	TIEn	TIEn	TIEn	TIEn
0xE1		15:8	TIEn	TIEn	TIEn	TIEn	TIEn	TIEn	TIEn	TIEn
0xE2		23:16	TIEn	TIEn	TIEn	TIEn	TIEn	TIEn	TIEn	TIEn
0xE3		31:24	TIEn	TIEn	TIEn	TIEn	TIEn	TIEn	TIEn	TIEn
0xE4	TXBCIE	7:0	CFIEn	CFIEn	CFIEn	CFIEn	CFIEn	CFIEn	CFIEn	CFIEn

All enabled filter elements are used for acceptance filtering of standard frames. Acceptance filtering stops at the first matching enabled filter element or when the end of the filter list is reached. If SFEC = “100”, “101”, or “110” a match sets interrupt flag IR.HPM and, if enabled, an interrupt is generated. In this case register HPMS is updated with the status of the priority match.

Table 34-14. Standard Filter Element Configuration

Value	Name	Description
0x0	DISABLE	Disable filter element
0x1	STF0M	Store in Rx FIFO 0 if filter matches
0x2	STF1M	Store in Rx FIFO 1 if filter matches
0x3	REJECT	Reject ID if filter matches
0x4	PRIORITY	Set priority if filter matches.
0x5	PRIF0M	Set priority and store in FIFO 0 if filter matches.
0x6	PRIF1M	Set priority and store in FIFO 1 if filter matches.
0x7	STRXBUF	Store into Rx Buffer or as debug message, configuration of SFT[1:0] ignored.

- Bits 26:16 - SFID1[10:0]: Standard Filter ID 1

  First ID of standard ID filter element.

  When filtering for Rx Buffers or for debug messages this field defines the ID of a standard mesage to be stored. The received identifiers must match exactly, no masking mechanism is used.
- Bits 15:11 - Reserved
- Bits 10:0 - SFID2[10:0]: Standard Filter ID 2

  This bit field has a different meaning depending on the configuration of SFEC.

  5.1. SFEC = “001” ... “110”: Second ID of standard ID filter element.

  5.2. SFEC = “111”: Filter for Rx Buffers or for debug messages.

  SFID2[10:9] decides whether the received message is stored into an Rx Buffer or treated as message A, B, or C of the debug message sequence.
  00 = Store message into an Rx Buffer
  01 = Debug Message A
  10 = Debug Message B
  11 = Debug Message C

  SFID2[8:6] is used to control the filter event pins at the Extension Interface. A ‘1’ at the respective bit position enables generation of a pulse at the related filter event pin with the duration of one CLK_CAN_APB period in case the filter matches.

  SFID2[5:0] defines the offset to the Rx Buffer Start Address RXBC.RBSA for storage of a matching message.

34.9.6 Extended Message ID Filter Element

Up to 64 filter elements can be configured for 29-bit extended IDs. When accessing an Extended Message ID Filter element, its address is the Filter List Extended Start Address XIDFC.FLESA plus two times the index of the filter element (0…63).

This bit is set when the synchronization of ENABLE bit between clock domains is started.

Bit 0 – SWRST: SWRST Synchronization Busy
This bit is cleared when the synchronization of SWRST bit between the clock domains is complete.

This bit is set when the synchronization of SWRST bit between clock domains is started.

35.7.3.13 Counter Value, 32-bit Mode

Note: Prior to any read access, this register must be synchronized by user by writing the according TC Command value to the Control B Set register (CTRLBSET.CMD=READSYNC).

Name: COUNT
Offset: 0x14 [ID-00001cd8]
Reset: 0x00
Property: PAC Write-Protection, Write-Synchronized, Read-Synchronized

Bit	31	30	29	28	27	26	25	24
	COUNT[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	COUNT[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	COUNT[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	COUNT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – COUNT[31:0]: Counter Value
These bits contain the current counter value.

35.7.3.14 Period Value, 32-bit Mode

Name: PER
Offset: 0x1A [ID-00001cd8]
Reset: 0xFFFFFFFF
Property: Write-Synchronized

Name: STATUSB
Offset: 0x08
Reset: 0x00
Property: Read-Only

Bit	7	6	5	4	3	2	1	0
					READYx	READYx	READYx	READYx
Access					R	R	R	R
Reset					0	0	0	0

Bits 3,2,1,0 – READYx: Comparator x Ready
This bit is cleared when the comparator x output is not ready.
This bit is set when the comparator x output is ready.

If comparator x is not implemented, READYx always reads as zero.

40.8.9 Debug Control

Name: DBGCTRL
Offset: 0x09 [ID-00000fbb]
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
								DBGRUN
Access								R/W
Reset								0

Bit 0 – DBGRUN: Debug Run
This bit is not reset by a software reset.

This bits controls the functionality when the CPU is halted by an external debugger.

Value	Description
0	The AC is halted when the CPU is halted by an external debugger. Any on-going comparison will complete.
1	The AC continues normal operation when the CPU is halted by an external debugger.

40.8.10 Window Control

Name: WINCTRL
Offset: 0x0A
Reset: 0x00
Property: PAC Write-Protection, Write-Synchronized

47. Electrical Characteristics 105°C (SAM C20/C21 N)

47.1 Disclaimer

All typical values are measured at Ta = 25°C unless otherwise specified. All minimum and maximum values are valid across operating temperature and voltage unless otherwise specified.

This chapter contains only characteristics specific for the SAM C20/C21N devices (Ta = 105°C). For all other values or missing characteristics, refer to the SAM C20/C21E/G/J 85°C and 105°C chapters.

Related Links

Electrical Characteristics 85°C (SAM C20/C21 E/G/J)

47.2 General Operating Ratings

The device must operate within the ratings listed in the table below in order for all other electrical characteristics and typical characteristics of the device to be valid.

Table 47-1. General operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
T_A	Temperature range	-40	25	105	°C
T_J	Junction temperature	-	-	125	°C

47.3 Power Consumption

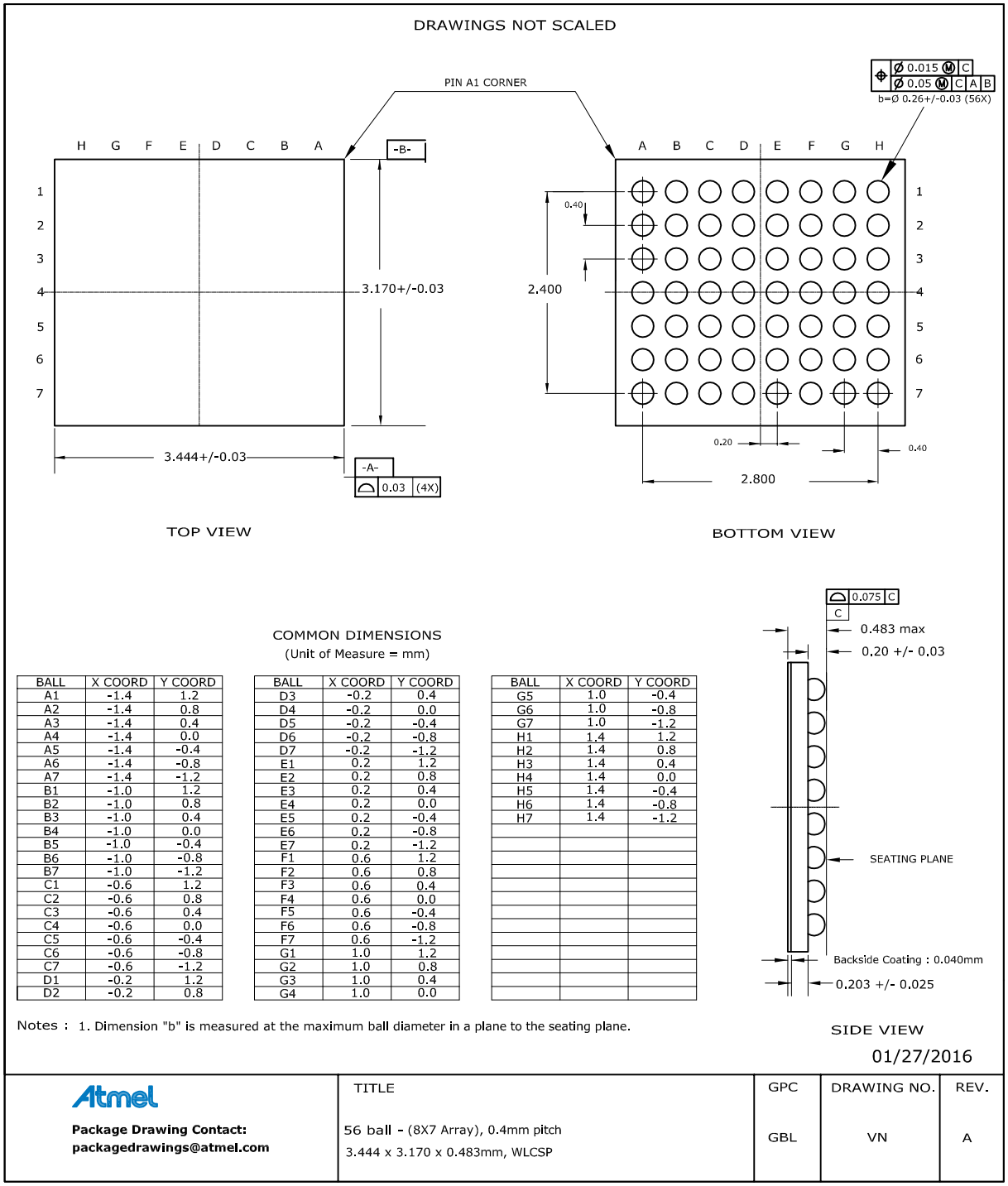
Table 47-2. Power Consumption(1)

Mode	Conditions	Ta	Vcc	Typ.	Max.	Units
ACTIVE	CPU running a While 1 algorithm	25°C	5.0V	3.8	4.2	mA
		105°C	5.0V	4.0	5.0	
	CPU running a While 1 algorithm	25°C	3.0V	3.7	4.1	mA
		105°C	3.0V	4.0	5.0	
	CPU running a While 1 algorithm. with GCLKIN as reference	25°C	5.0V	71*Freq+160	78*Freq+162	µA (with freq in MHz)
		105°C	5.0V	71*Freq+374	68*Freq+1564	
	CPU running a Fibonacci algorithm	25°C	5.0V	4.7	5.2	mA
		105°C	5.0V	5.0	6.1	
	CPU running a Fibonacci algorithm	25°C	3.0V	4.7	5.1	mA
		105°C	3.0V	5.0	6.0	
	CPU running a Fibonacci algorithm. with GCLKIN as reference	25°C	5.0V	90*Freq+163	99*Freq+168	µA (with freq in MHz)
		105°C	5.0V	90*Freq+379	90*Freq+1568	
	CPU running a CoreMark algorithm	25°C	5.0V	5.9	6.4	mA

Table 48-10. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E3

48.2.4 56-Ball WLCSP



BALL	X COORD	Y COORD
A1	-1.4	1.2
A2	-1.4	0.8
A3	-1.4	0.4
A4	-1.4	0.0
A5	-1.4	-0.4
A6	-1.4	-0.8
A7	-1.4	-1.2
B1	-1.0	1.2
B2	-1.0	0.8
B3	-1.0	0.4
B4	-1.0	0.0
B5	-1.0	-0.4
B6	-1.0	-0.8
B7	-1.0	-1.2
C1	-0.6	1.2
C2	-0.6	0.8
C3	-0.6	0.4
C4	-0.6	0.0
C5	-0.6	-0.4
C6	-0.6	-0.8
C7	-0.6	-1.2
D1	-0.2	1.2
D2	-0.2	0.8

BALL	X COORD	Y COORD
D3	-0.2	0.4
D4	-0.2	0.0
D5	-0.2	-0.4
D6	-0.2	-0.8
D7	-0.2	-1.2
E1	0.2	1.2
E2	0.2	0.8
E3	0.2	0.4
E4	0.2	0.0
E5	0.2	-0.4
E6	0.2	-0.8
E7	0.2	-1.2
F1	0.6	1.2
F2	0.6	0.8
F3	0.6	0.4
F4	0.6	0.0
F5	0.6	-0.4
F6	0.6	-0.8
F7	0.6	-1.2
G1	1.0	1.2
G2	1.0	0.8
G3	1.0	0.4
G4	1.0	0.0

BALL	X COORD	Y COORD
G5	1.0	-0.4
G6	1.0	-0.8
G7	1.0	-1.2
H1	1.4	1.2
H2	1.4	0.8
H3	1.4	0.4
H4	1.4	0.0
H5	1.4	-0.4
H6	1.4	-0.8
H7	1.4	-1.2

Table 48-11. Device and Package Maximum Weight

9.63	mg

resistor. External or internal pull up/down resistors can be used, e.g. the pins can be configured in pull-up or pull-down mode eliminating the need for external components. There are no obvious benefit in choosing external vs. internal pull resistors.

Related Links

PORT - I/O Pin Controller

49.7 Clocks and Crystal Oscillators

The SAM C20/C21 can be run from internal or external clock sources, or a mix of internal and external sources. An example of usage will be to use the internal 8MHz oscillator as source for the system clock, and an external 32.768kHz watch crystal as clock source for the Real-Time counter (RTC).

49.7.1 External Clock Source

Figure 49-6. External Clock Source Schematic

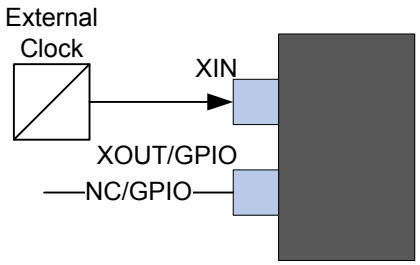
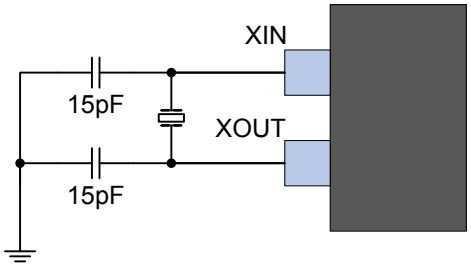


Table 49-4. External Clock Source Connections

Signal Name	Recommended Pin Connection	Description
XIN	XIN is used as input for an external clock signal	Input for inverting oscillator pin
XOUT/GPIO	Can be left unconnected or used as normal GPIO	NC/GPIO

49.7.2 Crystal Oscillator

Figure 49-7. Crystal Oscillator Schematic



The crystal should be located as close to the device as possible. Long signal lines may cause too high load to operate the crystal, and cause crosstalk to other parts of the system.

Table 49-5. Crystal Oscillator Checklist

Signal Name	Recommended Pin Connection	Description
XIN	Load capacitor 15pF(1)(2)	External crystal between 0.4 to 32MHz
XOUT	Load capacitor 15pF(1)(2)	

ADC – Analog-to-Digital Converter	• Block Diagram: Renamed ADC input signals from ADC to AIN. • Signal Description: Renamed ADC signal to AIN
PTC - Peripheral Touch Controller	• Block Diagram updated. • Section Self-capacitance Sensor Arrangement updated.

50.12 Rev B - 06/2015

Ordering Information	• Remove carrier type Tray option.

50.13 Rev A - 04/2015

Initial revision.