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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, WDT
Number of I/O	26
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-VQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamc20e17a-mnt

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Table 13-5. AMOD Bit Descriptions for MBIST

AMOD[1:0]	Description
0x0	Exit on Error
0x1	Pause on Error
0x2, 0x3	Reserved

Related Links

NVMCTRL – Non-Volatile Memory Controller Security Bit Product Mapping

13.11.6 System Services Availability when Accessed Externally and Device is Protected

External access: Access performed in the DSU address offset 0x200-0x1FFF range.

Internal access: Access performed in the DSU address offset 0x000-0x100 range.

Table 13-6. Available Features when Operated From The External Address Range and Device is Protected

Features	Availability From The External Address Range and Device is Protected
Chip-Erase command and status	Yes
CRC32	Yes, only full array or full EEPROM
CoreSight Compliant Device identification	Yes
Debug communication channels	Yes
Testing of onboard memories (MBIST)	No
STATUSA.CRSTEXT clearing	No (STATUSA.PERR is set when attempting to do so)

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Bits 7:4 – CCLASS[3:0]: Component Class

These bits will always return 0x1 when read indicating that this ARM CoreSight component is ROM table (refer to the ARM Debug Interface v5 Architecture Specification at http://www.arm.com).

Bits 3:0 – PREAMBLE[3:0]: Preamble

These bits will always return 0x00 when read.

13.13.21 Component Identification 2

 Name:
 CID2

 Offset:
 0x1FF8

 Reset:
 0x0000005

 Property:

15.4 Enabling a Peripheral

To enable a peripheral clocked by a generic clock, the following parts of the system needs to be configured:

- A running clock source.
- A clock from the Generic Clock Generator must be configured to use one of the running clock sources, and the generator must be enabled.
- The generic clock, through the Generic Clock Multiplexer, that connects to the peripheral needs to be configured with a running clock from the Generic Clock Generator, and the generic clock must be enabled.
- The user interface of the peripheral needs to be unmasked in the PM. If this is not done the peripheral registers will read as all 0's and any writes to the peripheral will be discarded.

15.5 On-demand, Clock Requests

Figure 15-3. Clock request routing



All the clock sources in the system can be run in an on-demand mode, where the clock source is in a stopped state when no peripherals are requesting the clock source. Clock requests propagate from the peripheral, via the GCLK, to the clock source. If one or more peripheral is using a clock source, the clock source will be started/kept running. As soon as the clock source is no longer needed and no peripheral have an active request the clock source will be stopped until requested again. For the clock request to reach the clock source, the peripheral, the generic clock and the clock from the Generic Clock Generator in-between must be enabled. The time taken from a clock request being asserted to the clock source being ready is dependent on the clock source startup time, clock source frequency as well as the divider used in the Generic Clock Generator. The total startup time from a clock request to the clock is available for the peripheral is:

```
Delay_start_max = Clock source startup time + 2 * clock source periods + 2 * divided clock
source periods
Delay_start_min = Clock source startup time + 1 * clock source period + 1 * divided clock
source periodDelay_start_min = Clock source startup time + 1 * clock source period + 1 *
divided clock source period
```

The delay for shutting down the clock source when there is no longer an active request is:

Delay_stop_min = 1 * divided clock source period + 1 * clock source period
Delay_stop_max = 2 * divided clock source periods + 2 * clock source periods

The On-Demand principle can be disabled individually for each clock source by clearing the ONDEMAND bit located in each clock source controller. The clock is always running whatever is the clock request. This has the effect to remove the clock source startup time at the cost of the power consumption.

In standby mode, the clock request mechanism is still working if the modules are configured to run in standby mode (RUNSTDBY bit).

17.7 Register Summary

Offset	Name	Bit Pos.								
0x00	CTRLA	7:0								
0x01	INTENCLR	7:0								CKRDY
0x02	INTENSET	7:0								CKRDY
0x03	INTFLAG	7:0								CKRDY
0x04	Reserved									
0x05	CPUDIV	7:0				CPUD	IV[7:0]			
0x06										
	Reserved									
0x0F										
0x10		7:0	DMAC	HSRAM	NVMCTRL	HMATRIXHS	DSU	APBC	APBB	APBA
0x11	AHBMASK	15:8						PAC	CAN1	CAN0
0x12		23:16								
0x13		31:24								
0x14		7:0	GCLK	SUPC	OSC32KCTR L	OSCCTRL	RSTC	MCLK	РМ	PAC
0x15	APBAMASK	15:8				TSENS	FREQM	EIC	RTC	WDT
0x16		23:16								
0x17		31:24								
0x18		7:0			HMATRIXHS			NVMCTRL	DSU	PORT
0x19		15:8								
0x1A	AFBBWASK	23:16								
0x1B		31:24								
0x1C		7:0		SERCOM5	SERCOM4	SERCOM3	SERCOM2	SERCOM1	SERCOM0	EVSYS
0x1D	ADROMASK	15:8	TC3	TC2	TC1	TC0	TCC2	TCC1	TCC0	
0x1E	AFBOWASK	23:16	CCL	PTC	DAC	AC	SDADC	ADC1	ADC0	TC4
0x1F		31:24								
0x20		7:0				TC7	TC6	TC5	SERCOM7	SERCOM6
0x21		15:8								
0x22	AFDUWASK	23:16								
0x23		31:24								

17.8 Register Description

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16-, and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly.

Some registers can be write-protected optionally by the Peripheral Access Controller (PAC). This is denoted by the property "PAC Write-Protection" in each individual register description. Refer to the Register Access Protection for details.

17.8.1 Control A

All bits in this register are reserved.

Some registers require synchronization when read and/or written. Synchronization is denoted by the "Read-Synchronized" and/or "Write-Synchronized" property in each individual register description.

Optional write-protection by the Peripheral Access Controller (PAC) is denoted by the "PAC Write-Protection" property in each individual register description.

Some registers are enable-protected, meaning they can only be written when the module is disabled. Enable-protection is denoted by the "Enable-Protected" property in each individual register description.

24.8.1 Control A in COUNT32 mode (CTRLA.MODE=0)

 Name:
 CTRLA

 Offset:
 0x00

 Reset:
 0x0000

 Property:
 PAC Write-Protection, Enable-Protected, Write-Synchronized

Bit	15	14	13	12	11	10	9	8		
	COUNTSYNC				PRESCALER[3:0]					
Access	R/W				R/W	R/W	R/W	R/W		
Reset	0				0	0	0	0		
Bit	7	6	5	4	3	2	1	0		
	MATCHCLR				MOD	E[1:0]	ENABLE	SWRST		
Access	R/W			·	R/W	R/W	R/W	R/W		
Reset	0				0	0	0	0		

Bit 15 – COUNTSYNC: COUNT Read Synchronization Enable

The COUNT register requires synchronization when reading. Disabling the synchronization will prevent reading valid values from the COUNT register.

This bit is not enable-protected.

Value	Description
0	COUNT read synchronization is disabled
1	COUNT read synchronization is enabled

Bits 11:8 - PRESCALER[3:0]: Prescaler

These bits define the prescaling factor for the RTC clock source (GCLK_RTC) to generate the counter clock (CLK_RTC_CNT). Periodic events and interrupts are not available when the prescaler is off. These bits are not synchronized.

Value	Name	Description
0x0	OFF	CLK_RTC_CNT = GCLK_RTC/1
0x1	DIV1	CLK_RTC_CNT = GCLK_RTC/1
0x2	DIV2	CLK_RTC_CNT = GCLK_RTC/2
0x3	DIV4	CLK_RTC_CNT = GCLK_RTC/4
0x4	DIV8	CLK_RTC_CNT = GCLK_RTC/8
0x5	DIV16	CLK_RTC_CNT = GCLK_RTC/16
0x6	DIV32	CLK_RTC_CNT = GCLK_RTC/32
0x7	DIV64	CLK_RTC_CNT = GCLK_RTC/64
0x8	DIV128	CLK_RTC_CNT = GCLK_RTC/128
0x9	DIV256	CLK_RTC_CNT = GCLK_RTC/256

Offset	Name	Bit Pos.								
0x2E		23:16	PBLDATA[23:16]							
0x2F		31:24	PBLDATA[31:24]							

27.8 Register Description

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16-, and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly.

Some registers require synchronization when read and/or written. Synchronization is denoted by the "Read-Synchronized" and/or "Write-Synchronized" property in each individual register description.

Some registers are enable-protected, meaning they can only be written when the module is disabled. Enable-protection is denoted by the "Enable-Protected" property in each individual register description.

27.8.1 Control A

Name:CTRLAOffset:0x00 [ID-00000b2c]Reset:0x0000Property:PAC Write-Protection

Bit	15	14	13	12	11	10	9	8	
				CMD	EX[7:0]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0	
Bit	7	6	5	4	3	2	1	0	
			CMD[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset		0	0	0	0	0	0	0	

Bits 15:8 – CMDEX[7:0]: Command Execution

When this bit group is written to the key value 0xA5, the command written to CMD will be executed. If a value different from the key value is tried, the write will not be performed and the Programming Error bit in the Status register (STATUS.PROGE) will be set. PROGE is also set if a previously written command is not completed yet.

The key value must be written at the same time as CMD. If a command is issued through the APB bus on the same cycle as an AHB bus access, the AHB bus access will be given priority. The command will then be executed when the NVM block and the AHB bus are idle.

INTFLAG.READY must be '1' when the command is issued.

Bit 0 of the CMDEX bit group will read back as '1' until the command is issued.

Note: The NVM Address bit field in the Address register (ADDR.ADDR) uses 16-bit addressing.

Bits 6:0 - CMD[6:0]: Command

These bits define the command to be executed when the CMDEX key is written.

Value	Description
0	The PMUXn registers of the selected pins will not be updated.
1	The PMUXn registers of the selected pins will be updated.

Bits 27:24 – PMUX[3:0]: Peripheral Multiplexing

These bits determine the new value written to the Peripheral Multiplexing register (PMUXn) for all pins selected by the WRCONFIG.PINMASK and WRCONFIG.HWSEL bits, when the WRCONFIG.WRPMUX bit is set.

These bits will always read as zero.

Bit 22 – DRVSTR: Output Driver Strength Selection

This bit determines the new value written to PINCFGy.DRVSTR for all pins selected by the WRCONFIG.PINMASK and WRCONFIG.HWSEL bits, when the WRCONFIG.WRPINCFG bit is set.

This bit will always read as zero.

Bit 18 – PULLEN: Pull Enable

This bit determines the new value written to PINCFGy.PULLEN for all pins selected by the WRCONFIG.PINMASK and WRCONFIG.HWSEL bits, when the WRCONFIG.WRPINCFG bit is set.

This bit will always read as zero.

Bit 17 – INEN: Input Enable

This bit determines the new value written to PINCFGy.INEN for all pins selected by the WRCONFIG.PINMASK and WRCONFIG.HWSEL bits, when the WRCONFIG.WRPINCFG bit is set.

This bit will always read as zero.

Bit 16 – PMUXEN: Peripheral Multiplexer Enable

This bit determines the new value written to PINCFGy.PMUXEN for all pins selected by the WRCONFIG.PINMASK and WRCONFIG.HWSEL bits, when the WRCONFIG.WRPINCFG bit is set.

This bit will always read as zero.

Bits 15:0 – PINMASK[15:0]: Pin Mask for Multiple Pin Configuration

These bits select the pins to be configured within the half-word group selected by the WRCONFIG.HWSEL bit.

These bits will always read as zero.

Value	Description
0	The configuration of the corresponding I/O pin in the half-word group will be left unchanged.
1	The configuration of the corresponding I/O pin in the half-word PORT group will be updated.

28.9.12 Event Input Control

Tip: The I/O pins are assembled in pin groups ("PORT groups") with up to 32 pins. Group 0 consists of the PA pins, group 1 is for the PB pins, etc. Each pin group has its own PORT registers. For example, the register address offset for the Data Direction (DIR) register for group 0 (PA00 to PA31) is 0x00, and the register address offset for the DIR register for group 1 (PB00 to PB31) is 0x80.

31.3 Block Diagram

Figure 31-1. USART Block Diagram



31.4 Signal Description

Table 31-1. SERCOM USART Signals

Signal Name	Туре	Description
PAD[3:0]	Digital I/O	General SERCOM pins

One signal can be mapped to one of several pins.

Related Links

I/O Multiplexing and Considerations

31.5 **Product Dependencies**

In order to use this peripheral, other parts of the system must be configured correctly, as described below.

31.5.1 I/O Lines

Using the USART's I/O lines requires the I/O pins to be configured using the I/O Pin Controller (PORT).

When the SERCOM is used in USART mode, the SERCOM controls the direction and value of the I/O pins according to the table below. Both PORT control bits PINCFGn.PULLEN and PINCFGn.DRVSTR are still effective. If the receiver or transmitter is disabled, these pins can be used for other purposes.

Table 31-2. USART Pin Configuration

Pin	Pin Configuration
TxD	Output
RxD	Input
ХСК	Output or input

The combined configuration of PORT and the Transmit Data Pinout and Receive Data Pinout bit fields in the Control A register (CTRLA.TXPO and CTRLA.RXPO, respectively) will define the physical position of the USART signals in Table 31-2.

Value	Description
0	SWRST synchronization is not busy.
1	SWRST synchronization is busy.

32.8.9 Address

Name:ADDROffset:0x24 [ID-0000e74]Reset:0x0000000Property:PAC Write-Protection, Enable-Protected



Bits 23:16 – ADDRMASK[7:0]: Address Mask

These bits hold the address mask when the transaction format with address is used (CTRLA.FORM, CTRLB.AMODE).

Bits 7:0 - ADDR[7:0]: Address

These bits hold the address when the transaction format with address is used (CTRLA.FORM, CTRLB.AMODE).

32.8.10 Data

 Name:
 DATA

 Offset:
 0x28 [ID-00000e74]

 Reset:
 0x0000

 Property:
 –

Bit 22 – MEXTTOEN: Master SCL Low Extend Time-Out

This bit enables the master SCL low extend time-out. If SCL is cumulatively held low for greater than 10ms from START-to-ACK, ACK-to-ACK, or ACK-to-STOP the master will release its clock hold if enabled, and complete the current transaction. A STOP will automatically be transmitted.

SB or MB will be set as normal, but CLKHOLD will be released. The MEXTTOUT and BUSERR status bits will be set.

This bit is not synchronized.

Value	Description
0	Time-out disabled
1	Time-out enabled

Bits 21:20 – SDAHOLD[1:0]: SDA Hold Time

These bits define the SDA hold time with respect to the negative edge of SCL.

These bits are not synchronized.

Value	Name	Description
0x0	DIS	Disabled
0x1	75NS	50-100ns hold time
0x2	450NS	300-600ns hold time
0x3	600NS	400-800ns hold time

Bit 16 – PINOUT: Pin Usage

This bit set the pin usage to either two- or four-wire operation:

This bit is not synchronized.

Value	Description
0	4-wire operation disabled.
1	4-wire operation enabled.

Bit 7 – RUNSTDBY: Run in Standby

This bit defines the functionality in standby sleep mode.

This bit is not synchronized.

Value	Description
0	GCLK_SERCOMx_CORE is disabled and the I ² C master will not operate in standby sleep
	mode.
1	GCLK_SERCOMx_CORE is enabled in all sleep modes.

Bits 4:2 – MODE[2:0]: Operating Mode

These bits must be written to 0x5 to select the I²C master serial communication interface of the SERCOM.

These bits are not synchronized.

Bit 1 – ENABLE: Enable

Due to synchronization, there is delay from writing CTRLA.ENABLE until the peripheral is enabled/ disabled. The value written to CTRL.ENABLE will read back immediately and the Synchronization Enable Busy bit in the Synchronization Busy register (SYNCBUSY.ENABLE) will be set. SYNCBUSY.ENABLE will be cleared when the operation is complete.

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Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access				Į		Į	ļ	
Reset								
Bit	15	14	13	12	11	10	9	8
		TXP	EFBI	PXHD			BRSE	FDOE
Access		R/W	R/W	R/W			R/W	R/W
Reset		0	0	0			0	0
Bit	7	6	5	4	3	2	1	0
	TEST	DAR	MON	CSR	CSA	ASM	CCE	INIT
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	1

Bit 14 – TXP: Transmit Pause

This bit field is write-restricted and only writable if bit fields CCE = 1 and INIT = 1.

Value	Description
0	Transmit pause disabled.
1	Transmit pause enabled. The CAN pauses for two CAN bit times before starting the next
	transmission after itself has successfully transmitted a frame.

Bit 13 – EFBI: Edge Filtering during Bus Integration

Value	Description
0	Edge filtering is disabled.
1	Two consecutive dominant tq required to detect an edge for hard synchronization.

Bit 12 – PXHD: Protocol Exception Handling Disable

Note: When protocol exception handling is disabled, the CAN will transmit an error frame when it detects a protocol exception condition.

Value	Description
0	Protocol exception handling enabled.
1	Protocol exception handling disabled.

Bit 9 – BRSE: Bit Rate Switch Enable

Note: When CAN FD operation is disabled FDOE = 0, BRSE is not evaluated.

Value	Description
0	Bit rate switching for transmissions disabled.
1	Bit rate switching for transmissions enabled.

Bit 8 – FDOE: FD Operation Enable

Table 34-11. Event Type

Value	Name	Description
0x0 or 0x3	RES	Reserved
0x1	TXE	Tx event
0x2	TXC	Transmission in spite of cancellation (always set for transmission in DAR mode)

- E1 Bit 21 FDF: FD Format
 - 0 : Standard frame format.
 - 1 : CAN FD frame format (new DLC-coding and CRC).
- E1 Bit 20 BRS: Bit Rate Search
 - 0 : Frame received without bit rate switching.
 - 1 : Frame received with bit rate switching.
- E1 Bits 19:16 DLC[3:0]: Data Length Code

0-8 : CAN + CAN FD: received frame has 0-8 data bytes.

9-15 : CAN: received frame has 8 data bytes.

9-15 : CAN FD: received frame has 12/16/20/24/32/48/64 data bytes.

E1 Bits 15:0 - TXTS[15:0]: Tx Timestamp

Timestamp Counter value captured on start of frame transmission. Resolution depending on configuration of the Timestamp Counter Prescaler TSCC.TCP.

34.9.5 Standard Message ID Filter Element

Up to 128 filter elements can be configured for 11-bit standard IDs. When accessing a Standard Message ID Filter element, its address is the Filter List Standard Start Address SIDFC.FLSSA plus the index of the filter element (0 ... 127).

Table 34-12. Standard Message ID Filter Element

		31	3 0	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
[20	SFT SFEC				SEID1[10:0]															<u></u>		0.01										
ľ	50	[1:0]		[2:0]		SFID I[10:0]																	SFI	טצניי	0.0]							

Bits 31:30 - SFT[1:0]: Standard Filter Type

This field defines the standard filter type.

Table 3	4-13.	Standard	Filter	Туре
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Value	Name	Description
0x0	RANGE	Range filter from SFID1 to SFID2 (SFID2 >= SFID1)
0x1	DUAL	Dual ID filter for SFID1 or SFID2
0x2	CLASSIC	Classic filter: SFID1 = filter, SFID2 = mask
0x3	RES	Reserved

• Bits 29:27 - SFEC[2:0]: Standard Filter Element Configuration

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Bit	31	30	29	28	27	26	25	24
				CAPTMC	DDE1[1:0]		CAPTMO	DE0[1:0]
Access				R/W	R/W		R/W	R/W
Reset				0	0		0	0
Bit	23	22	21	20	19	18	17	16
			COPEN1	COPEN0			CAPTEN1	CAPTEN0
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0
Bit	15	14	13	12	11	10	9	8
					ALOCK	F	PRESCALER[2:0]
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0
Bit	7	6	5	4	3	2	1	0
	ONDEMAND	RUNSTDBY	PRESCS	YNC[1:0]	MOD	E[1:0]	ENABLE	SWRST
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	W
Reset	0	0	0	0	0	0	0	0

Bits 28:27 – CAPTMODE1[1:0]: Capture mode Channel 1

These bits select the channel 1 capture mode.

Value	Name	Description
0x0	DEFAULT	Default capture
0x1	CAPTMIN	Minimum capture
0x2	CAPTMAX	Maximum capture
0x3		Reserved

Bits 25:24 – CAPTMODE0[1:0]: Capture mode Channel 0

These bits select the channel 0 capture mode.

Value	Name	Description
0x0	DEFAULT	Default capture
0x1	CAPTMIN	Minimum capture
0x2	CAPTMAX	Maximum capture
0x3		Reserved

Bits 20, 21 – COPENx: Capture On Pin x Enable

Bit x of COPEN[1:0] selects the trigger source for capture operation, either events or I/O pin input.

Value	Description
0	Event from Event System is selected as trigger source for capture operation on channel x.
1	I/O pin is selected as trigger source for capture operation on channel x.

Bits 16, 17 – CAPTENx: Capture Channel x Enable

Bit x of CAPTEN[1:0] selects whether channel x is a capture or a compare channel.

These bits are not synchronized.

Bits 16, 17 – CAPTENx: Capture Channel x Enable

Bit x of CAPTEN[1:0] selects whether channel x is a capture or a compare channel.

These bits are not synchronized.

Value	Description
0	CAPTEN disables capture on channel x.
1	CAPTEN enables capture on channel x.

Bit 11 – ALOCK: Auto Lock

When this bit is set, Lock bit update (LUPD) is set to '1' on each overflow/underflow or re-trigger event.

This bit is not synchronized.

Value	Description
0	The LUPD bit is not affected on overflow/underflow, and re-trigger event.
1	The LUPD bit is set on each overflow/underflow or re-trigger event.

Bits 10:8 – PRESCALER[2:0]: Prescaler

These bits select the counter prescaler factor.

These bits are not synchronized.

Value	Name	Description
0x0	DIV1	Prescaler: GCLK_TC
0x1	DIV2	Prescaler: GCLK_TC/2
0x2	DIV4	Prescaler: GCLK_TC/4
0x3	DIV8	Prescaler: GCLK_TC/8
0x4	DIV16	Prescaler: GCLK_TC/16
0x5	DIV64	Prescaler: GCLK_TC/64
0x6	DIV256	Prescaler: GCLK_TC/256
0x7	DIV1024	Prescaler: GCLK_TC/1024

Bit 7 – ONDEMAND: Clock On Demand

This bit selects the clock requirements when the TC is stopped.

In standby mode, if the Run in Standby bit (CTRLA.RUNSTDBY) is '0', ONDEMAND is forced to '0'.

This bit is not synchronized.

Value	Description
0	The On Demand is disabled. If On Demand is disabled, the TC will continue to request the clock when its operation is stopped (STATUS.STOP=1).
1	The On Demand is enabled. When On Demand is enabled, the stopped TC will not request the clock. The clock is requested when a software re-trigger command is applied or when an event with start/re-trigger action is detected.

Bit 6 – RUNSTDBY: Run in Standby

This bit is used to keep the TC running in standby mode.

This bit is not synchronized.

Value	Description
0	The TC is halted in standby.
1	The TC continues to run in standby.

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Bit	31	30	29	28	27	26	25	24
					MCEOx	MCEOx	MCEOx	MCEOx
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0
Bit	23	22	21	20	19	18	17	16
					MCEIx	MCEIx	MCEIx	MCEIx
Access			•		R/W	R/W	R/W	R/W
Reset					0	0	0	0
Bit	15	14	13	12	11	10	9	8
	TCEIx	TCEIx	TCINVx	TCINVx		CNTEO	TRGEO	OVFEO
Access	R/W	R/W	R/W	R/W		R/W	R/W	R/W
Reset	0	0	0	0		0	0	0
Bit	7	6	5	4	3	2	1	0
	CNTSEL[1:0]		EVACT1[2:0]			EVACT0[2:0]		
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 27,26,25,24 – MCEOx: Match or Capture Channel x Event Output Enable

These bits control if the Match/capture event on channel x is enabled and will be generated for every match or capture.

Value	Description
0	Match/capture x event is disabled and will not be generated.
1	Match/capture x event is enabled and will be generated for every compare/capture on channel x.

Bits 19,18,17,16 – MCEIx: Match or Capture Channel x Event Input Enable

These bits indicate if the Match/capture x incoming event is enabled

These bits are used to enable match or capture input events to the CCx channel of TCC.

Value	Description
0	Incoming events are disabled.
1	Incoming events are enabled.

Bits 15,14 – TCEIx: Timer/Counter Event Input x Enable

This bit is used to enable input event x to the TCC.

Value	Description
0	Incoming event x is disabled.
1	Incoming event x is enabled.

Bits 13,12 – TCINVx: Timer/Counter Event x Invert Enable

This bit inverts the event x input.

Value	Description
0	Input event source x is not inverted.
1	Input event source x is inverted.

Table 37-4. D-Latch Characteristics

G	D	ουτ
0	Х	Hold state (no change)
1	0	Clear
1	1	Set

RS Latch (RS)

When this configuration is selected, the S-input is driven by the even LUT output (LUT0 and LUT2), and the R-input is driven by the odd LUT output (LUT1 and LUT3), as shown in Figure 37-17.

Figure 37-17. RS-Latch



When the even LUT is disabled LUTCTRL0.ENABLE=0 / LUTCTRL2.ENABLE=0), the latch output will be cleared. The R-input is forced enabled for one more APB clock cycle and S-input to zero. In all other cases, the latch output (OUT) is refreshed as shown in Table 37-5.

Table 37-5. RS-Latch Characteristics

S	R	ουτ
0	0	Hold state (no change)
0	1	Clear
1	0	Set
1	1	Forbidden state

37.6.3 Events

The CCL can generate the following output events:

• OUTx: Lookup Table Output Value

Writing a '1' to the LUT Control Event Output Enable bit (LUTCTRL.LUTEO) enables the corresponding output event. Writing a '0' to this bit disables the corresponding output event.

The CCL can take the following actions on an input event:

• INSELx: The event is used as input for the TRUTH table. For further details refer to Events.

Writing a '1' to the LUT Control Event Input Enable bit (LUTCTRL.LUTEI) enables the corresponding action on input event. Writing a '0' to this bit disables the corresponding action on input event.



Figure 38-9. ADC Master - Slave Block Diagram

In this mode of operation, the slave ADC is enabled by accessing the CTRLA register of master ADC. In the same way, the master ADC event inputs will be automatically routed to the slave ADC, meaning that the input events configuration must be done in the master ADC (ADC0.EVCTRL).

Note: If several events are connected to the ADC, the enabled action will be taken on any of the incoming events. If FLUSH and START events are available at the same time, the FLUSH event has priority.

Related Links

EVSYS - Event System

38.6.7 Sleep Mode Operation

The ONDEMAND and RUNSTDBY bits in the Control A register (CTRLA) control the behavior of the ADC during standby sleep mode, in cases where the ADC is enabled (CTRLA.ENABLE = 1). For further details on available options, refer to Table 38-4.

Note: When CTRLA.ONDEMAND=1, the analog block is powered-off when the conversion is complete. When a start request is detected, the system returns from sleep and starts a new conversion after the start-up time delay.

CTRLA.RUNSTDBY	CTRLA.ONDEMAND	CTRLA.ENABLE	Description
x	x	0	Disabled
0	0	1	Run in all sleep modes except STANDBY.
0	1	1	Run in all sleep modes on request, except STANDBY.
1	0	1	Run in all sleep modes.
1	1	1	Run in all sleep modes on request.

Table 38-4. ADC Sleep Behavior

38.6.8 Synchronization

Due to asynchronicity between the main clock domain and the peripheral clock domains, some registers need to be synchronized when written or read.

The following bits are synchronized when written:

- Software Reset bit in Control A register (CTRLA.SWRST)
- Enable bit in Control A register (CTRLA.ENABLE)

The following registers are synchronized when written:

- Input Control register (INPUTCTRL)
- Control C register (CTRLC)
- Average control register (AVGCTRL)
- Sampling time control register (SAMPCTRL)
- Window Monitor Lower Threshold register (WINLT)
- Window Monitor Upper Threshold register (WINUT)
- Gain correction register (GAINCORR)
- Offset Correction register (OFFSETCORR)
- Software Trigger register (SWTRIG)

Required write-synchronization is denoted by the "Write-Synchronized" property in the register description.

Related Links

Bit 2 – FLUSHINV: Flush Event Invert Enable

For the slave ADC, this bit has no effect when the SLAVEEN bit is set (CTRLA.SLAVEEN= 1).

Value	Description
0	Flush event input source is not inverted.
1	Flush event input source is inverted.

Bit 1 – STARTEI: Start Conversion Event Input Enable

For the slave ADC, this bit has no effect when the SLAVEEN bit is set (CTRLA.SLAVEEN= 1).

Value	Description
0	A new conversion will not be triggered on any incoming event.
1	A new conversion will be triggered on any incoming event.

Bit 0 – FLUSHEI: Flush Event Input Enable

For the slave ADC, this bit has no effect when the SLAVEEN bit is set (CTRLA.SLAVEEN= 1).

Value	Description
0	A flush and new conversion will not be triggered on any incoming event.
1	A flush and new conversion will be triggered on any incoming event.

38.8.5 Interrupt Enable Clear

This register allows the user to disable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Set (INTENSET) register.

Name:INTENCLROffset:0x04 [ID-0000120e]Reset:0x00Property:PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
						WINMON	OVERRUN	RESRDY
Access						R/W	R/W	R/W
Reset						0	0	0

Bit 2 – WINMON: Window Monitor Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Window Monitor Interrupt Enable bit, which disables the corresponding interrupt request.

Value	Description
0	The window monitor interrupt is disabled.
1	The window monitor interrupt is enabled, and an interrupt request will be generated when the
	Window Monitor interrupt flag is set.

Bit 1 – OVERRUN: Overrun Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Overrun Interrupt Enable bit, which disables the corresponding interrupt request.

1. These are based on characterization.

46.4.4 Digital-to-Analog Converter (DAC) Characteristics Table 46-7. Power Consumption⁽¹⁾

Symbol	Parameters	Conditions	Та	Тур.	Max	Units
IDD VDDANA	DC supply current	Output buffer On, VREF = VDDANA=5.0V	Max 105°C Typ 25°C	318	414	μA
		Output buffer Off, VREF = VDDANA=0.5V		74	82	

1. These values are based on characterization.

46.4.5 Analog Comparator (AC) Characteristics Table 46-8. Power Consumption⁽¹⁾

Symbol	Parameters	Conditions	Та	Тур.	Max	Units
IDDANA	Current consumption - Vcm=Vddana/2,	COMPCTRLn.SPEED = 0x0, VDDANA =3.3V	Max 105°C Typ 25°C	10	13	μA
	+-100 mV overdrive from Vcm, Voltage scaler disabled	COMPCTRLn.SPEED = 0x3, VDDANA =3.3V		39	51	
	Current consumption Voltage scaler only	VDDANA =3.3V		43	57	

1. These values are based on characterization.

46.4.6 Temperature Sensor Characteristics

Table 46-9. Temperature Sensor Characteristics⁽¹⁾

Parameter	Condition	Min.	Max.	Unit
Accuracy	[-40,105]°C	-14.6	10.5	°C

1. These are based on characterization. Data has been obtained by averaging 10 TSENS acquisitions per measurement.

46.5 NVM Characteristics

Table 46-10. Flash Endurance

Symbol	Parameter	Conditions	Min.	Тур.	Units
Cyc _{NVM}	Cycling Endurance ⁽¹⁾	-40°C < T _A < 105°C	5k	-	Cycles

1. An endurance cycle is a write and an erase operation.

Table 46-11. EEPROM Emulation⁽¹⁾ Endurance

Symbol	Parameter	Conditions	Min.	Тур.	Units
Cyc _{EEPROM}	Cycling Endurance ⁽²⁾	-40°C < T _A < 105°C	100k	-	Cycles