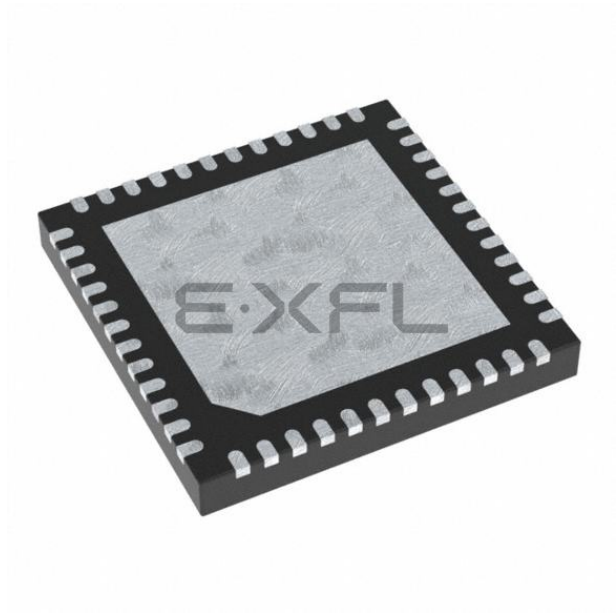

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, WDT
Number of I/O	38
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamc20g15a-mnt

	SAM C21N	SAM C21J	SAM C21G	SAM C21E
Digital-to-Analog Converter (DAC) channels	1	1	1	1
Temperature Sensor (TSENS)	1	1	1	1
Real-Time Counter (RTC)	Yes	Yes	Yes	Yes
RTC alarms	1	1	1	1
RTC compare values	One 32-bit value or two 16-bit values	One 32-bit value or two 16-bit values	One 32-bit value or two 16-bit values	One 32-bit value or two 16-bit values
External Interrupt lines	16 with HW debouncing	16	16	16
Peripheral Touch Controller (PTC) Number of self-capacitance channels (Y-lines)	32	32	22	16
Peripheral Touch Controller (PTC) Number of mutual-capacitance channels (X x Y lines)	256 (16x16)	256 (16x16)	121 (11x11)	64 (8x8)
Frequency Meter (FREQM) reference clock divider	Yes	Yes	Yes	Yes
Maximum CPU frequency	48 MHz			
Packages	TQFP	QFN TQFP WLCSP	QFN TQFP	QFN TQFP
Oscillators	32.768 kHz crystal oscillator (XOSC32K) 0.4-32 MHz crystal oscillator (XOSC) 32.768 kHz internal oscillator (OSC32K) 32 kHz ultra low-power internal oscillator (OSCULP32K) 48 MHz high-accuracy internal oscillator (OSC48M) 96 MHz Fractional Digital Phased Locked Loop (FDPLL96M)			
Event System channels	12	12	12	12
SW Debug Interface	Yes	Yes	Yes	Yes
Watchdog Timer (WDT)	Yes	Yes	Yes	Yes

Peripheral Name	Base Address	IRQ Line	AHB Clock		APB Clock		Generic Clock	PAC		Events		DMA	
			Index	Enabled at Reset	Index	Enabled at Reset	Index	Index	Prot at Reset	User	Generator	Index	Sleep Walking
										45: STOP			
AHB-APB Bridge C	0x42000000		2	Y									N/A
EVSYS	0x42000000	8			0	N	6-17: one per CHANNEL	0	N				Y
SERCOM0	0x42000400	9			1	N	19: CORE 18: SLOW	1	N			2: RX 3: TX	Y
SERCOM1	0x42000800	10			2	N	20: CORE 18: SLOW	2	N			4: RX 5: TX	Y
SERCOM2	0x42000C00	11			3	N	21: CORE 18: SLOW	3	N			6: RX 7: TX	Y
SERCOM3	0x42001000	12			4	N	22: CORE 18: SLOW	4	N			8: RX 9: TX	Y
SERCOM4	0x42001400	13			5	N	23: CORE 18: SLOW	5	N			10: RX 11: TX	Y
SERCOM5	0x42001800	14			6	N	25: CORE 24: SLOW	6	N			12: RX 13: TX	Y
CAN0	0x42001C00	15	8	N			26					14: DEBUG	N/A
CAN1	0x42002000	16	9	N			27					15: DEBUG	N/A
TCC0	0x42002400	17			9	N	28	9	N	9-10: EV0-1 11-14: MC0-3	34: OVF 35: TRG 36: CNT 37-40: MC0-3	16: OVF 17-20: MC0-3	Y
TCC1	0x42002800	18			10	N	28	10	N	15-16: EV0-1 17-18: MC0-1	41: OVF 42: TRG 43: CNT 44-45: MC0-1	21: OVF 22-23: MC0-1	Y
TCC2	0x42002C00	19			11	N	29	11	N	19-20: EV0-1 21-22: MC0-1	46: OVF 47: TRG 48: CNT 49-50: MC0-1	24: OVF 25-26: MC0-1	Y
TC0	0x42003000	20			12	N	30	12	N	23: EVU	51: OVF 52-53: MC0-1	27: OVF 28-29: MC0-1	Y
TC1	0x42003400	21			13	N	30	13	N	24: EVU	54: OVF 55-56: MC0-1	30: OVF 21-32: MC0-1	Y
TC2	0x42003800	22			14	N	31	14	N	25: EVU	57: OVF 58-59: MC0-1	33: OVF 23-35: MC0-1	Y
TC3	0x42003C00	23			15	N	31	15	N	26: EVU	60: OVF 61-62: MC0-1	36: OVF 37-38: MC0-1	Y
TC4	0x42004000	24			16	N	32	16	N	27: EVU	63: OVF 64-65: MC0-1	39: OVF 40-41: MC0-1	Y
ADC0	0x42004400	25			17	N	33	17	N	28: START 29: SYNC	66: RESRDY 67: WINMON	42: RESRDY	Y
ADC1	0x42004800	26			18	N	34	18	N	30: START 31: SYNC	68: RESRDY 69: WINMON	43: RESRDY	Y
SDADC	0x42004C00	29			19	N	35	19	N	32: START 33: FLUSH	70: RESRDY 71: WINMON	44: RESRDY	Y
AC	0x42005000	27			20	N	34	20	N	34-37: SOC0-3	72-75: COMP0-3 76-77: WIN0-1		Y

Frequencies must never exceed the specified maximum frequency for each clock domain.

Value	Name	Description
0x01	DIV1	Divide by 1
0x02	DIV2	Divide by 2
0x04	DIV4	Divide by 4
0x08	DIV8	Divide by 8
0x10	DIV16	Divide by 16
0x20	DIV32	Divide by 32
0x40	DIV64	Divide by 64
0x80	DIV128	Divide by 128
others	-	Reserved

17.8.6 AHB Mask

Note: This register is only available for SAMC2x "N" series devices.

Name: AHBMASK
Offset: 0x10 [ID-00001086]
Reset: 0x000003CFF
Property: PAC Write-Protection

Bit	31	30	29	28	27	26	25	24
Access			R	R	R	R	R	R
Reset			0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
						PAC	CAN1	CAN0
Access	R	R	R	R	R	R/W	R/W	R/W
Reset	0	0	0	0	1	1	0	0

Bit	7	6	5	4	3	2	1	0
	DMAC	HSRAM	NVMCTRL	HMATRIXHS	DSU	APBC	APBB	APBA
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit 13 – APBD: APBD AHB Clock Enable

Value	Description
0	The AHB clock for the APBD is stopped.
1	The AHB clock for the APBD is enabled.

Bit 12 – DIVAS: DIVAS AHB Clock Enable

Bit	7	6	5	4	3	2	1	0
	ONDEMAND	RUNSTDBY					ENABLE	
Access	R/W	R/W					R/W	
Reset	1	0					0	

Bit 7 – ONDEMAND: On Demand Clock Activation
The On Demand operation mode allows the DPLL to be enabled or disabled depending on peripheral clock requests.

If the ONDEMAND bit has been previously written to '1', the DPLL will only be running when requested by a peripheral. If there is no peripheral requesting the DPLL's clock source, the DPLL will be in a disabled state.

If On Demand is disabled the DPLL will always be running when enabled.

In standby sleep mode, the On Demand operation is still active.

Value	Description
0	The DPLL is always on, if enabled.
1	The DPLL is enabled when a peripheral is requesting the DPLL to be used as a clock source. The DPLL is disabled if no peripheral is requesting the clock source.

Bit 6 – RUNSTDBY: Run in Standby
This bit controls how the DPLL behaves during standby sleep mode:

Value	Description
0	The DPLL is disabled in standby sleep mode if no peripheral requests the clock.
1	The DPLL is not stopped in standby sleep mode. If ONDEMAND=1, the DPLL will be running when a peripheral is requesting the clock. If ONDEMAND=0, the clock source will always be running in standby sleep mode.

Bit 1 – ENABLE: DPLL Enable
The software operation of enabling or disabling the DPLL takes a few clock cycles, so the DPLLSYNCBUSY.ENABLE status bit indicates when the DPLL is successfully enabled or disabled.

Value	Description
0	The DPLL is disabled.
1	The DPLL is enabled.

20.8.13 DPLL Ratio Control

Name: DPLLRATIO
Offset: 0x20 [ID-00001eee]
Reset: 0x00
Property: PAC Write-Protection, Write-Synchronized

Name: EWCTRL
Offset: 0x02
Reset: X determined from NVM User Row
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
					EWOFFSET[3:0]			
Access					R/W	R/W	R/W	R/W
Reset					x	x	x	x

Bits 3:0 – EWOFFSET[3:0]: Early Warning Interrupt Time Offset
These bits determine the number of GCLK_WDT clock cycles between the start of the watchdog time-out period and the generation of the Early Warning interrupt. These bits are loaded from NVM User Row at start-up.

Value	Name	Description
0x0	CYC8	8 clock cycles
0x1	CYC16	16 clock cycles
0x2	CYC32	32 clock cycles
0x3	CYC64	64 clock cycles
0x4	CYC128	128 clock cycles
0x5	CYC256	256 clock cycles
0x6	CYC512	512 clock cycles
0x7	CYC1024	1024 clock cycles
0x8	CYC2048	2048 clock cycles
0x9	CYC4096	4096 clock cycles
0xA	CYC8192	8192 clock cycles
0xB	CYC16384	16384 clock cycles
0xC - 0xF	-	Reserved

23.8.4 Interrupt Enable Clear

This register allows the user to disable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Set (INTENSET) register.

Name: INTENCLR
Offset: 0x04 [ID-0000067a]
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
								EW
Access								R/W
Reset								0

Bit 0 – EW: Early Warning Interrupt Enable
Writing a '0' to this bit has no effect.

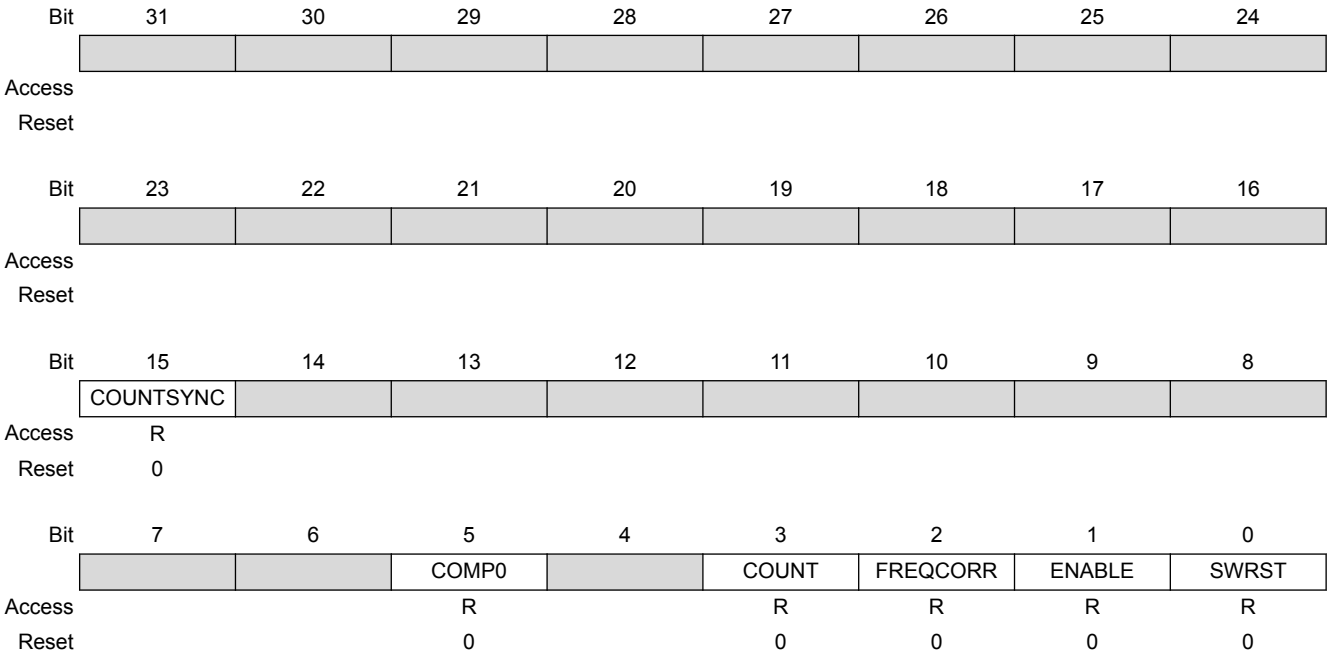
Writing a '1' to this bit clears the Early Warning Interrupt Enable bit, which disables the Early Warning interrupt.

This bit controls the functionality when the CPU is halted by an external debugger.

Value	Description
0	The RTC is halted when the CPU is halted by an external debugger.
1	The RTC continues normal operation when the CPU is halted by an external debugger.

24.8.7 Synchronization Busy in COUNT32 mode (CTRLA.MODE=0)

Name: SYNCBUSY
Offset: 0x10
Reset: 0x00000000
Property: -



Bit 15 – COUNTSYNC: Count Read Sync Enable Synchronization Busy Status

Value	Description
0	Write synchronization for CTRLA.COUNTSYNC bit is complete.
1	Write synchronization for CTRLA.COUNTSYNC bit is ongoing.

Bit 5 – COMP0: Compare 0 Synchronization Busy Status

Value	Description
0	Write synchronization for COMP0 register is complete.
1	Write synchronization for COMP0 register is ongoing.

Bit 3 – COUNT: Count Value Synchronization Busy Status

Value	Description
0	Read/write synchronization for COUNT register is complete.
1	Read/write synchronization for COUNT register is ongoing.

Name: INTENSET
Offset: 0x0A
Reset: 0x0000
Property: PAC Write-Protection

Bit	15	14	13	12	11	10	9	8
	OVF							ALARM0
Access	R/W							R/W
Reset	0							0

Bit	7	6	5	4	3	2	1	0
	PERn	PERn	PERn	PERn	PERn	PERn	PERn	PERn
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – OVF: Overflow Interrupt Enable
Writing a '0' to this bit has no effect. Writing a '1' to this bit will set the Overflow Interrupt Enable bit, which enables the Overflow interrupt.

Value	Description
0	The Overflow interrupt is disabled.
1	The Overflow interrupt is enabled.

Bit 8 – ALARM0: Alarm 0 Interrupt Enable
Writing a '0' to this bit has no effect. Writing a '1' to this bit will set the Alarm 0 Interrupt Enable bit, which enables the Alarm 0 interrupt.

Value	Description
0	The Alarm 0 interrupt is disabled.
1	The Alarm 0 interrupt is enabled.

Bits 7:0 – PERn: Periodic Interval n Interrupt Enable [n = 7..0]
Writing a '0' to this bit has no effect. Writing a '1' to this bit will set the Periodic Interval n Interrupt Enable bit, which enables the Periodic Interval n interrupt.

Value	Description
0	Periodic Interval n interrupt is disabled.
1	Periodic Interval n interrupt is enabled.

24.12.5 Interrupt Flag Status and Clear in Clock/Calendar mode (CTRLA.MODE=2)

Name: INTFLAG
Offset: 0x0C
Reset: 0x0000
Property: -

Bit	31	30	29	28	27	26	25	24
	OUTCLR[31:24]							
Access	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	OUTCLR[23:16]							
Access	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	OUTCLR[15:8]							
Access	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	OUTCLR[7:0]							
Access	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – OUTCLR[31:0]: PORT Data Output Value Clear
Writing '0' to a bit has no effect.

Writing '1' to a bit will clear the corresponding bit in the OUT register. Pins configured as outputs via the Data Direction register (DIR) will be set to low output drive level. Pins configured as inputs via DIR and with pull enabled via the Pull Enable bit in the Pin Configuration register (PINCFG.PULLEN) will set the input pull direction to an internal pull-down.

Value	Description
0	The corresponding I/O pin in the PORT group will keep its configuration.
1	The corresponding I/O pin output is driven low, or the input is connected to an internal pull-down.

28.9.7 Data Output Value Set

This register allows the user to set one or more output I/O pin drive levels high, without doing a read-modify-write operation. Changes in this register will also be reflected in the Data Output Value (OUT), Data Output Value Toggle (OUTTGL) and Data Output Value Clear (OUTCLR) registers.

Tip: The I/O pins are assembled in pin groups (”PORT groups”) with up to 32 pins. Group 0 consists of the PA pins, group 1 is for the PB pins, etc. Each pin group has its own PORT registers. For example, the register address offset for the Data Direction (DIR) register for group 0 (PA00 to PA31) is 0x00, and the register address offset for the DIR register for group 1 (PB00 to PB31) is 0x80.

Name: OUTSET
Offset: 0x18
Reset: 0x00000000
Property: PAC Write-Protection

counter is stopped. At this moment, the 13 most significant bits of the counter (value divided by 8) give the new clock divider (BAUD.BAUD), and the 3 least significant bits of this value (the remainder) give the new Fractional Part (BAUD.FP).

When the Sync Field has been received, the clock divider (BAUD.BAUD) and the Fractional Part (BAUD.FP) are updated after a synchronization delay. After the Break and Sync Fields are received, multiple characters of data can be received.

31.6.3.5 LIN Master

LIN master is available with the following configuration:

- LIN master format (CTRLA.FORM = 0x02)
- Asynchronous mode (CTRLA.CMODE = 0)
- 16x sample rate using fractional baud rate generation (CTRLA.SAMPR = 1)

LIN frames start with a header transmitted by the master. The header consists of the break, sync, and identifier fields. After the master transmits the header, the addressed slave will respond with 1-8 bytes of data plus checksum.

Figure 31-12. LIN Frame Format

Using the LIN command field (CTRLB.LINCMD), the complete header can be automatically transmitted, or software can control transmission of the various header components.

When CTRLB.LINCMD=0x1, software controls transmission of the LIN header. In this case, software uses the following sequence.

- CTRLB.LINCMD is written to 0x1.
- DATA register written to 0x00. This triggers transmission of the break field by hardware. Note that writing the DATA register with any other value will also result in the transmission of the break field by hardware.
- DATA register written to 0x55. The 0x55 value (sync) is transmitted.
- DATA register written to the identifier. The identifier is transmitted.

When CTRLB.LINCMD=0x2, hardware controls transmission of the LIN header. In this case, software uses the following sequence.

- CTRLB.LINCMD is written to 0x2.
- DATA register written to the identifier. This triggers transmission of the complete header by hardware. First the break field is transmitted. Next, the sync field is transmitted, and finally the identifier is transmitted.

In LIN master mode, the length of the break field is programmable using the break length field (CTRLC.BRKLEN). When the LIN header command is used (CTRLB.LINCMD=0x2), the delay between the break and sync fields, in addition to the delay between the sync and ID fields are configurable using the header delay field (CTRLC.HDRDLY). When manual transmission is used (CTRLB.LINCMD=0x1), software controls the delay between break and sync.

33.5.2 Power Management

This peripheral can continue to operate in any sleep mode where its source clock is running. The interrupts can wake up the device from sleep modes.

Related Links

PM – Power Manager

33.5.3 Clocks

The SERCOM bus clock (CLK_SERCOMx_APB) can be enabled and disabled in the Main Clock Controller. Refer to *Peripheral Clock Masking* for details and default status of this clock.

Two generic clocks are used by SERCOM, GCLK_SERCOMx_CORE and GCLK_SERCOM_SLOW. The core clock (GCLK_SERCOMx_CORE) can clock the I^2C when working as a master. The slow clock (GCLK_SERCOM_SLOW) is required only for certain functions, e.g. SMBus timing. These two clocks must be configured and enabled in the Generic Clock Controller (GCLK) before using the I^2C.

These generic clocks are asynchronous to the bus clock (CLK_SERCOMx_APB). Due to this asynchronicity, writes to certain registers will require synchronization between the clock domains. Refer to Synchronization for further details.

Related Links

GCLK - Generic Clock Controller

Peripheral Clock Masking

PM – Power Manager

33.5.4 DMA

The DMA request lines are connected to the DMA Controller (DMAC). In order to use DMA requests with this peripheral the DMAC must be configured first. Refer to *DMAC – Direct Memory Access Controller* for details.

Related Links

DMAC – Direct Memory Access Controller

33.5.5 Interrupts

The interrupt request line is connected to the Interrupt Controller. In order to use interrupt requests of this peripheral, the Interrupt Controller (NVIC) must be configured first. Refer to *Nested Vector Interrupt Controller* for details.

Related Links

Nested Vector Interrupt Controller

33.5.6 Events

Not applicable.

33.5.7 Debug Operation

When the CPU is halted in debug mode, this peripheral will continue normal operation. If the peripheral is configured to require periodical service by the CPU through interrupts or similar, improper operation or data loss may result during debugging. This peripheral can be forced to halt operation during debugging - refer to the Debug Control (DBGCTRL) register for details.

33.5.8 Register Access Protection

Registers with write-access can be write-protected optionally by the peripheral access controller (PAC).

PAC Write-Protection is not available for the following registers:

Bit	31	30	29	28	27	26	25	24
	NDn	NDn	NDn	NDn	NDn	NDn	NDn	NDn
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	NDn	NDn	NDn	NDn	NDn	NDn	NDn	NDn
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NDn	NDn	NDn	NDn	NDn	NDn	NDn	NDn
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NDn	NDn	NDn	NDn	NDn	NDn	NDn	NDn
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – NDn: New Data n [n = 0..31]
The register holds the New Data flags of Rx Buffers 0 to 31. The flags are set when the respective Rx Buffer has been updated from a received frame. The flags remain set until the Host clears them. A flag is cleared by writing 1 to the corresponding bit position. Writing a 0 has no effect. A hard reset will clear the register.

34.8.26 New Data 2

Name: NDAT2
Offset: 0x9C
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
	TOn	TOn	TOn	TOn	TOn	TOn	TOn	TOn
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	TOn	TOn	TOn	TOn	TOn	TOn	TOn	TOn
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TOn	TOn	TOn	TOn	TOn	TOn	TOn	TOn
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TOn	TOn	TOn	TOn	TOn	TOn	TOn	TOn
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – TOn: Transmission Occurred

Each Tx Buffer has its own Transmission Occurred bit.

The bits are set when the corresponding TXBRP bit is cleared after a successful transmission.

The bits are reset when a new transmission is requested by writing ‘1’ to the corresponding bit of register TXBAR.

34.8.42 Tx Buffer Cancellation Finished

Name: TXBCF
Offset: 0xDC [ID-0000a4bb]
Reset: 0x00000000
Property: Read-only

Table 34-15. Extended Message ID Filter Element

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F0	EFEC [2:0]			EFID1[28:0]																												
F1	EFT [1:0]			EFID2[28:0]																												

- F0 Bits 31:29 - EFEC[2:0]: Extended Filter Element Configuration

  All enabled filter elements are used for acceptance filtering of extended frames. Acceptance filtering stops at the first matching enabled filter element or when the end of the filter list is reached. If EFEC = “100”, “101”, or “110” a match sets interrupt flag IR.HPM and, if enabled, an interrupt is generated. In this case register HPMS is updated with the status of the priority match.

Table 34-16. Extended Filter Element Configuration

Value	Name	Description
0x0	DISABLE	Disable filter element.
0x1	STF0M	Store in Rx FIFO 0 if filter matches.
0x2	STF1M	Store in Rx FIFO 1 if filter matches.
0x3	REJECT	Reject ID if filter matches.
0x4	PRIORITY	Set priority if filter matches.
0x5	PRIF0M	Set priority and store in FIFO 0 if filter matches.
0x6	PRIF1M	Set priority and store in FIFO 1 if filter matches.
0x7	STRXBUF	Store into Rx Buffer or as debug message, configuration of EFT[1:0] ignored.

- F0 Bits 28:0 - EFID1[28:0]: Extended Filter ID 1

  First ID of extended ID filter element.

  When filtering for Rx Buffers or for debug messages this field defines the ID of a extended mesage to be stored. The received identifiers must match exactly, only XIDAM masking mechanism is used.
- F1 Bits 31:30 - EFT[1:0]: Extended Filter Type

  This field defines the extended filter type.

Table 34-17. Extended Filter Type

Value	Name	Description
0x0	RANGEM	Range filter from EFID1 to EFID2 (EFID2 >= EFID1).
0x1	DUAL	Dual ID filter for EFID1 or EFID2.
0x2	CLASSIC	Classic filter: EFID1 = filter, EFID2 = mask.
0x3	RANGE	Range filter from EFID1 to EFID2 (EFID2 >= EFID1), XIDAM mask not applied.

- F1 Bits 28:0 - EFID2[28:0]: Extended Filter ID 2

This register allows the user to clear bits in the CTRLB register without doing a read-modify-write operation. Changes in this register will also be reflected in the Control B Set register (CTRLBSET).

Name: CTRLBCLR
Offset: 0x04
Reset: 0x00
Property: PAC Write-Protection, Read-Synchronized, Write-Synchronized

Bit	7	6	5	4	3	2	1	0
	CMD[2:0]					ONESHOT	LUPD	DIR
Access	R/W	R/W	R/W			R/W	R/W	R/W
Reset	0	0	0			0	0	0

Bits 7:5 – CMD[2:0]: Command
These bits are used for software control of the TC. The commands are executed on the next prescaled GCLK_TC clock cycle. When a command has been executed, the CMD bit group will be read back as zero.

Writing 0x0 to these bits has no effect.

Writing a '1' to any of these bits will clear the pending command.

Bit 2 – ONESHOT: One-Shot on Counter
This bit controls one-shot operation of the TC.

Writing a '0' to this bit has no effect

Writing a '1' to this bit will disable one-shot operation.

Value	Description
0	The TC will wrap around and continue counting on an overflow/underflow condition.
1	The TC will wrap around and stop on the next underflow/overflow condition.

Bit 1 – LUPD: Lock Update
This bit controls the update operation of the TC buffered registers.

When CTRLB.LUPD is set, no any update of the registers with value of its buffered register is performed on hardware UPDATE condition. Locking the update ensures that all buffer registers are valid before an hardware update is performed. After all the buffer registers are loaded correctly, the buffered registers can be unlocked.

This bit has no effect when input capture operation is enabled.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the LUPD bit.

Value	Description
0	The CCBUFx and PERBUF buffer registers value are copied into CCx and PER registers on hardware update condition.
1	The CCBUFx and PERBUF buffer registers value are not copied into CCx and PER registers on hardware update condition.

Bit 0 – DIR: Counter Direction
This bit is used to change the direction of the counter.

36.7 Register Summary

Offset	Name	Bit Pos.								
0x00	CTRLA	7:0		RESOLUTION[1:0]					ENABLE	SWRST
0x01		15:8	MSYNC	ALOCK	PRESCYNC[1:0]		RUNSTDBY	PRESCALER[2:0]		
0x02		23:16								
0x03		31:24					CPTEN3	CPTEN2	CPTEN1	CPTEN0
0x04	CTRLBCLR	7:0	CMD[2:0]			IDXCMD[1:0]		ONESHOT	LUPD	DIR
0x05	CTRLBSET	7:0	CMD[2:0]			IDXCMD[1:0]		ONESHOT	LUPD	DIR
0x06 ... 0x07	Reserved									
0x08	SYNCBUSY	7:0	PER	WAVE	PATT	COUNT	STATUS	CTRLB	ENABLE	SWRST
0x09		15:8					CC3	CC2	CC1	CC0
0x0A		23:16								
0x0B		31:24								
0x0C	FCTRLA	7:0	RESTART	BLANK[1:0]		QUAL	KEEP		SRC[1:0]	
0x0D		15:8		CAPTURE[2:0]			CHSEL[1:0]		HALT[1:0]	
0x0E		23:16	BLANKVAL[7:0]							
0x0F		31:24					FILTERVAL[3:0]			
0x10	FCTRLB	7:0	RESTART	BLANK[1:0]		QUAL	KEEP		SRC[1:0]	
0x11		15:8		CAPTURE[2:0]			CHSEL[1:0]		HALT[1:0]	
0x12		23:16	BLANKVAL[7:0]							
0x13		31:24					FILTERVAL[3:0]			
0x14	WEXCTRL	7:0							OTMX[1:0]	
0x15		15:8					DTIENx	DTIENx	DTIENx	DTIENx
0x16		23:16	DTLS[7:0]							
0x17		31:24	DTHS[7:0]							
0x18	DRVCTRL	7:0	NREx	NREx	NREx	NREx	NREx	NREx	NREx	NREx
0x19		15:8	NRVx	NRVx	NRVx	NRVx	NRVx	NRVx	NRVx	NRVx
0x1A		23:16	INVENx	INVENx	INVENx	INVENx	INVENx	INVENx	INVENx	INVENx
0x1B		31:24	FILTERVAL1[3:0]				FILTERVAL0[3:0]			
0x1C ... 0x1D	Reserved									
0x1E	DBGCTRL	7:0						FDDBD		DBGRUN
0x1F	Reserved									
0x20	EVCTRL	7:0	CNTSEL[1:0]		EVACT1[2:0]			EVACT0[2:0]		
0x21		15:8	TCEIx	TCEIx	TCINVx	TCINVx		CNTEO	TRGEO	OVFEO
0x22		23:16					MCEIx	MCEIx	MCEIx	MCEIx
0x23		31:24					MCEOx	MCEOx	MCEOx	MCEOx
0x24	INTENCLR	7:0					ERR	CNT	TRG	OVF
0x25		15:8	FAULTx	FAULTx	FAULTB	FAULTA	DFS	UFS		
0x26		23:16					MCx	MCx	MCx	MCx
0x27	Reserved									
0x28	INTENSET	7:0					ERR	CNT	TRG	OVF
0x29		15:8	FAULTx	FAULTx	FAULTB	FAULTA	DFS	UFS		

43.8.6 Interrupt Enable Set

This register allows the user to enable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Clear (INTENCLR) register.

Name: INTENSET
Offset: 0x05 [ID-00001f13]
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
					OVF	WINMON	OVERRUN	RESRDY
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 3 – OVF: Overflow Interrupt Enable
Writing a zero to this bit has no effect.

Writing a one to this bit will set the Overflow Interrupt bit, which enables the Overflow interrupt.

Value	Description
0	The Overflow interrupt is disabled.
1	The Overflow interrupt is enabled.

Bit 2 – WINMON: Window Monitor Interrupt Enable
Writing a zero to this bit has no effect.

Writing a one to this bit will set the Window Monitor Interrupt bit, which enables the Window Monitor interrupt.

Value	Description
0	The Window Monitor interrupt is disabled.
1	The Window Monitor interrupt is enabled.

Bit 1 – OVERRUN: Overrun Interrupt Enable
Writing a zero to this bit has no effect.

Writing a one to this bit will set the Overrun Interrupt Enable bit, which enables the corresponding interrupt request.

Value	Description
0	The Overrun interrupt is disabled.
1	The Overrun interrupt is enabled.

Bit 0 – RESRDY: Result Ready Interrupt Enable
Writing a zero to this bit has no effect.

Writing a one to this bit will set the Result Ready Interrupt bit, which enables the Result Ready interrupt.

Value	Description
0	The Result Ready interrupt is disabled.
1	The Result Ready interrupt is enabled.

43.8.7 Interrupt Flag Status and Clear

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
			TCAL[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			FCAL[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 13:8 – TCAL[5:0]: Temperature Calibration
This value from production test must be loaded from the NVM software calibration row into the CAL register by software to achieve the specified accuracy. The value must be copied only, and must not be changed.

Bits 5:0 – FCAL[5:0]: Frequency Calibration
This value from production test must be loaded from the NVM software calibration row into the CAL register by software to achieve the specified accuracy. The value must be copied only, and must not be changed.

43.8.16 Debug Control

Name: DBGCTRL
Offset: 0x24 [ID-00001f13]
Reset: 0x00
Property: –

Bit	7	6	5	4	3	2	1	0
								DBGRUN
Access								R/W
Reset								0

Bit 0 – DBGRUN: Debug Run
This bit is not reset by a software reset.

This bits controls the functionality when the CPU is halted by an external debugger.

Symbol	Parameter	Conditions		Measurement			Unit
				Min	Typ	Max	
			Vddana=2.7V Vref=2.0V	-	30.4	61.0	
INL	Integral Non Linearity	Fadc = 500 ksps	Vddana=5.0V Vref=Vddana	-	+/-2.4	+/-4	LSB
			Vddana=2.7V Vref=2.0V	-	+/-3.7	+/-6	
		Fadc = 1 Msps	Vddana=5.0V Vref=Vddana	-	+/-2.2	+/-4	
			Vddana=2.7V Vref=2.0V	-	+/-4.1	+/-6	
DNL	Differential Non Linearity	Fadc = 500 ksps	Vddana=5.0V Vref=Vddana	-	-0.8/+1.1	-1/+3.8	LSB
			Vddana=2.7V Vref=2.0V	-	-0.8/+1.1	-1/+1.7	
		Fadc = 1 Msps	Vddana=5.0V Vref=Vddana	-	-0.8/+1	-1/+2	
			Vddana=2.7V Vref=2.0V	-	-1/+1.1	-1/+2.4	
Gain	Gain Error (1)	Fadc = 1 Msps	Vddana=2.7V Vref=2.0V	-	+/-13	+/-28	mV
			Vddana=5.0V Vref=4.096V	-	+/-26	+/-52	
			Vddana=3.0V Vref=Vddana	-	+/-14	+/-24	
			Vddana=5.0V Vref=Vddana		+/-22	+/-42	
TCg	Gain Drift	Fadc = 1 Msps	Vddana=5.0V Vref=Vddana	-170	-140	-80	uV/°C
Offset	Offset Error (1)	Fadc = 1 Msps	Vddana=2.7V Vref=2.0V	-	+/-2.2	+/-21	mV
			Vddana=5.0V Vref=4.096V	-	+/-2.3	+/-61	
			Vddana=3.0V Vref=Vddana	-	+/-15	+/-42	
			Vddana=5.0V Vref=Vddana		+/-31	+/-80	
Tco	Offset Drift	Fadc = 1 Msps	Vddana=5.0V Vref=Vddana	160	180	210	µV/°C

48. Packaging Information

48.1 Thermal Considerations

48.1.1 Thermal Resistance Data

The following table summarizes the thermal resistance data depending on the package.

Table 48-1. Thermal Resistance Data

Package Type	θ_{JA}	θ_{JC}
32-pin TQFP	63.1°C/W	14.3°C/W
48-pin TQFP	62.7°C/W	11.6°C/W
64-pin TQFP	56.3°C/W	11.1°C/W
100-pin TQFP	55.0°C/W	11.1°C/W
32-pin QFN	40.5°C/W	16.0°C/W
48-pin QFN	30.9°C/W	10.4°C/W
64-pin QFN	31.4°C/W	10.2°C/W
56-ball WLCSP	37.5°C/W	5.48°C/W

48.1.2 Junction Temperature

The average chip-junction temperature, T_J, in °C can be obtained from the following:

1. $T_J = T_A + (P_D \times \theta_{JA})$
2. $T_J = T_A + (P_D \times (\theta_{HEATSINK} + \theta_{JC}))$

where:

- θ_{JA} = Package thermal resistance, Junction-to-ambient (°C/W), see Thermal Resistance Data
- θ_{JC} = Package thermal resistance, Junction-to-case thermal resistance (°C/W), see Thermal Resistance Data
- $\theta_{HEATSINK}$ = Thermal resistance (°C/W) specification of the external cooling device
- P_D = Device power consumption (W)
- T_A = Ambient temperature (°C)

From the first equation, the user can derive the estimated lifetime of the chip and decide if a cooling device is necessary or not. If a cooling device is to be fitted on the chip, the second equation should be used to compute the resulting average chip-junction temperature T_J in °C.

48.2 Package Drawings

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

RTC – Real-Time Counter	• Clock/Calendar (Mode 2): Updated description.
DMAC – Direct Memory Access Controller	• Sleep Mode Operation: Added information on behaviour of DMA channels with CHCTRLA.RUNSTDBY=0.
EIC – External Interrupt Controller	• Added interrupt pin debouncing.
SERCOM USART – SERCOM Universal Synchronous and Asynchronous Receiver and Transmitter	• LIN Master section added. • CTRLA.TXPO: Row heading updated from RTS to RTS/TE. • CTRLA.FORM: Added LIN Master to FORM[3:0]=0x2. Added LIN Slave to FORM[3:0]=0x4. • CTRLB.LINCMD[3:0] bit group added • CTRLC.GTIME: Bitfield values removed.
TC – Timer/Counter	• CTRLA.ENABLE and SWRST bit description updated: Added "This bit is not enable protected."
ADC – Analog-to-Digital Converter	• Reference Configuration: Removed information on number of external and internal voltage references and supported voltage supply range. This information is replaced with references to the REFCTRL.REFSEL register bits and ADC characteristics for reference selection details and voltage ranges respectively.
DAC – Digital-to-Analog Converter	• CTRLB.ION bit description updated: For bit value '1' the internal DAC can be used as input to the AC or ADC.
TSENS – Temperature Sensor	• Added example to the VALUE register.
Electrical Characteristics 85°C (SAM C20/C21 E/G/J)	• Absolute Maximum Ratings: VDD max updated from 5.5V to 6.1V. • General Operating Ratings: Updated note. • Injection Current: New section added. • Power Consumption: Standby typical values updated and maximum values added. • Analog-to-Digital Converter (ADC) Characteristics: – Added Ts, sampling tile with DAC as input. – Analog-to-Digital Converter (ADC) Characteristics: In the condition column REFCTRL.REFSEL is corrected to CTRLC.RESSEL. – Analog Comparator Characteristics: Removed Hysteresis for COMPCTRLn.SPEED = 0x0 (low power), Updated IDDANS units from nA to µA and updated condition for IDDANA with voltage scaler disabled (COMPCTRLn.SPEED = 0x1 changed to 0x3).