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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0+ |
| Core Size | 32-Bit Single-Core |
| Speed | 48MHz |
| Connectivity | I²C, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, POR, WDT |
| Number of I/O | 52 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | A/D 12x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-TQFP |
| Supplier Device Package | 64-TQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/atsamc20j16a-ant |

- Drop in compatible with SAM D20 and SAM D21 (see **Note**)

**Note:** Only applicable for 32-, 48-, and 64-pin TQFP and QFN packages.

# 6. I/O Multiplexing and Considerations

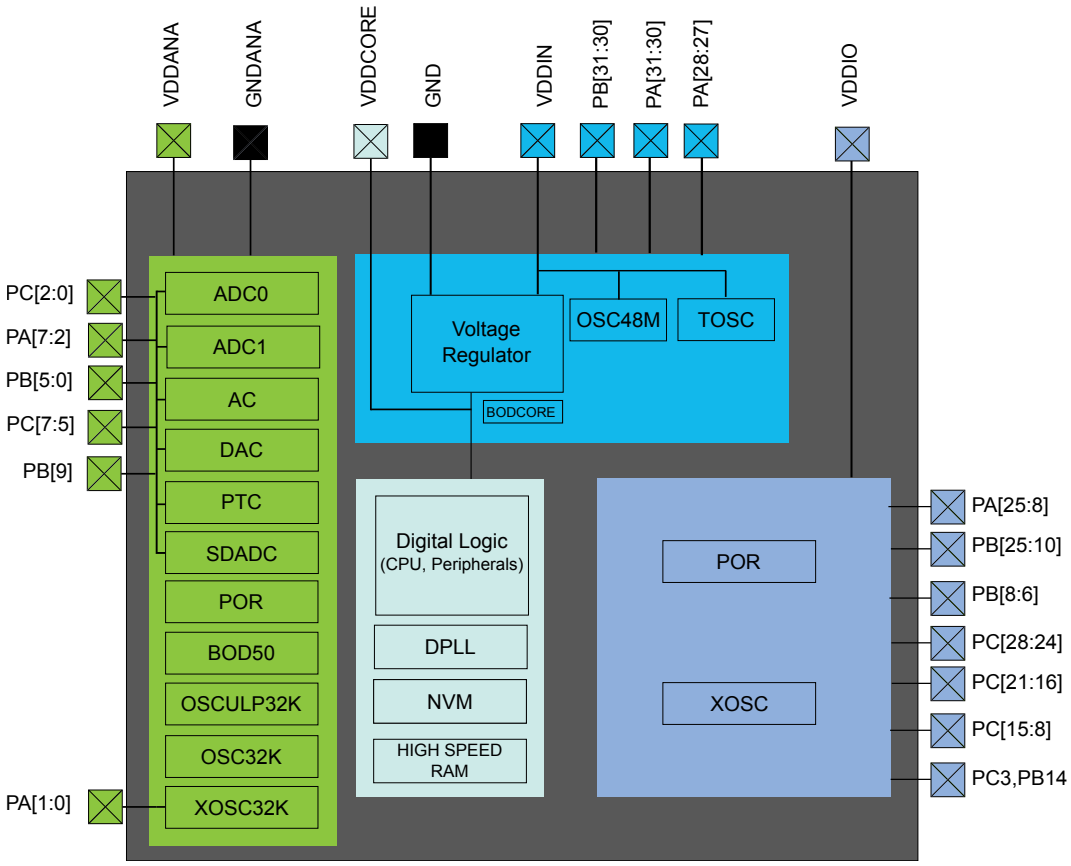
## 6.1 Multiplexed Signals

Each pin is by default controlled by the PORT as a general purpose I/O and alternatively it can be assigned to one of the peripheral functions A, B, C, D, E, F, G, H, or I. To enable a peripheral function on a pin, the Peripheral Multiplexer Enable bit in the Pin Configuration register corresponding to that pin (PINCFGn.PMUXEN, n = 0-31) in the PORT must be written to one. The selection of peripheral function A to H is done by writing to the Peripheral Multiplexing Odd and Even bits in the Peripheral Multiplexing register (PMUXn.PMUXE/O) in the PORT.

**Table 6-1. PORT Function Multiplexing for SAM C21 N**

| Pin | I/O Pin | Supply | A | | B | | | B[1][2] | | | C | D | E | F | G | H | I |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | EIC | REF | ADC0 | ADC1 | SDADC | AC | PTC | DAC | SERCOM | SERCOM-ALT | TC | TCC | COM | AC/GCLK | CCL |
| 1 | PA00 | VDDANA | EXTINT[0] | | | | | | | | | SERCOM1/PAD[0] | TC2/WO[0] | | | CMP[2] | |
| 2 | PA01 | VDDANA | EXTINT[1] | | | | | | | | | SERCOM1/PAD[1] | TC2/WO[1] | | | CMP[3] | |
| 3 | PC00 | VDDANA | EXTINT[8] | | AIN[8] | | | | | | | | | | | | |
| 4 | PC01 | VDDANA | EXTINT[9] | | AIN[9] | | | | | | | | | | | | |
| 5 | PC02 | VDDANA | EXTINT[10] | | AIN[10] | | | | | | | | | | | | |
| 6 | PC03 | VDDIO | EXTINT[11] | | AIN[11] | | | | | | SERCOM7/PAD[0] | | | TCC2/WO[0] | | | |
| 7 | PA02 | VDDANA | EXTINT[2] | | AIN[0] | | | AIN[4] | Y[0] | VOUT | | | | | | | |
| 8 | PA03 | VDDANA | EXTINT[3] | ADC/VREFA<br>DAC/VREFB | AIN[1] | | | | Y[1] | | | | | | | | |
| 9 | PB04 | VDDANA | EXTINT[4] | | | AIN[6] | | AIN[5] | Y[10] | | | | | | | | |
| 10 | PB05 | VDDANA | EXTINT[5] | | | AIN[7] | | AIN[6] | Y[11] | | | | | | | | |
| 13 | PB06 | VDDIO | EXTINT[6] | | | AIN[8] | INN[2] | AIN[7] | Y[12] | | SERCOM7/PAD[1] | | | | | | CCL2/IN[6] |
| 14 | PB07 | VDDIO | EXTINT[7] | | | AIN[9] | INP[2] | | Y[13] | | SERCOM7/PAD[3] | SERCOM7/PAD[2] | | | | | CCL2/IN[7] |
| 15 | PB08 | VDDIO | EXTINT[8] | | AIN[2] | AIN[4] | INN[1] | | Y[14] | | SERCOM7/PAD[2] | SERCOM7/PAD[3] | TC4/WO[0] | | | | CCL2/IN[8] |
| 16 | PB09 | VDDANA | EXTINT[9] | | AIN[3] | AIN[5] | INP[1] | | Y[15] | | | SERCOM4/PAD[1] | TC4/WO[1] | | | | CCL2/OUT[2] |
| 17 | PA04 | VDDANA | EXTINT[4] | SDADC/VREFB | AIN[4] | | | AIN[0] | Y[2] | | | SERCOM0/PAD[0] | TC0/WO[0] | | | | CCL0/IN[0] |
| 18 | PA05 | VDDANA | EXTINT[5] | | AIN[5] | | | AIN[1] | Y[3] | | | SERCOM0/PAD[1] | TC0/WO[1] | | | | CCL0/IN[1] |
| 19 | PA06 | VDDANA | EXTINT[6] | | AIN[6] | | INN[0] | AIN[2] | Y[4] | | | SERCOM0/PAD[2] | TC1/WO[0] | | | | CCL0/IN[2] |
| 20 | PA07 | VDDANA | EXTINT[7] | | AIN[7] | | INP[0] | AIN[3] | Y[5] | | | SERCOM0/PAD[3] | TC1/WO[1] | | | | CCL0/OUT[0] |
| 21 | PC05 | VDDANA | EXTINT[13] | | | | | | | | SERCOM6/PAD[3] | | | TCC2/WO[1] | | | |
| 22 | PC06 | VDDANA | EXTINT[14] | | | | | | | | SERCOM6/PAD[0] | | | | | | |
| 23 | PC07 | VDDANA | EXTINT[15] | | | | | | | | SERCOM6/PAD[1] | | | | | | |
| 26 | PA08 | VDDIO | NMI | | | AIN[10] | | | X[0]/Y[16] | | SERCOM0/PAD[0] | SERCOM2/PAD[0] | TC0/WO[0] | TCC0/WO[0] | | | CCL1/IN[3] |
| 27 | PA09 | VDDIO | EXTINT[9] | | | AIN[11] | | | X[1]/Y[17] | | SERCOM0/PAD[1] | SERCOM2/PAD[1] | TC0/WO[1] | TCC0/WO[1] | | | CCL1/IN[4] |
| 28 | PA10 | VDDIO | EXTINT[10] | | | | | | X[2]/Y[18] | | SERCOM0/PAD[2] | SERCOM2/PAD[2] | TC1/WO[0] | TCC0/WO[2] | | GCLK_IO[4] | CCL1/IN[5] |
| 29 | PA11 | VDDIO | EXTINT[11] | | | | | | X[3]/Y[19] | | SERCOM0/PAD[3] | SERCOM2/PAD[3] | TC1/WO[1] | TCC0/WO[3] | | GCLK_IO[5] | CCL1/OUT[1] |
| 30 | PB10 | VDDIO | EXTINT[10] | | | | | | | | | SERCOM4/PAD[2] | TC5/WO[0] | TCC0_WO4 | | GCLK_IO[4] | CCL1/IN[5] |
| 31 | PB11 | VDDIO | EXTINT[11] | | | | | | | | | SERCOM4/PAD[3] | TC5/WO[1] | TCC0_WO5 | | GCLK_IO[5] | CCL1/OUT[1] |
| 32 | PB12 | VDDIO | EXTINT[12] | | | | | | X[12]/Y[28] | | SERCOM4/PAD[0] | | TC4/WO[0] | TCC0_WO6 | CAN1/TX | GCLK_IO[6] | |
| 33 | PB13 | VDDIO | EXTINT[13] | | | | | | X[13]/Y[29] | | SERCOM4/PAD[1] | | TC4/WO[1] | TCC0_WO7 | CAN1/RX | GCLK_IO[7] | |
| 34 | PB14 | VDDIO | EXTINT[14] | | | | | | X[14]/Y[30] | | SERCOM4/PAD[2] | | TC5/WO[0] | | CAN1/TX | GCLK_IO[0] | CCL3/IN[9] |
| 35 | PB15 | VDDIO | EXTINT[15] | | | | | | X[15]/Y[31] | | SERCOM4/PAD[3] | | TC5/WO[1] | | CAN1/RX | GCLK_IO[1] | CCL3/IN[10] |
| 38 | PC08 | VDDIO | EXTINT[0] | | | | | | | | SERCOM6/PAD[0] | SERCOM7/PAD[0] | | | | | |
| 39 | PC09 | VDDIO | EXTINT[1] | | | | | | | | SERCOM6/PAD[1] | SERCOM7/PAD[1] | | | | | |
| 40 | PC10 | VDDIO | EXTINT[2] | | | | | | | | SERCOM6/PAD[2] | SERCOM7/PAD[2] | | | | | |
| 41 | PC11 | VDDIO | EXTINT[3] | | | | | | | | SERCOM6/PAD[3] | SERCOM7/PAD[3] | | | | | |
| 42 | PC12 | VDDIO | EXTINT[4] | | | | | | | | SERCOM7/PAD[0] | | | | | | |
| 43 | PC13 | VDDIO | EXTINT[5] | | | | | | | | SERCOM7/PAD[1] | | | | | | |
| 44 | PC14 | VDDIO | EXTINT[6] | | | | | | | | SERCOM7/PAD[2] | | | | | | |
| 45 | PC15 | VDDIO | EXTINT[7] | | | | | | | | SERCOM7/PAD[3] | | | | | | |
| 46 | PA12 | VDDIO | EXTINT[12] | | | | | | | | SERCOM2/PAD[0] | SERCOM4/PAD[0] | TC2/WO[0] | TCC0_WO6 | | CMP[0] | |
| 47 | PA13 | VDDIO | EXTINT[13] | | | | | | | | SERCOM2/PAD[1] | SERCOM4/PAD[1] | TC2/WO[1] | TCC0_WO7 | | CMP[1] | |
| 48 | PA14 | VDDIO | EXTINT[14] | | | | | | | | SERCOM2/PAD[2] | SERCOM4/PAD[2] | TC3/WO[0] | | | GCLK_IO[0] | |
| 49 | PA15 | VDDIO | EXTINT[15] | | | | | | | | SERCOM2/PAD[3] | SERCOM4/PAD[3] | TC3/WO[1] | | | GCLK_IO[1] | |
| 52 | PA16 | VDDIO | EXTINT[0] | | | | | | X[4]/Y[20] | | SERCOM1/PAD[0] | SERCOM3/PAD[0] | TC2/WO[0] | TCC1/WO[0] | | GCLK_IO[2] | CCL0/IN[0] |
| 53 | PA17 | VDDIO | EXTINT[1] | | | | | | X[5]/Y[21] | | SERCOM1/PAD[1] | SERCOM3/PAD[1] | TC2/WO[1] | TCC1/WO[1] | | GCLK_IO[3] | CCL0/IN[1] |
| 54 | PA18 | VDDIO | EXTINT[2] | | | | | | X[6]/Y[22] | | SERCOM1/PAD[2] | SERCOM3/PAD[2] | TC3/WO[0] | TCC1/WO[2] | | CMP[0] | CCL0/IN[2] |
| 55 | PA19 | VDDIO | EXTINT[3] | | | | | | X[7]/Y[23] | | SERCOM1/PAD[3] | SERCOM3/PAD[3] | TC3/WO[1] | TCC1/WO[3] | | CMP[1] | CCL0/OUT[0] |
| 56 | PC16 | VDDIO | EXTINT[8] | | | | | | | | SERCOM6/PAD[0] | | | | | | |
| 57 | PC17 | VDDIO | EXTINT[9] | | | | | | | | SERCOM6/PAD[1] | | | | | | |
| 58 | PC18 | VDDIO | EXTINT[10] | | | | | | | | SERCOM6/PAD[2] | | | | | | |

**Figure 7-2. Power Domain Overview, SAM C20/C21 N**




## 7.2 Power Supply Considerations

### 7.2.1 Power Supplies, SAM C21/SAM C20

The SAM C21 has the following power supply pins:

- VDDIO: Powers I/O lines and XOSC. Voltage is 2.70V to 5.50V.
- VDDIN: Powers I/O lines and the OSC48M, TOSC and internal regulator. Voltage is 2.70V to 5.50V.
- VDDANA: Powers I/O lines and the ADC, AC, DAC, PTC, SDADC, OSCULP32K, OSC32K, and XOSC32K. Voltage is 2.70V to 5.50V.
- VDDCORE: Internal regulated voltage output. Powers the core, memories, peripherals, and FDPLL96M. Voltage is 1.2V typical.

The same voltage must be applied to both the VDDIN and VDDANA pins. This common voltage is referred to as $V_{DD}$ in the datasheet. VDDIO must always be less than or equal to VDDIN.

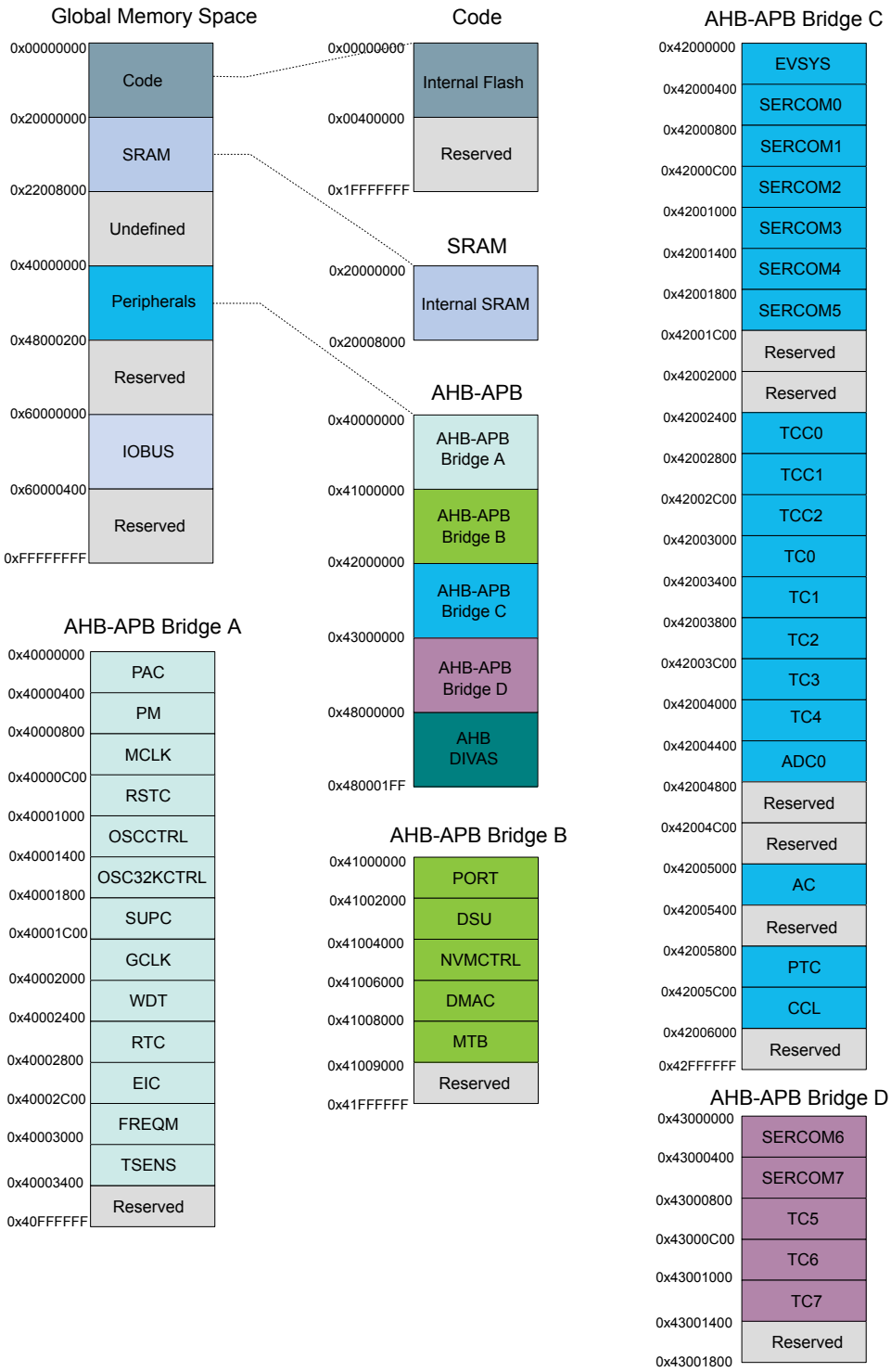
The ground pins, GND, are common to VDDCORE, VDDIO and VDDIN. The ground pin for VDDANA is GNDANA.

For decoupling recommendations for the different power supplies, refer to the schematic checklist.

The SAM C20 has the following power supply pins:

- VDDIO: Powers I/O lines and XOSC. Voltage is 2.70V to 5.50V.
- VDDIN: Powers I/O lines and the OSC48M, TOSC and internal regulator. Voltage is 2.70V to 5.50V.

**Figure 8-2. SAM C20 N Product Mapping**



cleared or locked at the user discretion. A set of Interrupt Flag and Status registers informs the user on the status of the violation in the peripherals. In addition, slaves bus errors can be also reported in the cases where reserved area is accessed by the application.

### 11.5.2 Basic Operation

#### 11.5.2.1 Initialization

After reset, the PAC is enabled.

#### 11.5.2.2 Initialization, Enabling and Resetting

The PAC is always enabled after reset.

Only a hardware reset will reset the PAC module.

#### 11.5.2.3 Operations

The PAC module allows the user to set, clear or lock the write protection status of all peripherals on all Peripheral Bridges.

If a peripheral register violation occurs, the Peripheral Interrupt Flag n registers (INTFLAGn) are updated to inform the user on the status of the violation in the peripherals connected to the Peripheral Bridge n (n = A,B,C ...). The corresponding Peripheral Write Control Status n register (STATUSn) gives the state of the write protection for all peripherals connected to the corresponding Peripheral Bridge n. Refer to the Peripheral Access Errors for details.

The PAC module also report the errors occurring at slave bus level when an access to reserved area is detected. AHB Slave Bus Interrupt Flag register (INTFLAGAHB) informs the user on the status of the violation in the corresponding slave. Refer to the AHB Slave Bus Errors for details.

#### 11.5.2.4 Peripheral Access Errors

The following events will generate a Peripheral Access Error:

- Protected write: To avoid unexpected writes to a peripheral's registers, each peripheral can be write protected. Only the registers denoted as “PAC Write-Protection” in the module’s datasheet can be protected. If a peripheral is not write protected, write data accesses are performed normally. If a peripheral is write protected and if a write access is attempted, data will not be written and peripheral returns an access error. The corresponding interrupt flag bit in the INTFLAGn register will be set.
- Illegal access: Access to an unimplemented register within the module.
- Synchronized write error: For write-synchronized registers an error will be reported if the register is written while a synchronization is ongoing.

When any of the INTFLAGn registers bit are set, an interrupt will be requested if the PAC interrupt enable bit is set.

#### 11.5.2.5 Write Access Protection Management

Peripheral access control can be enabled or disabled by writing to the WRCTRL register.

The data written to the WRCTRL register is composed of two fields; WRCTRL.PERID and WRCTRL.KEY. The WRCTRL.PERID is an unique identifier corresponding to a peripheral. The WRCTRL.KEY is a key value that defines the operation to be done on the control access bit. These operations can be “clear protection”, “set protection” and “set and lock protection bit”.

The “clear protection” operation will remove the write access protection for the peripheral selected by WRCTRL.PERID. Write accesses are allowed for the registers in this peripheral.

| Peripheral Name | Base Address | IRQ Line | AHB Clock | | APB Clock | | Generic Clock | PAC | | Events | | DMA | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Index | Enabled at Reset | Index | Enabled at Reset | Index | Index | Prot at Reset | User | Generator | Index | Sleep Walking |
| SERCOM7 | 0x43000400 | 10 | | | 1 | N | 42: CORE<br>18: SLOW | 1 | N | | | 51: RX<br>52: TX | Y |
| TC5 | 0x43000800 | 20 | | | 2 | N | 43 | 2 | N | 47: EVU | 87: OVF<br>88-89: MC0-1 | 53: OVF<br>54-55: MC0-1 | Y |
| TC6 | 0x43000C00 | 21 | | | 3 | N | 44 | 3 | N | 48:EVU | 90: OVF<br>91-92: MC0-1 | 56: OVF<br>57-58: MC0-1 | Y |
| TC7 | 0x43001000 | 22 | | | 4 | N | 45 | 4 | N | 49:EVU | 93: OVF<br>94-95: MC0-1 | 59: OVF<br>60-61: MC0-1 | Y |
| DIVAS | 0x48000000 | | 12 | Y | | | | | | | | | N/A |

**Table 12-2. Peripherals Configuration Summary SAM C20 N**

| Peripheral Name | Base Address | IRQ Line | AHB Clock | | APB Clock | | Generic Clock | PAC | | Events | | DMA | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Index | Enabled at Reset | Index | Enabled at Reset | Index | Index | Prot at Reset | User | Generator | Index | Sleep Walking |
| AHB-APB Bridge A | 0x40000000 | | 0 | Y | | | | | | | | | N/A |
| PAC | 0x40000000 | 0 | 10 | Y | 0 | Y | | 0 | N | | 85 : ACCERR | | N/A |
| PM | 0x40000400 | 0 | | | 1 | Y | | 1 | N | | | | N/A |
| MCLK | 0x40000800 | 0 | | | 2 | Y | | 2 | N | | | | Y |
| RSTC | 0x40000C00 | | | | 3 | Y | | 3 | N | | | | N/A |
| OSCCTRL | 0x40001000 | 0 | | | 4 | Y | 0: FDPLL96M clk source<br>1: FDPLL96M 32kHz | 4 | N | | 0: XOSC_FAIL | | Y |
| OSC32KCTRL | 0x40001400 | 0 | | | 5 | Y | | 5 | N | | 1: XOSC32K_FAIL | | Y |
| SUPC | 0x40001800 | 0 | | | 6 | Y | | 6 | N | | | | N/A |
| GCLK | 0x40001C00 | | | | 7 | Y | | 7 | N | | | | N/A |
| WDT | 0x40002000 | 1 | | | 8 | Y | | 8 | N | | | | Y |
| RTC | 0x40002400 | 2 | | | 9 | Y | | 9 | N | | 2: CMP0/ALARM0<br>3: CMP1<br>4: OVF5-1<br>5:12: PER0-7 | | Y |
| EIC | 0x40002800 | 3, NMI | | | 10 | Y | 2 | 10 | N | | 13-28: EXTINT0-15 | | Y |
| FREQM | 0x40002C00 | 4 | | | 11 | Y | 3: Measure<br>4: Reference | 11 | N | | | | N/A |
| AHB-APB Bridge B | 0x41000000 | | 1 | Y | | | | | | | | | N/A |
| PORT | 0x41000000 | | | | 0 | Y | | 0 | N | 1-4 : EV0-3 | | | Y |
| DSU | 0x41002000 | | 3 | Y | 1 | Y | | 1 | Y | | | | N/A |
| NVMCTRL | 0x41004000 | 6 | 5 | Y | 2 | Y | 39 | 2 | N | | | | Y |
| DMAC | 0x41006000 | 7 | 7 | Y | | | | 3 | N | 5-8: CH0-3 | 30-33: CH0-3 | | Y |
| MTB | 0x41008000 | | | | | | | | N | 45: START<br>46: STOP | | | N/A |
| AHB-APB Bridge C | 0x42000000 | | 2 | Y | | | | | | | | | N/A |
| EVSYS | 0x42000000 | 8 | | | 0 | N | 6-17: one per CHANNEL | 0 | N | | | | Y |

# 14. DIVAS – Divide and Square Root Accelerator

## 14.1 Overview

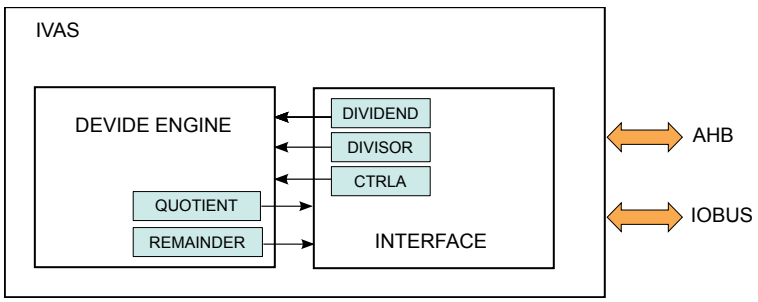
The Divide and Square Root Accelerator (DIVAS) is a programmable 32-bit signed or unsigned hardware divider and a 32-bit unsigned square root hardware engine. The DIVAS is connected to the high-speed bus matrix and may also be accessed using the low-latency CPU local bus (IOBUS; ARM® single-cycle I/O port). The DIVAS takes dividend and divisor values and returns the quotient and remainder when it is used as divider. The DIVAS takes unsigned input value and returns its square root and remainder when it is used as square root function.

## 14.2 Features

- Division accelerator for Cortex-M0+ systems
- 32-bit signed or unsigned integer division
- 32-bit unsigned square root
- 32-bit division in 2-16 cycles
- Programmable leading zero optimization
- Result includes quotient and remainder
- Result includes square root and remainder
- Busy and Divide-by-zero status
- Automatic start of operation when divisor or square root input is loaded

## 14.3 Block Diagram

**Figure 14-1. DIVAS Block Diagram**




## 14.4 Signal Description

Not applicable

## 14.5 Product Dependencies

In order to use this peripherial, other parts of the system must be configured correctly, as described below.

When the Run in Standby bit in the VREG register (VREG.RUNSTDBY) is written to '1', VDDCORE is supplied by the main voltage regulator. The VDDCORE level is set to the active mode voltage level.

**Related Links**

Sleep Mode Controller

### 22.6.2 Voltage Reference System Operation

The reference voltages are generated by a functional block DETREF inside of the SUPC. DETREF is providing a fixed-voltage source, BANDGAP=1V, and a variable voltage, INTREF.

#### 22.6.2.1 Initialization

The voltage reference output and the temperature sensor are disabled after any Reset.

#### 22.6.2.2 Enabling, Disabling, and Resetting

The voltage reference output is enabled/disabled by setting/clearing the Voltage Reference Output Enable bit in the Voltage Reference register (VREF.VREFOE).

The temperature sensor is enabled/disabled by setting/clearing the Temperature Sensor Enable bit in the Voltage Reference register (VREF.TSEN).

**Note:** When VREF.ONDEMAND=0, it is not recommended to enable both voltage reference output and temperature sensor at the same time - only the voltage reference output will be present at both ADC inputs.

#### 22.6.2.3 Selecting a Voltage Reference

The Voltage Reference Selection bit field in the VREF register (VREF.SEL) selects the voltage of INTREF to be applied to analog modules, e.g. the ADC.

#### 22.6.2.4 Sleep Mode Operation

The Voltage Reference output and the Temperature Sensor output behavior during sleep mode can be configured using the Run in Standby bit and the On Demand bit in the Voltage Reference register (VREF.RUNSTDBY, VREF.ONDEMAND), see the following table:

**Table 22-1. VREF Sleep Mode Operation**

| VREF.ONDEMAND | VREF.RUNSTDBY | Voltage Reference Sleep behavior |
|---|---|---|
| - | - | Disable |
| 0 | 0 | Always run in all sleep modes *except* standby sleep mode |
| 0 | 1 | Always run in all sleep modes *including* standby sleep mode |
| 1 | 0 | Only run if requested by the ADC, in all sleep modes *except* standby sleep mode |
| 1 | 1 | Only run if requested by the ADC, in all sleep modes *including* standby sleep mode |

### 22.6.3 Brown-Out Detectors

#### 22.6.3.1 Initialization

Before a Brown-Out Detector (BODVDD) is enabled, it must be configured, as outlined by the following:

- Set the BOD threshold level (BODVDD.LEVEL)
- Set the configuration in active, standby (BODVDD.ACTCDG, BODVDD.STDBYCFG)
- Set the prescaling value if the BOD will run in sampling mode (BODVDD.PSEL)
- Set the action and hysteresis (BODVDD.ACTION and BODVDD.HYST)

| Value | Description |
|---|---|
| 0 | BODVDD is disabled. |
| 1 | BODVDD is enabled. |

**Related Links**

Electrical Characteristics 85°C (SAM C20/C21 E/G/J)

NVM User Row Mapping

### 22.8.6 Voltage Regulator System (VREG) Control

**Name:** VREG
**Offset:** 0x18 [ID-00001e33]
**Reset:** 0x00000000
**Property:** PAC Write-Protection

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Access | R | R | R | R | R | R | R | R |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Access | R | R | R | R | R | R | R | R |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Access | R | R | R | R | R | R | R | R |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | | RUNSTDBY | | | | | ENABLE | |
| Access | R | R/W | R | R | R | R | R/W | R |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bit 6 – RUNSTDBY: Run in Standby**

| Value | Description |
|---|---|
| 0 | The voltage regulator is in low power mode in Standby sleep mode. |
| 1 | The voltage regulator is in normal mode in Standby sleep mode. |

**Bit 1 – ENABLE: Enable**

| Value | Description |
|---|---|
| 0 | The voltage regulator is disabled. |
| 1 | The voltage regulator is enabled. |

### 22.8.7 Voltage References System (VREF) Control

## 23.7 Register Summary

| Offset | Name | Bit Pos. | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x00 | CTRLA | 7:0 | ALWAYSON | | | | | WEN | ENABLE | |
| 0x01 | CONFIG | 7:0 | WINDOW[3:0] | | | | PER[3:0] | | | |
| 0x02 | EWCTRL | 7:0 | | | | | EWOFFSET[3:0] | | | |
| 0x03 | Reserved | | | | | | | | | |
| 0x04 | INTENCLR | 7:0 | | | | | | | | EW |
| 0x05 | INTENSET | 7:0 | | | | | | | | EW |
| 0x06 | INTFLAG | 7:0 | | | | | | | | EW |
| 0x07 | Reserved | | | | | | | | | |
| 0x08 | SYNCBUSY | 7:0 | | | | | | WEN | ENABLE | |
| 0x09 | | 15:8 | | | | | | | | |
| 0x0A | | 23:16 | | | | | | | | |
| 0x0B | | 31:24 | | | | | | | | |
| 0x0C | CLEAR | 7:0 | CLEAR[7:0] | | | | | | | |

## 23.8 Register Description

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16- and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly.

Some registers are optionally write-protected by the Peripheral Access Controller (PAC). Optional PAC write-protection is denoted by the "PAC Write-Protection" property in each individual register description. For details, refer to Register Access Protection.

Some registers are synchronized when read and/or written. Synchronization is denoted by the "Write-Synchronized" or the "Read-Synchronized" property in each individual register description. For details, refer to Synchronization.

Some registers are enable-protected, meaning they can only be written when the peripheral is disabled. Enable-protection is denoted by the "Enable-Protected" property in each individual register description.

### 23.8.1 Control A

**Name:** CTRLA
**Offset:** 0x00
**Reset:** X determined from NVM User Row
**Property:** PAC Write-Protection, Write-Synchronized

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | ALWAYSON | | | | | WEN | ENABLE | |
| Access | R/W | | | | | R/W | R/W | |
| Reset | x | | | | | x | x | |

**Bit 7 – ALWAYSON: Always-On**
This bit allows the WDT to run continuously. After being set, this bit cannot be written to '0', and the WDT will remain enabled until a power-on Reset is received. When this bit is '1', the Control A register

| Value | Description |
|---|---|
| 0 | The EIC is clocked by GCLK_EIC. |
| 1 | The EIC is clocked by CLK_ULP32K. |

**Bit 1 – ENABLE: Enable**
Due to synchronization there is a delay between writing to CTRLA.ENABLE until the peripheral is enabled/disabled. The value written to CTRLA.ENABLE will read back immediately and the Enable bit in the Synchronization Busy register will be set (SYNCBUSY.ENABLE=1). SYNCBUSY.ENABLE will be cleared when the operation is complete.

This bit is not Enable-Protected.

This bit is Write-Synchronized.

| Value | Description |
|---|---|
| 0 | The EIC is disabled. |
| 1 | The EIC is enabled. |

**Bit 0 – SWRST: Software Reset**
Writing a '0' to this bit has no effect.

Writing a '1' to this bit resets all registers in the EIC to their initial state, and the EIC will be disabled.

Writing a '1' to CTRLA.SWRST will always take precedence, meaning that all other writes in the same write operation will be discarded.

Due to synchronization there is a delay from writing CTRLA.SWRST until the Reset is complete. CTRLA.SWRST and SYNCBUSY.SWRST will both be cleared when the Reset is complete.

This bit is not Enable-Protected.

This bit is Write-Synchronized.

| Value | Description |
|---|---|
| 0 | There is no ongoing reset operation. |
| 1 | The reset operation is ongoing. |

### 26.8.2 Non-Maskable Interrupt Control

**Name:** NMICTRL
**Offset:** 0x01
**Reset:** 0x00
**Property:** PAC Write-Protection

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | | | | NMIASYNCH | NMIFILTEN | NMISENSE[2:0] | | |
| Access | | | | R/W | R/W | R/W | R/W | R/W |
| Reset | | | | 0 | 0 | 0 | 0 | 0 |

**Bit 4 – NMIASYNCH: Asynchronous Edge Detection Mode**
The NMI edge detection can be operated synchronously or asynchronously to the EIC clock.

| Value | Name | Description |
|---|---|---|
| 0x0 | SYNCHRONOUS | Synchronous path |
| 0x1 | RESYNCHRONIZED | Resynchronized path |
| 0x2 | ASYNCHRONOUS | Asynchronous path |
| 0x3 | - | Reserved |

**Bits 7:0 – EVGEN[7:0]: Event Generator**
These bits are used to choose the event generator to connect to the selected channel.

**Table 29-2. Event Generators**

| Value | Event Generator | Description |
|---|---|---|
| 0x00 | NONE | No event generator selected |
| 0x01 | OSCCTRL FAIL | XOSC Clock Failure |
| 0x02 | OSC32KCTRL FAIL | XOSC32K Clock Failure |
| 0x03 | RTC CMP0 | Compare 0 (mode 0 and 1) or Alarm 0 (mode 2) |
| 0x04 | RTC CMP1 | Compare 1 |
| 0x05 | RTC OVF | Overflow |
| 0x06 | RTC PER0 | Period 0 |
| 0x07 | RTC PER1 | Period 1 |
| 0x08 | RTC PER2 | Period 2 |
| 0x09 | RTC PER3 | Period 3 |
| 0x0A | RTC PER4 | Period 4 |
| 0x0B | RTC PER5 | Period 5 |
| 0x0C | RTC PER6 | Period 6 |
| 0x0D | RTC PER7 | Period 7 |
| 0x0E | EIC EXTINT0 | External Interrupt 0 |
| 0x0F | EIC EXTINT1 | External Interrupt 1 |
| 0x10 | EIC EXTINT2 | External Interrupt 2 |
| 0x11 | EIC EXTINT3 | External Interrupt 3 |
| 0x12 | EIC EXTINT4 | External Interrupt 4 |
| 0x13 | EIC EXTINT5 | External Interrupt 5 |
| 0x14 | EIC EXTINT6 | External Interrupt 6 |
| 0x15 | EIC EXTINT7 | External Interrupt 7 |
| 0x16 | EIC EXTINT8 | External Interrupt 8 |
| 0x17 | EIC EXTINT9 | External Interrupt 9 |
| 0x18 | EIC EXTINT10 | External Interrupt 10 |

**Bit 1 – TXC: Transmit Complete**
This flag is cleared by writing '1' to it or by writing new data to DATA.

In master mode, this flag is set when the data have been shifted out and there are no new data in DATA.

In slave mode, this flag is set when the _SS pin is pulled high. If address matching is enabled, this flag is only set if the transaction was initiated with an address match.

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the flag.

**Bit 0 – DRE: Data Register Empty**
This flag is cleared by writing new data to DATA.

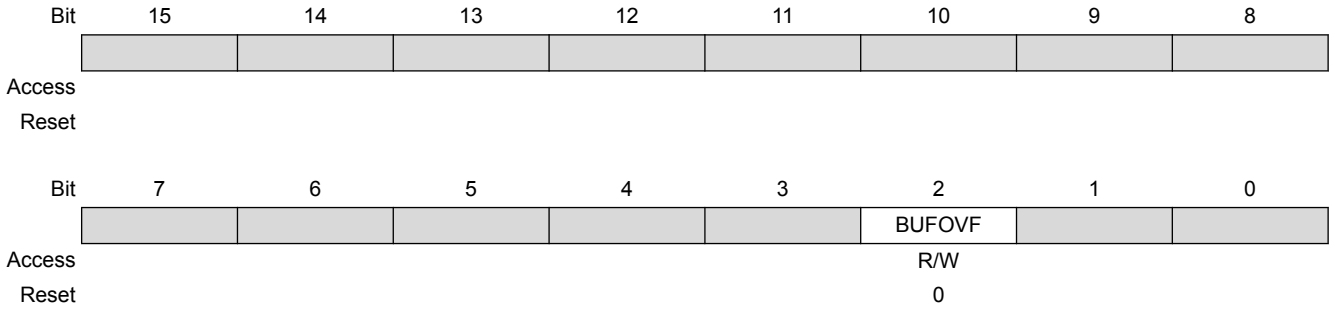
This flag is set when DATA is empty and ready for new data to transmit.

Writing '0' to this bit has no effect.

Writing '1' to this bit has no effect.

### 32.8.7 Status

**Name:** STATUS
**Offset:** 0x1A [ID-00000e74]
**Reset:** 0x0000
**Property:** –




**Bit 2 – BUFOVF: Buffer Overflow**
Reading this bit before reading DATA will indicate the error status of the next character to be read.

This bit is cleared by writing '1' to the bit or by disabling the receiver.

This bit is set when a buffer overflow condition is detected. See also CTRLA.IBON for overflow handling.

When set, the corresponding RxDATA will be zero.

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear it.

| Value | Description |
|---|---|
| 0 | No Buffer Overflow has occurred. |
| 1 | A Buffer Overflow has occurred. |

### 32.8.8 Synchronization Busy

This register allows the user to clear bits in the CTRLB register without doing a read-modify-write operation. Changes in this register will also be reflected in the Control B Set register (CTRLBSET).

**Name:** CTRLBCLR
**Offset:** 0x04
**Reset:** 0x00
**Property:** PAC Write-Protection, Read-Synchronized, Write-Synchronized

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | CMD[2:0] | | | | | ONESHOT | LUPD | DIR |
| Access | R/W | R/W | R/W | | | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | | | 0 | 0 | 0 |

**Bits 7:5 – CMD[2:0]: Command**
These bits are used for software control of the TC. The commands are executed on the next prescaled GCLK_TC clock cycle. When a command has been executed, the CMD bit group will be read back as zero.

Writing 0x0 to these bits has no effect.

Writing a '1' to any of these bits will clear the pending command.

**Bit 2 – ONESHOT: One-Shot on Counter**
This bit controls one-shot operation of the TC.

Writing a '0' to this bit has no effect

Writing a '1' to this bit will disable one-shot operation.

| Value | Description |
|---|---|
| 0 | The TC will wrap around and continue counting on an overflow/underflow condition. |
| 1 | The TC will wrap around and stop on the next underflow/overflow condition. |

**Bit 1 – LUPD: Lock Update**
This bit controls the update operation of the TC buffered registers.

When CTRLB.LUPD is set, no any update of the registers with value of its buffered register is performed on hardware UPDATE condition. Locking the update ensures that all buffer registers are valid before an hardware update is performed. After all the buffer registers are loaded correctly, the buffered registers can be unlocked.

This bit has no effect when input capture operation is enabled.

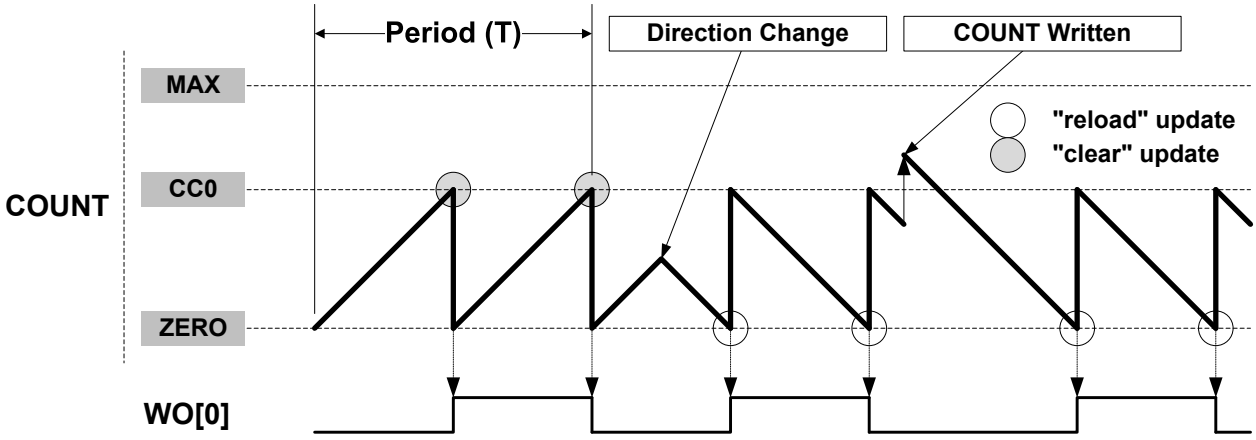
Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the LUPD bit.

| Value | Description |
|---|---|
| 0 | The CCBUFx and PERBUF buffer registers value are copied into CCx and PER registers on hardware update condition. |
| 1 | The CCBUFx and PERBUF buffer registers value are not copied into CCx and PER registers on hardware update condition. |

**Bit 0 – DIR: Counter Direction**
This bit is used to change the direction of the counter.

**Figure 36-5. Match Frequency Operation**



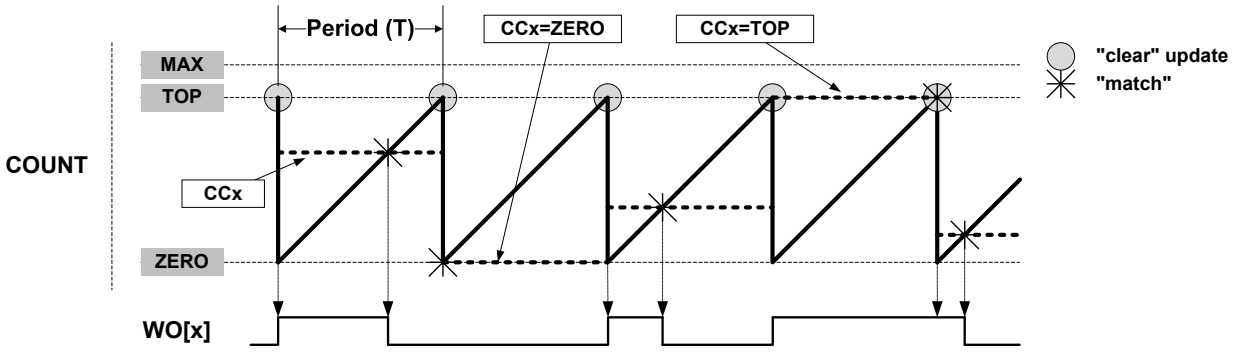

**Normal Pulse-Width Modulation (NPWM)**

NPWM uses single-slope PWM generation.

**Single-Slope PWM Operation**

For single-slope PWM generation, the period time (T) is controlled by Top value, and CCx controls the duty cycle of the generated waveform output. When up-counting, the WO[x] is set at start or compare match between the COUNT and TOP values, and cleared on compare match between COUNT and CCx register values. When down-counting, the WO[x] is cleared at start or compare match between the COUNT and ZERO values, and set on compare match between COUNT and CCx register values.

**Figure 36-6. Single-Slope PWM Operation**




The following equation calculates the exact resolution for a single-slope PWM ($R_{PWM\_SS}$) waveform:

$$R_{PWM\_SS} = \frac{\log(TOP+1)}{\log(2)}$$

The PWM frequency depends on the Period register value (PER) and the peripheral clock frequency ($f_{GCLK\_TCC}$), and can be calculated by the following equation:

$$f_{PWM\_SS} = \frac{f_{GCLK\_TCC}}{N(TOP+1)}$$

Where N represents the prescaler divider used (1, 2, 4, 8, 16, 64, 256, 1024).

**Dual-Slope PWM Generation**

For dual-slope PWM generation, the period setting (TOP) is controlled by PER, while CCx control the duty cycle of the generated waveform output. The figure below shows how the counter repeatedly counts from ZERO to PER and then from PER to ZERO. The waveform generator output is set on compare match when up-counting, and cleared on compare match when down-counting. An interrupt and/or event is generated on TOP (when counting upwards) and/or ZERO (when counting up or down).

| Value | Name | Description |
|---|---|---|
| 0x2 | FALL | Blanking applied from falling edge of the waveform output |
| 0x3 | BOTH | Blanking applied from each toggle of the waveform output |

**Bit 4 – QUAL: Recoverable Fault n Qualification**
Setting this bit enables the recoverable Fault n input qualification.

| Value | Description |
|---|---|
| 0 | The recoverable Fault n input is not disabled on CMPx value condition. |
| 1 | The recoverable Fault n input is disabled when output signal is at inactive level (CMPx == 0). |

**Bit 3 – KEEP: Recoverable Fault n Keep**
Setting this bit enables the Fault n keep action.

| Value | Description |
|---|---|
| 0 | The Fault n state is released as soon as the recoverable Fault n is released. |
| 1 | The Fault n state is released at the end of TCC cycle. |

**Bits 1:0 – SRC[1:0]: Recoverable Fault n Source**
These bits select the TCC event input for recoverable Fault n.

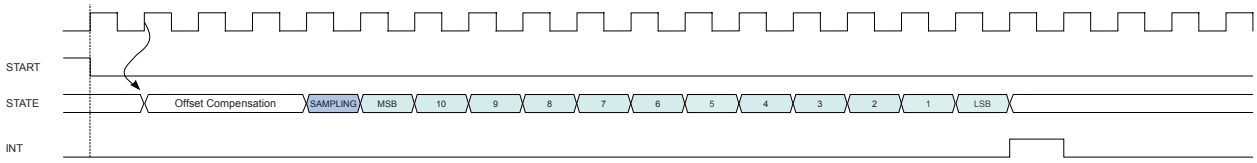
Event system channel connected to MCEx event input, must be configured to route the event asynchronously, when used as a recoverable Fault n input.

| Value | Name | Description |
|---|---|---|
| 0x0 | DISABLE | Fault input disabled |
| 0x1 | ENABLE | MCEx (x=0,1) event input |
| 0x2 | INVERT | Inverted MCEx (x=0,1) event input |
| 0x3 | ALTFAULT | Alternate fault (A or B) state at the end of the previous period. |

### 36.8.6 Waveform Extension Control

**Name:** WEXCTRL
**Offset:** 0x14 [ID-00002e48]
**Reset:** 0x00000000
**Property:** PAC Write-Protection, Enable-Protected

**Figure 38-5. ADC Timing for One Conversion with Offset Compensation, 12-bit**




The impact of resolution on the sampling rate is seen in the next two figures, where free-running sampling in 12-bit and 8-bit resolution are compared.

**Figure 38-6. ADC Timing for Free Running in 12-bit Resolution**

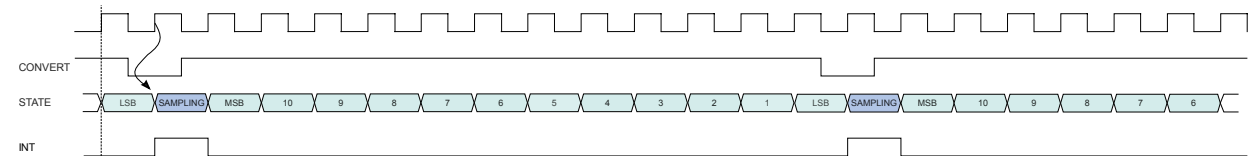
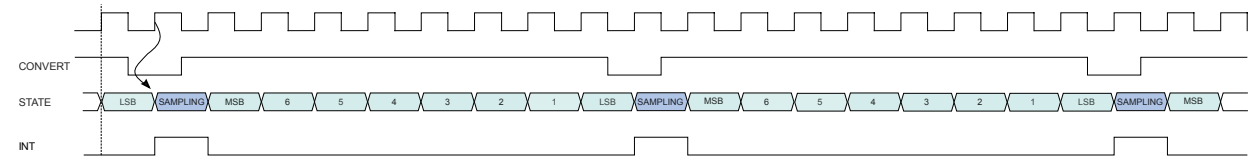



**Figure 38-7. ADC Timing for Free Running in 8-bit Resolution**




The propagation delay of an ADC measurement is given by:

$$\text{PropagationDelay} = \frac{1 + \text{Resolution}}{f_{\text{ADC}}}$$

> **Example.** In order to obtain 1MSPS in 12-bit resolution with a sampling time length of four CLK_ADC cycles, $f_{CLK\_ADC}$ must be 1MSPS * (4 + 12) = 16MHz. As the minimal division factor of the prescaler is 2, GCLK_ADC must be 32MHz.

#### 38.6.2.9 Accumulation

The result from multiple consecutive conversions can be accumulated. The number of samples to be accumulated is specified by the Sample Number field in the Average Control register (AVGCTRL.SAMPLENUM). When accumulating more than 16 samples, the result will be too large to match the 16-bit RESULT register size. To avoid overflow, the result is right shifted automatically to fit within the available register size. The number of automatic right shifts is specified in the table below.

**Note:** To perform the accumulation of two or more samples, the Conversion Result Resolution field in the Control C register (CTRLC.RESSEL) must be set.

**Table 38-1. Accumulation**

| Number of Accumulated Samples | AVGCTRL. SAMPLENUM | Number of Automatic Right Shifts | Final Result Precision | Automatic Division Factor |
|---|---|---|---|---|
| 1 | 0x0 | 0 | 12 bits | 0 |
| 2 | 0x1 | 0 | 13 bits | 0 |

- Result Ready (RESRDY): the request is set when a measurement result is available, and cleared when the VALUE register is read. The request is generated independent of any Window Monitor condition.

**Related Links**

DMAC – Direct Memory Access Controller

### 43.6.4 Interrupts

The TSENS has the following interrupt sources:

- Result Ready (RESRDY): Indicates when a measurement result is available.
- Window Monitor (WINMON): Generated when the measurement result matches the window monitor condition. Refer to CTRLC for details.
- Overrun (OVERRUN): Indicates that a new result is ready before the previous result has been read.
- Overflow (OVF): Indicates that the result is invalid because the result required more than 16 bits and overflowed the VALUE register.

Each interrupt source has an interrupt flag associated with it. The interrupt flag in the Interrupt Flag Status and Clear (INTFLAG) register is set when the interrupt condition occurs. Each interrupt can be individually enabled by writing a one to the corresponding bit in the Interrupt Enable Set (INTENSET) register, and disabled by writing a one to the corresponding bit in the Interrupt Enable Clear (INTENCLR) register. An interrupt request is generated when the interrupt flag is set and the corresponding interrupt is enabled. The interrupt request remains active until the interrupt flag is cleared, the interrupt is disabled, or the TSENS is reset. See INTFLAG for details on how to clear interrupt flags. All interrupt requests from the peripheral are ORed together on system level to generate one combined interrupt request to the NVIC. The user must read the INTFLAG register to determine which interrupt condition is present.

Note that interrupts must be globally enabled for interrupt requests to be generated.

**Related Links**

Nested Vector Interrupt Controller

### 43.6.5 Events

The TSENS can generate the following output event:

- Window Monitor (WINMON): Generated when the measurement results matches the window monitor condition. Refer to CTRLC for details.

Writing a one to an Event Output bit in the Event Control Register (EVCTRL.WINEO) enables the corresponding output event. Writing a zero to this bit disables the corresponding output event. Refer to the Event System chapter for details on configuring the event system.

The TSENS can take the following action on an input event:

- Start measurement (START): Start a measurement. Refer to CTRLB for details.

Writing a one to an Event Input bit into the Event Control register (EVCTRL.STARTEI) enables the corresponding action on input event. Writing a zero to this bit disables the corresponding action on input event. Refer to the Event System chapter for details. By default, the TSENS will detect a rising edge on the incoming event. If the TSENS action must be performed on the falling edge of the incoming event, the event line must be inverted first, by writing to one the corresponding Event Invert Enable bit in Event Control register (EVCTRL.STARTINV).

**Related Links**

EVSYS – Event System

Conditions for VDD: VDD<=4.9V.

If Vpin is lower than GND-0.6V, then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as R = |(GND-0.6V - $V_{PIN}$)/$I_{INJ2}$|. If Vpin is greater than VDD+0.6V, then a current limiting resistor is required. The positive DC injection current limiting resistor is calculated as R = ($V_{PIN}$-(VDD+0.6))/$I_{INJ2}$.

## 45.5 Supply Characteristics

The following characteristics are applicable to the operating temperature range: $T_A$ = -40°C to 105°C, unless otherwise specified and are valid for a junction temperature up to $T_J$ = 125°C.

**Table 45-4. Supply Characteristics**

| Symbol | Conditions | Voltage | | |
|---|---|---|---|---|
| | | Min. | Max. | Units |
| $V_{DDIO}$<br>$V_{DDIN}$<br>$V_{DDANA}$ | Full Voltage Range | 2.7 | 5.5 | V |

**Table 45-5. Supply Rise Rates**

| Symbol | Parameter | Fall Rate | Rise Rate | Units |
|---|---|---|---|---|
| | | Max | Max. | |
| $V_{DDIO}$ | DC supply peripheral I/Os, internal regulator and analog supply | 0.05 | 0.1 | V/µs |
| $V_{DDIN}$ | | 0.05 | 0.1 | |
| $V_{DDANA}$ | | 0.05 | 0.1 | |

**Table 45-6. Power Supply Current Requirement**

| Symbol | Conditions | Current | Units |
|---|---|---|---|
| | | Max | |
| $I_{INPUT}$(1) | Power up Maximum current | 1.9 | mA |

1. $I_{INPUT}$ is the minimum requirement for the power supply connected to the device.

**Related Links**

Power Supply and Start-Up Considerations

## 45.6 Maximum Clock Frequencies

**Table 45-7. Maximum GCLK Generator Output Frequencies**

| Symbol | Condition | Max. | Units |
|---|---|---|---|
| $f_{GCLKGEN0}$ / $f_{GCLK\_MAIN}$ | Undivided | 96 | MHz |
| $f_{GCLKGEN1}$ | | | |
| $f_{GCLKGEN2}$ | | | |

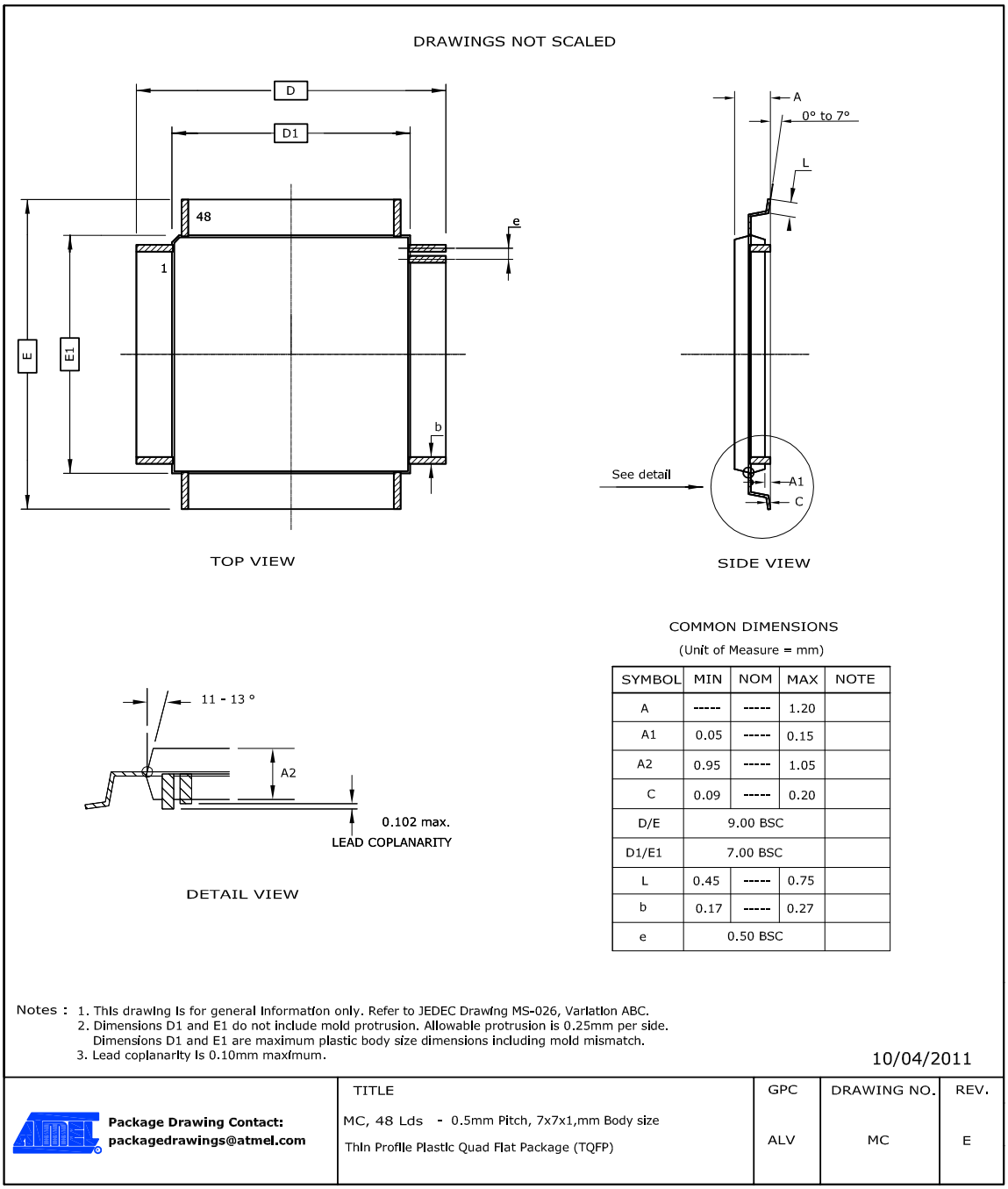
**Table 48-12. Package Characteristics**

| | |
|---|---|
| Moisture Sensitivity Level | MSL1 |

**Table 48-13. Package Reference**

| | |
|---|---|
| JEDEC Drawing Reference | N/A |
| JESD97 Classification | e1 |

### 48.2.5 48 pin TQFP




COMMON DIMENSIONS

(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | ----- | ----- | 1.20 | |
| A1 | 0.05 | ----- | 0.15 | |
| A2 | 0.95 | ----- | 1.05 | |
| C | 0.09 | ----- | 0.20 | |
| D/E | 9.00 BSC | | | |
| D1/E1 | 7.00 BSC | | | |
| L | 0.45 | ----- | 0.75 | |
| b | 0.17 | ----- | 0.27 | |
| e | 0.50 BSC | | | |

Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MS-026, Variation ABC.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

10/04/2011

| | TITLE | GPC | DRAWING NO. | REV. |
|---|---|---|---|---|
| Package Drawing Contact: packagedrawings@atmel.com | MC, 48 Lds - 0.5mm Pitch, 7x7x1,mm Body size<br>Thin Profile Plastic Quad Flat Package (TQFP) | ALV | MC | E |