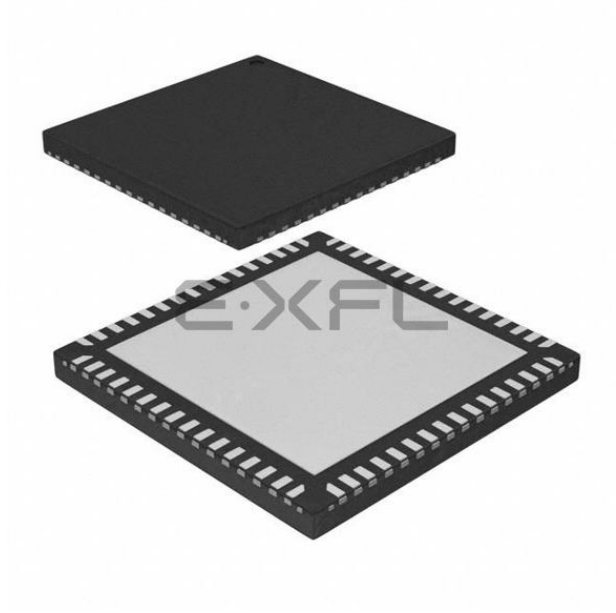

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, WDT
Number of I/O	52
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamc20j17a-mnt

1. Use the SAM C21J pinout muxing for the WLCSP56 package.
2. All analog pin functions are on peripheral function B. Peripheral function B must be selected to disable the digital control of the pin.
3. Only some pins can be used in SERCOM I2C mode. Refer to SERCOM I2C Pins.
4. SERCOM4 and SERCOM5 are not supported on SAM C21E.

Table 6-3. PORT Function Multiplexing for SAM C20 N

Pin	I/O Pin	Supply	A		B	B[1][2]		C	D	E	F	G	H	I
			EIC	REF	ADC0	AC	PTC	SERCOM	SERCOM-ALT	TC	TCC	COM	AC/GCLK	CCL
1	PA00	VDDANA	EXTINT[0]						SERCOM1/PAD[0]	TC2/WO[0]			CMP[2]	
2	PA01	VDDANA	EXTINT[1]						SERCOM1/PAD[1]	TC2/WO[1]			CMP[3]	
3	PC00	VDDANA	EXTINT[8]		AIN[8]									
4	PC01	VDDANA	EXTINT[9]		AIN[9]									
5	PC02	VDDANA	EXTINT[10]		AIN[10]									
6	PC03	VDDIO	EXTINT[11]		AIN[11]			SERCOM7/PAD[0]			TCC2/WO[0]			
7	PA02	VDDANA	EXTINT[2]		AIN[0]	AIN[4]	Y[0]							
8	PA03	VDDANA	EXTINT[3]	ADC/VREFA	AIN[1]		Y[1]							
9	PB04	VDDANA	EXTINT[4]			AIN[5]	Y[10]							
10	PB05	VDDANA	EXTINT[5]			AIN[6]	Y[11]							
13	PB06	VDDIO	EXTINT[6]			AIN[7]	Y[12]	SERCOM7/PAD[1]						CCL2/IN[6]
14	PB07	VDDIO	EXTINT[7]				Y[13]	SERCOM7/PAD[3]	SERCOM7/PAD[2]					CCL2/IN[7]
15	PB08	VDDIO	EXTINT[8]		AIN[2]		Y[14]	SERCOM7/PAD[2]	SERCOM7/PAD[3]	TC4/WO[0]				CCL2/IN[8]
16	PB09	VDDANA	EXTINT[9]		AIN[3]		Y[15]		SERCOM4/PAD[1]	TC4/WO[1]				CCL2/OUT[2]
17	PA04	VDDANA	EXTINT[4]		AIN[4]	AIN[0]	Y[2]		SERCOM0/PAD[0]	TC0/WO[0]				CCL0/IN[0]
18	PA05	VDDANA	EXTINT[5]		AIN[5]	AIN[1]	Y[3]		SERCOM0/PAD[1]	TC0/WO[1]				CCL0/IN[1]
19	PA06	VDDANA	EXTINT[6]		AIN[6]	AIN[2]	Y[4]		SERCOM0/PAD[2]	TC1/WO[0]				CCL0/IN[2]
20	PA07	VDDANA	EXTINT[7]		AIN[7]	AIN[3]	Y[5]		SERCOM0/PAD[3]	TC1/WO[1]				CCL0/OUT[0]
21	PC05	VDDANA	EXTINT[13]					SERCOM6/PAD[3]			TCC2/WO[1]			
22	PC06	VDDANA	EXTINT[14]					SERCOM6/PAD[0]						
23	PC07	VDDANA	EXTINT[15]					SERCOM6/PAD[1]						
26	PA08	VDDIO	NMI				X[0]/Y[16]	SERCOM0/PAD[0]	SERCOM2/PAD[0]	TC0/WO[0]	TCC0/WO[0]			CCL1/IN[3]
27	PA09	VDDIO	EXTINT[9]				X[1]/Y[17]	SERCOM0/PAD[1]	SERCOM2/PAD[1]	TC0/WO[1]	TCC0/WO[1]			CCL1/IN[4]
28	PA10	VDDIO	EXTINT[10]				X[2]/Y[18]	SERCOM0/PAD[2]	SERCOM2/PAD[2]	TC1/WO[0]	TCC0/WO[2]		GCLK_IO[4]	CCL1/IN[5]
29	PA11	VDDIO	EXTINT[11]				X[3]/Y[19]	SERCOM0/PAD[3]	SERCOM2/PAD[3]	TC1/WO[1]	TCC0/WO[3]		GCLK_IO[5]	CCL1/OUT[1]
30	PB10	VDDIO	EXTINT[10]						SERCOM4/PAD[2]	TC5/WO[0]	TCC0_WO4		GCLK_IO[4]	CCL1/IN[5]
31	PB11	VDDIO	EXTINT[11]						SERCOM4/PAD[3]	TC5/WO[1]	TCC0_WO5		GCLK_IO[5]	CCL1/OUT[1]
32	PB12	VDDIO	EXTINT[12]				X[12]/Y[28]	SERCOM4/PAD[0]		TC4/WO[0]	TCC0_WO6		GCLK_IO[6]	
33	PB13	VDDIO	EXTINT[13]				X[13]/Y[29]	SERCOM4/PAD[1]		TC4/WO[1]	TCC0_WO7		GCLK_IO[7]	
34	PB14	VDDIO	EXTINT[14]				X[14]/Y[30]	SERCOM4/PAD[2]		TC5/WO[0]			GCLK_IO[0]	CCL3/IN[9]
35	PB15	VDDIO	EXTINT[15]				X[15]/Y[31]	SERCOM4/PAD[3]		TC5/WO[1]			GCLK_IO[1]	CCL3/IN[10]
38	PC08	VDDIO	EXTINT[0]					SERCOM6/PAD[0]	SERCOM7/PAD[0]					
39	PC09	VDDIO	EXTINT[1]					SERCOM6/PAD[1]	SERCOM7/PAD[1]					
40	PC10	VDDIO	EXTINT[2]					SERCOM6/PAD[2]	SERCOM7/PAD[2]					
41	PC11	VDDIO	EXTINT[3]					SERCOM6/PAD[3]	SERCOM7/PAD[3]					
42	PC12	VDDIO	EXTINT[4]					SERCOM7/PAD[0]						
43	PC13	VDDIO	EXTINT[5]					SERCOM7/PAD[1]						
44	PC14	VDDIO	EXTINT[6]					SERCOM7/PAD[2]						
45	PC15	VDDIO	EXTINT[7]					SERCOM7/PAD[3]						
46	PA12	VDDIO	EXTINT[12]					SERCOM2/PAD[0]	SERCOM4/PAD[0]	TC2/WO[0]	TCC0_WO6		CMP[0]	
47	PA13	VDDIO	EXTINT[13]					SERCOM2/PAD[1]	SERCOM4/PAD[1]	TC2/WO[1]	TCC0_WO7		CMP[1]	
48	PA14	VDDIO	EXTINT[14]					SERCOM2/PAD[2]	SERCOM4/PAD[2]	TC3/WO[0]			GCLK_IO[0]	
49	PA15	VDDIO	EXTINT[15]					SERCOM2/PAD[3]	SERCOM4/PAD[3]	TC3/WO[1]			GCLK_IO[1]	
52	PA16	VDDIO	EXTINT[0]				X[4]/Y[20]	SERCOM1/PAD[0]	SERCOM3/PAD[0]	TC2/WO[0]	TCC1/WO[0]		GCLK_IO[2]	CCL0/IN[0]
53	PA17	VDDIO	EXTINT[1]				X[5]/Y[21]	SERCOM1/PAD[1]	SERCOM3/PAD[1]	TC2/WO[1]	TCC1/WO[1]		GCLK_IO[3]	CCL0/IN[1]
54	PA18	VDDIO	EXTINT[2]				X[6]/Y[22]	SERCOM1/PAD[2]	SERCOM3/PAD[2]	TC3/WO[0]	TCC1/WO[2]		CMP[0]	CCL0/IN[2]
55	PA19	VDDIO	EXTINT[3]				X[7]/Y[23]	SERCOM1/PAD[3]	SERCOM3/PAD[3]	TC3/WO[1]	TCC1/WO[3]		CMP[1]	CCL0/OUT[0]
56	PC16	VDDIO	EXTINT[8]					SERCOM6/PAD[0]						
57	PC17	VDDIO	EXTINT[9]					SERCOM6/PAD[1]						
58	PC18	VDDIO	EXTINT[10]					SERCOM6/PAD[2]						
59	PC19	VDDIO	EXTINT[11]					SERCOM6/PAD[3]						
60	PC20	VDDIO	EXTINT[12]											CCL3/IN[9]
61	PC21	VDDIO	EXTINT[13]											CCL3/IN[10]
64	PB16	VDDIO	EXTINT[0]					SERCOM5/PAD[0]		TC6/WO[0]			GCLK_IO[2]	CCL3/IN[11]
65	PB17	VDDIO	EXTINT[1]					SERCOM5/PAD[1]		TC6/WO[1]			GCLK_IO[3]	CCL3/OUT[3]
66	PB18	VDDIO	EXTINT[2]					SERCOM5/PAD[2]	SERCOM3/PAD[2]				GCLK_IO[4]	
67	PB19	VDDIO	EXTINT[3]					SERCOM5/PAD[3]	SERCOM3/PAD[3]				GCLK_IO[5]	
68	PB20	VDDIO	EXTINT[4]					SERCOM3/PAD[0]	SERCOM2/PAD[0]				GCLK_IO[6]	
69	PB21	VDDIO	EXTINT[5]					SERCOM3/PAD[1]	SERCOM2/PAD[1]				GCLK_IO[7]	
70	PA20	VDDIO	EXTINT[4]				X[8]/Y[24]	SERCOM5/PAD[2]	SERCOM3/PAD[2]	TC7/WO[0]	TCC2/WO[0]		GCLK_IO[4]	

Table 9-3. SAM C20/C21 RWW Section Parameters(1)

Device	Flash size (FLASH_PM)	Number of pages (FLASH_P)	Page size (FLASH_W)
x18	8Kbytes	128	64 bytes
x17	4Kbytes	64	64 bytes
x16	2Kbytes	32	64 bytes
x15	1Kbytes	16	64 bytes

Note: 1. x = SAM C20/C21 G/J/E/N. The N-series (100-pin devices) does not include x16 and x15 option.

9.3 NVM User Row Mapping

The first two 32-bit words of the NVM User Row contains calibration data that are automatically read at device power on.

The NVM User Row can be read at address 0x804000.

To write the NVM User Row, refer to the NVMCTRL - Non-Volatile Memory Controller.

Note that when writing to the user row the values do not get loaded by the other modules on the device until a device reset occurs.

Table 9-4. NVM User Row Mapping

Bit Position	Name	Usage	Production setting	Related Peripheral Register
2:0	BOOTPROT	Used to select one of eight different bootloader sizes.	7	NVMCTRL
3	Reserved	-	1	-
6:4	EEPROM	Used to select one of eight different EEPROM sizes.	7	NVMCTRL
7	Reserved	-	1	-
13:8	BODVDD Level	BODVDD Threshold Level at power on.	8	SUPC.BODVDD
14	BODVDD Disable	BODVDD Disable at power on.	0	SUPC.BODVDD
16:15	BODVDD Action	BODVDD Action at power on.	1	SUPC.BODVDD
25:17	Reserved	Voltage Regulator Internal BOD (BODCORE) configuration. These bits are written in production and must not be changed.	0xA8	-
26	WDT Enable	WDT Enable at power on.	0	WDT.CTRLA
27	WDT Always-On	WDT Always-On at power on.	0	WDT.CTRLA
31:28	WDT Period	WDT Period at power on.	0xB	WDT.CONFIG

Peripheral Name	Base Address	IRQ Line	AHB Clock		APB Clock		Generic Clock	PAC		Events		DMA	
			Index	Enabled at Reset	Index	Enabled at Reset	Index	Index	Prot at Reset	User	Generator	Index	Sleep Walking
DAC	0x42005400	28			21	N	36	21	N	38: START	78: EMPTY	45: EMPTY	Y
PTC	0x42005800	30			22	N	37	22	N	39: STCONV	79: EOC 80: WCOMP	EOC: 46 WCOMP: 47 SEQ: 48	
CCL	0x42005C00				23	N	38	23	N	40-43 : LUTIN0-3	781-84: LUTOUT0-3		Y
DIVAS	0x48000000		12	Y									N/A

Table 12-4. Peripherals Configuration Summary SAM C20 E/G/J

Peripheral Name	Base Address	IRQ Line	AHB Clock		APB Clock		Generic Clock	PAC		Events		DMA	
			Index	Enabled at Reset	Index	Enabled at Reset	Index	Index	Prot at Reset	User	Generator	Index	Sleep Walking
AHB-APB Bridge A	0x40000000		0	Y									N/A
PAC	0x44000000	0	10	Y	0	Y		0	N		85 : ACCERR		N/A
PM	0x40000400	0			1	Y		1	N				N/A
MCLK	0x40000800	0			2	Y		2	N				Y
RSTC	0x40000C00				3	Y		3	N				N/A
OSCCTRL	0x40001000	0			4	Y	0: FDPLL96M clk source 1: FDPLL96M 32kHz	4	N		0: XOSC_FAIL		Y
OSC32KCTRL	0x40001400	0			5	Y		5	N		1: XOSC32K_FAIL		Y
SUPC	0x40001800	0			6	Y		6	N				N/A
GCLK	0x40001C00				7	Y		7	N				N/A
WDT	0x40002000	1			8	Y		8	N				Y
RTC	0x40002400	2			9	Y		9	N		2: CMP0/ALARM0 3: CMP1 4: OVF 5-12: PER0-7		Y
EIC	0x40002800	3, NMI			10	Y	2	10	N		13-28: EXTINT0-15		Y
FREQM	0x40002C00	4			11	Y	3: Measure 4: Reference	11	N				N/A
AHB-APB Bridge B	0x41000000		1	Y									N/A
PORT	0x41000000				0	Y		0	N	1-4 : EV0-3			Y
DSU	0x41002000		3	Y	1	Y		1	Y				N/A
NVMCTRL	0x41004000	6	5	Y	2	Y	39	2	N				Y
DMAC	0x41006000	7	7	Y				3	N	5-8: CH0-3	30-33: CH0-3		Y
MTB	0x41008000								N	44: START 45: STOP			N/A
AHB-APB Bridge C	0x42000000		2	Y									N/A
EVSYS	0x42000000	8			0	N	6-17: one per CHANNEL	0	N				Y
SERCOM0	0x42000400	9			1	N	19: CORE 18: SLOW	1	N			2: RX 3: TX	Y
SERCOM1	0x42000800	10			2	N	20: CORE 18: SLOW	2	N			4: RX 5: TX	Y
SERCOM2	0x42000C00	11			3	N	21: CORE 18: SLOW	3	N			6: RX 7: TX	Y

Bit	31	30	29	28	27	26	25	24
	ADDOFF[19:12]							
Access	R	R	R	R	R	R	R	R
Reset	x	x	x	x	x	x	x	x

Bit	23	22	21	20	19	18	17	16
	ADDOFF[11:4]							
Access	R	R	R	R	R	R	R	R
Reset	x	x	x	x	x	x	x	x

Bit	15	14	13	12	11	10	9	8
	ADDOFF[3:0]							
Access	R	R	R	R				
Reset	x	x	x	x				

Bit	7	6	5	4	3	2	1	0
							FMT	EPRES
Access							R	R
Reset							1	x

Bits 31:12 – ADDOFF[19:0]: Address Offset
The base address of the component, relative to the base address of this ROM table.

Bit 1 – FMT: Format
Always read as '1', indicating a 32-bit ROM table.

Bit 0 – EPRES: Entry Present
This bit indicates whether an entry is present at this location in the ROM table.

This bit is set at power-up if the device is not protected indicating that the entry is not present.

This bit is cleared at power-up if the device is not protected indicating that the entry is present.

13.13.12 CoreSight ROM Table End

Name: END
Offset: 0x1008
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
	END[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	END[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	END[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	END[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – END[31:0]: End Marker
Indicates the end of the CoreSight ROM table entries.

13.13.13 CoreSight ROM Table Memory Type

Name: MEMTYPE
Offset: 0x1FCC
Reset: 0x0000000x
Property: -

Offset	Name	Bit Pos.								
0xD8	PCHCTRL22	7:0	WRTLOCK	CHEN			GEN[3:0]			
0xD9		15:8								
0xDA		23:16								
0xDB		31:24								
0xDC	PCHCTRL23	7:0	WRTLOCK	CHEN			GEN[3:0]			
0xDD		15:8								
0xDE		23:16								
0xDF		31:24								
0xE0	PCHCTRL24	7:0	WRTLOCK	CHEN			GEN[3:0]			
0xE1		15:8								
0xE2		23:16								
0xE3		31:24								
0xE4	PCHCTRL25	7:0	WRTLOCK	CHEN			GEN[3:0]			
0xE5		15:8								
0xE6		23:16								
0xE7		31:24								
0xE8	PCHCTRL26	7:0	WRTLOCK	CHEN			GEN[3:0]			
0xE9		15:8								
0xEA		23:16								
0xEB		31:24								
0xEC	PCHCTRL27	7:0	WRTLOCK	CHEN			GEN[3:0]			
0xED		15:8								
0xEE		23:16								
0xEF		31:24								
0xF0	PCHCTRL28	7:0	WRTLOCK	CHEN			GEN[3:0]			
0xF1		15:8								
0xF2		23:16								
0xF3		31:24								
0xF4	PCHCTRL29	7:0	WRTLOCK	CHEN			GEN[3:0]			
0xF5		15:8								
0xF6		23:16								
0xF7		31:24								
0xF8	PCHCTRL30	7:0	WRTLOCK	CHEN			GEN[3:0]			
0xF9		15:8								
0xFA		23:16								
0xFB		31:24								
0xFC	PCHCTRL31	7:0	WRTLOCK	CHEN			GEN[3:0]			
0xFD		15:8								
0xFE		23:16								
0xFF		31:24								
0x0100	PCHCTRL32	7:0	WRTLOCK	CHEN			GEN[3:0]			
0x0101		15:8								
0x0102		23:16								
0x0103		31:24								
0x0104	PCHCTRL33	7:0	WRTLOCK	CHEN			GEN[3:0]			
0x0105		15:8								
0x0106		23:16								

Bit 2 – TC5: TC5 APBd Mask Clock Enable

Value	Description
0	The APBD clock for the TC5 is stopped.
1	The APBD clock for the TC5 is enabled.

Bit 1 – SERCOM7: SERCOM7 APBD Mask Clock Enable

Value	Description
0	The APBD clock for the SERCOM7 is stopped.
1	The APBD clock for the SERCOM7 is enabled.

Bit 0 – SERCOM6: SERCOM6 APBD Mask Clock Enable

Value	Description
0	The APBD clock for the SERCOM6 is stopped.
1	The APBD clock for the SERCOM6 is enabled.

Bit 0 – BODVDDRDY: BODVDD Ready Interrupt Enable
Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the BODVDD Ready Interrupt Enable bit, which disables the BODVDD Ready interrupt.

Value	Description
0	The BODVDD Ready interrupt is disabled.
1	The BODVDD Ready interrupt is enabled, and an interrupt request will be generated when the BODVDD Ready Interrupt flag is set.

22.8.2 Interrupt Enable Set

This register allows the user to disable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Clear register (INTENCLR).

Name: INTENSET
Offset: 0x04 [ID-00001e33]
Reset: 0x00000000
Property: PAC Write-Protection

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
						BVDDSRDY	BODVDDDET	BODVDDRDY
Access						R/W	R/W	R/W
Reset						0	0	0

Bit 2 – BVDDSRDY: BODVDD Synchronization Ready Interrupt Enable
Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the BODVDD Synchronization Ready Interrupt Enable bit, which enables the BODVDD Synchronization Ready interrupt.

Value	Description
0	The BODVDD Synchronization Ready interrupt is disabled.
1	The BODVDD Synchronization Ready interrupt is enabled, and an interrupt request will be generated when the BODVDD Synchronization Ready Interrupt flag is set.

23.6.2.4 Normal Mode

In Normal mode operation, the length of a time-out period is configured in CONFIG.PER. The WDT is enabled by writing a '1' to the Enable bit in the Control A register (CTRLA.ENABLE). Once enabled, the WDT will issue a system reset if a time-out occurs. This can be prevented by clearing the WDT at any time during the time-out period.

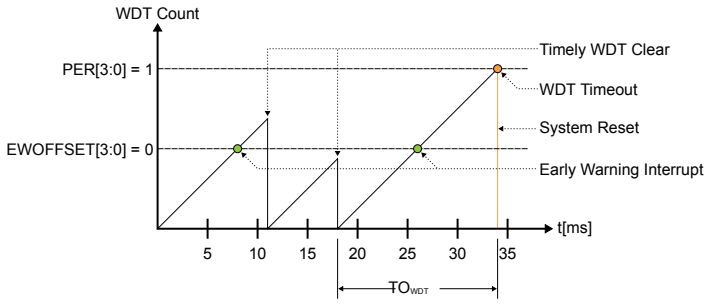
The WDT is cleared and a new WDT time-out period is started by writing 0xA5 to the Clear register (CLEAR). Writing any other value than 0xA5 to CLEAR will issue an immediate system reset.

There are 12 possible WDT time-out (TO_{WDT}) periods, selectable from 8ms to 16s.

By default, the early warning interrupt is disabled. If it is desired, the Early Warning Interrupt Enable bit in the Interrupt Enable register (INTENSET.EW) must be written to '1'. The Early Warning Interrupt is disabled again by writing a '1' to the Early Warning Interrupt bit in the Interrupt Enable Clear register (INTENCLR.EW).

If the Early Warning Interrupt is enabled, an interrupt is generated prior to a WDT time-out condition. In Normal mode, the Early Warning Offset bits in the Early Warning Interrupt Control register, EWCTRL.EWOFFSET, define the time when the early warning interrupt occurs. The Normal mode operation is illustrated in the figure Normal-Mode Operation.

Figure 23-2. Normal-Mode Operation



23.6.2.5 Window Mode

In Window mode operation, the WDT uses two different time specifications: the WDT can only be cleared by writing 0xA5 to the CLEAR register *after* the closed window time-out period (TO_{WDTW}), during the subsequent Normal time-out period (TO_{WDT}). If the WDT is cleared before the time window opens (before TO_{WDTW} is over), the WDT will issue a system reset.

Both parameters TO_{WDTW} and TO_{WDT} are periods in a range from 8ms to 16s, so the total duration of the WDT time-out period is the sum of the two parameters.

The closed window period is defined by the Window Period bits in the Configuration register (CONFIG.WINDOW), and the open window period is defined by the Period bits in the Configuration register (CONFIG.PER).

By default, the Early Warning interrupt is disabled. If it is desired, the Early Warning Interrupt Enable bit in the Interrupt Enable register (INTENSET.EW) must be written to '1'. The Early Warning Interrupt is disabled again by writing a '1' to the Early Warning Interrupt bit in the Interrupt Enable Clear (INTENCLR.EW) register.

If the Early Warning interrupt is enabled in Window mode, the interrupt is generated at the start of the open window period, i.e. after TO_{WDTW}. The Window mode operation is illustrated in figure Window-Mode Operation.

Bit 3 – COUNT: Count Value Synchronization Busy Status

Value	Description
0	Read/write synchronization for COUNT register is complete.
1	Read/write synchronization for COUNT register is ongoing.

Bit 2 – FREQCORR: Frequency Correction Synchronization Busy Status

Value	Description
0	Write synchronization for FREQCORR register is complete.
1	Write synchronization for FREQCORR register is ongoing.

Bit 1 – ENABLE: Enable Synchronization Busy Status

Value	Description
0	Write synchronization for CTRLA.ENABLE bit is complete.
1	Write synchronization for CTRLA.ENABLE bit is ongoing.

Bit 0 – SWRST: Software Reset Synchronization Busy Status

Value	Description
0	Write synchronization for CTRLA.SWRST bit is complete.
1	Write synchronization for CTRLA.SWRST bit is ongoing.

24.10.8 Frequency Correction

Name: FREQCORR
Offset: 0x14
Reset: 0x00
Property: PAC Write-Protection, Write-Synchronized

Bit	7	6	5	4	3	2	1	0
	SIGN	VALUE[6:0]						
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 7 – SIGN: Correction Sign

Value	Description
0	The correction value is positive, i.e., frequency will be decreased.
1	The correction value is negative, i.e., frequency will be increased.

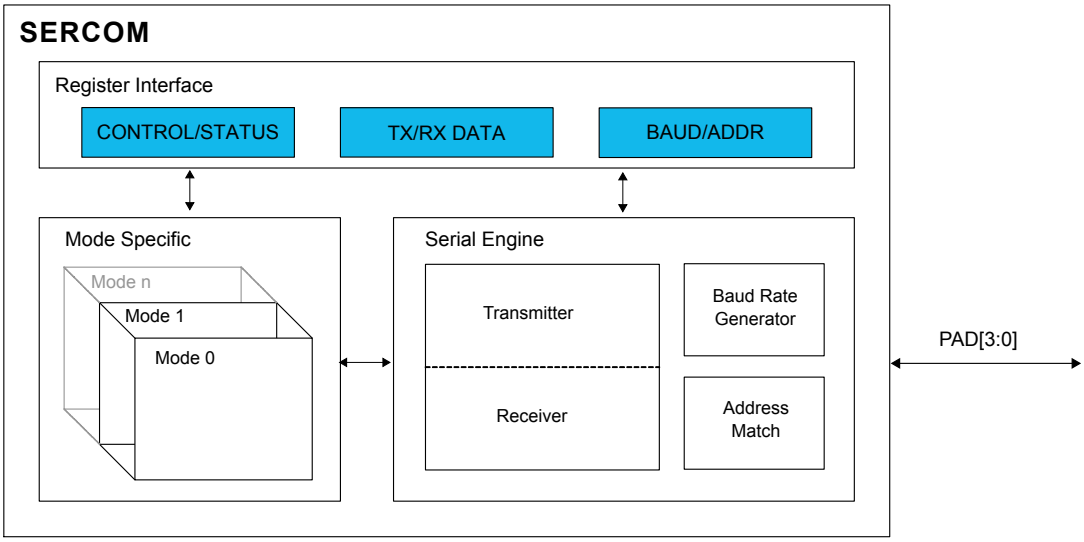
Bits 6:0 – VALUE[6:0]: Correction Value
These bits define the amount of correction applied to the RTC prescaler.

Value	Description
0	Correction is disabled and the RTC frequency is unchanged.
1 - 127	The RTC frequency is adjusted according to the value.

24.10.9 Counter Value in COUNT16 mode (CTRLA.MODE=1)

30.3 Block Diagram

Figure 30-1. SERCOM Block Diagram



30.4 Signal Description

See the respective SERCOM mode chapters for details.

Related Links

SERCOM USART – SERCOM Universal Synchronous and Asynchronous Receiver and Transmitter

SERCOM SPI – SERCOM Serial Peripheral Interface

SERCOM I2C – SERCOM Inter-Integrated Circuit

30.5 Product Dependencies

In order to use this peripheral, other parts of the system must be configured correctly, as described below.

30.5.1 I/O Lines

Using the SERCOM I/O lines requires the I/O pins to be configured using port configuration (PORT).

The SERCOM has four internal pads, PAD[3:0], and the signals from I2C, SPI and USART are routed through these SERCOM pads via a multiplexer. The configuration of the multiplexer is available from the different SERCOM modes. Refer to the mode specific chapters for details.

Related Links

SERCOM USART – SERCOM Universal Synchronous and Asynchronous Receiver and Transmitter

SERCOM SPI – SERCOM Serial Peripheral Interface

SERCOM I2C – SERCOM Inter-Integrated Circuit

PORT: IO Pin Controller

Block Diagram

30.5.2 Power Management

The SERCOM can operate in any sleep mode where the selected clock source is running. SERCOM interrupts can be used to wake up the device from sleep modes.

31.6.2.3 Clock Generation and Selection

For both synchronous and asynchronous modes, the clock used for shifting and sampling data can be generated internally by the SERCOM baud-rate generator or supplied externally through the XCK line.

The synchronous mode is selected by writing a '1' to the Communication Mode bit in the Control A register (CTRLA.CMODE), the asynchronous mode is selected by writing a zero to CTRLA.CMODE.

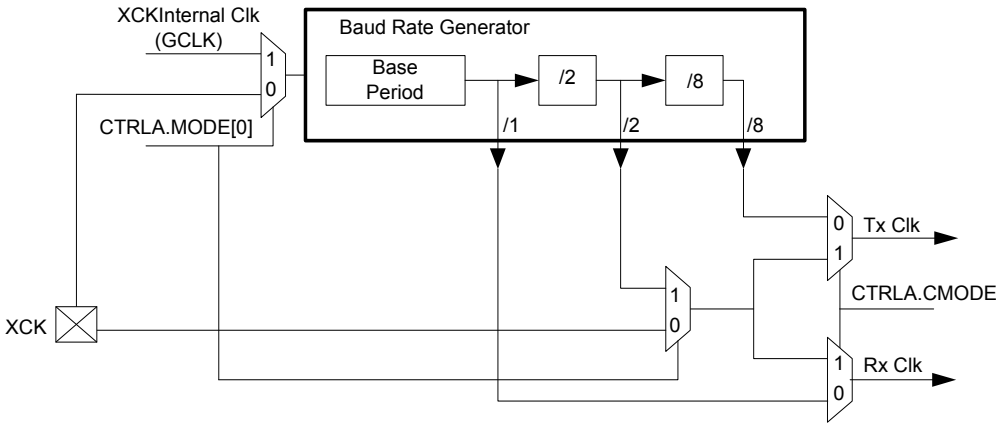
The internal clock source is selected by writing 0x1 to the Operation Mode bit field in the Control A register (CTRLA.MODE), the external clock source is selected by writing 0x0 to CTRLA.MODE.

The SERCOM baud-rate generator is configured as in the figure below.

In asynchronous mode (CTRLA.CMODE=0), the 16-bit Baud register value is used.

In synchronous mode (CTRLA.CMODE=1), the eight LSBs of the Baud register are used. Refer to *Clock Generation – Baud-Rate Generator* for details on configuring the baud rate.

Figure 31-3. Clock Generation



Related Links

Clock Generation – Baud-Rate Generator

Asynchronous Arithmetic Mode BAUD Value Selection

Synchronous Clock Operation

In synchronous mode, the CTRLA.MODE bit field determines whether the transmission clock line (XCK) serves either as input or output. The dependency between clock edges, data sampling, and data change is the same for internal and external clocks. Data input on the RxD pin is sampled at the opposite XCK clock edge when data is driven on the TxD pin.

The Clock Polarity bit in the Control A register (CTRLA.CPOL) selects which XCK clock edge is used for RxD sampling, and which is used for TxD change:

When CTRLA.CPOL is '0', the data will be changed on the rising edge of XCK, and sampled on the falling edge of XCK.

When CTRLA.CPOL is '1', the data will be changed on the falling edge of XCK, and sampled on the rising edge of XCK.

Bit 4 – CTSIC: Clear to Send Input Change
This flag is cleared by writing a '1' to it.

This flag is set when a change is detected on the CTS pin.

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the flag.

Bit 3 – RXS: Receive Start
This flag is cleared by writing '1' to it.

This flag is set when a start condition is detected on the RxD line and start-of-frame detection is enabled (CTRLB.SFDE is '1').

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the Receive Start interrupt flag.

Bit 2 – RXC: Receive Complete
This flag is cleared by reading the Data register (DATA) or by disabling the receiver.

This flag is set when there are unread data in DATA.

Writing '0' to this bit has no effect.

Writing '1' to this bit has no effect.

Bit 1 – TXC: Transmit Complete
This flag is cleared by writing '1' to it or by writing new data to DATA.

This flag is set when the entire frame in the transmit shift register has been shifted out and there are no new data in DATA.

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the flag.

Bit 0 – DRE: Data Register Empty
This flag is cleared by writing new data to DATA.

This flag is set when DATA is empty and ready to be written.

Writing '0' to this bit has no effect.

Writing '1' to this bit has no effect.

31.8.9 Status

Name: STATUS
Offset: 0x1A
Reset: 0x0000
Property: -

Figure 33-2. Transaction Diagram Symbols

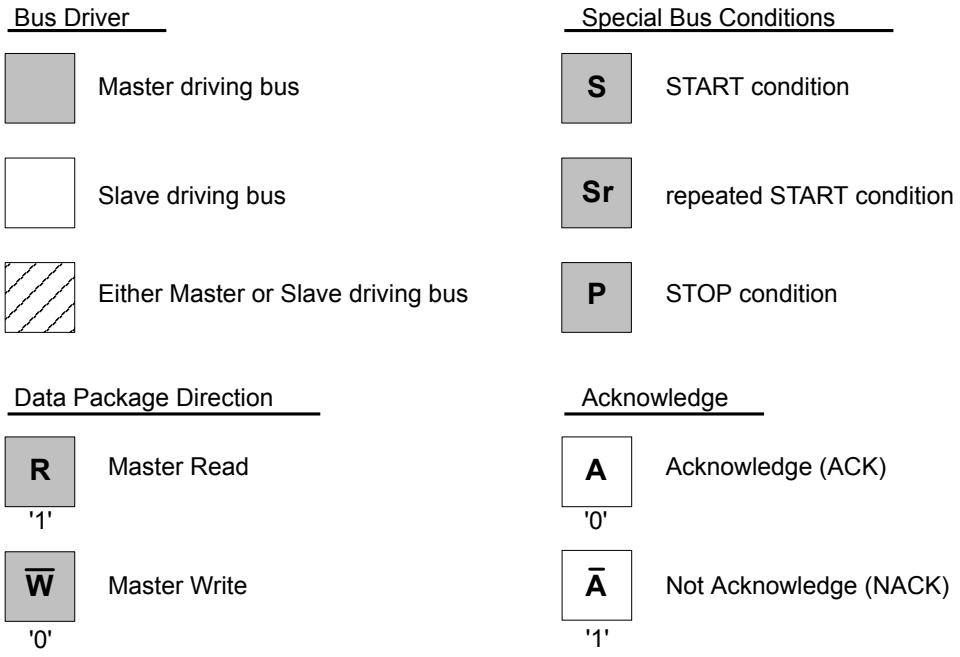
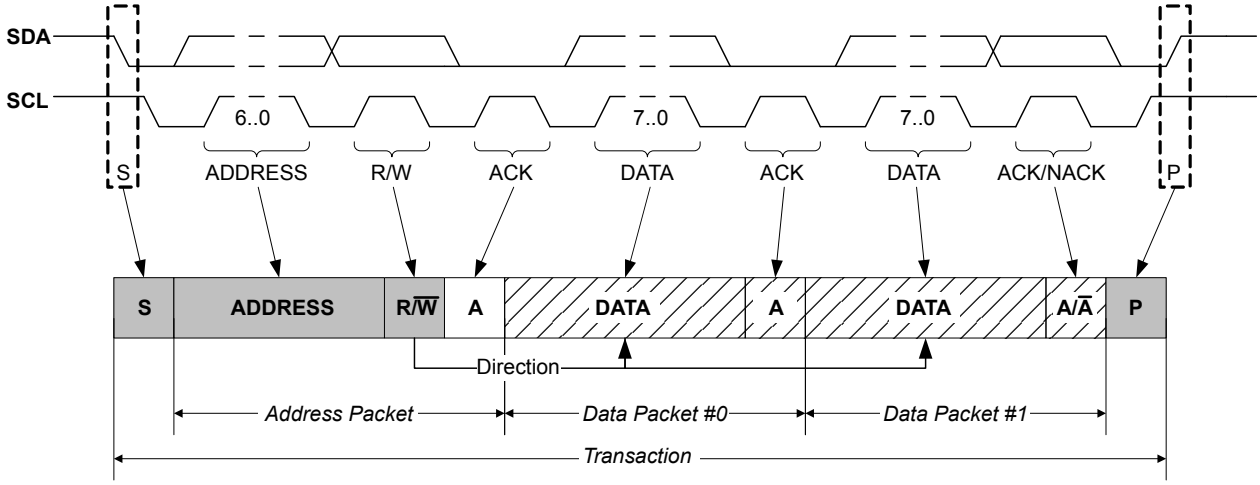


Figure 33-3. Basic I²C Transaction Diagram



33.6.2 Basic Operation

33.6.2.1 Initialization

The following registers are enable-protected, meaning they can be written only when the I²C interface is disabled (CTRLA.ENABLE is '0'):

- Control A register (CTRLA), except Enable (CTRLA.ENABLE) and Software Reset (CTRLA.SWRST) bits
- Control B register (CTRLB), except Acknowledge Action (CTRLB.ACKACT) and Command (CTRLB.CMD) bits
- Baud register (BAUD)
- Address register (ADDR) in slave operation.

When the I²C is enabled or is being enabled (CTRLA.ENABLE=1), writing to these registers will be discarded. If the I²C is being disabled, writing to these registers will be completed after the disabling.

Name: INTENCLR
Offset: 0x14 [ID-00001bb3]
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
	ERROR						SB	MB
Access	R/W						R/W	R/W
Reset	0						0	0

Bit 7 – ERROR: Error Interrupt Enable
Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the Error Interrupt Enable bit, which disables the Error interrupt.

Value	Description
0	Error interrupt is disabled.
1	Error interrupt is enabled.

Bit 1 – SB: Slave on Bus Interrupt Enable
Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the Slave on Bus Interrupt Enable bit, which disables the Slave on Bus interrupt.

Value	Description
0	The Slave on Bus interrupt is disabled.
1	The Slave on Bus interrupt is enabled.

Bit 0 – MB: Master on Bus Interrupt Enable
Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the Master on Bus Interrupt Enable bit, which disables the Master on Bus interrupt.

Value	Description
0	The Master on Bus interrupt is disabled.
1	The Master on Bus interrupt is enabled.

33.10.5 Interrupt Enable Clear

This register allows the user to enable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Clear register (INTENCLR).

Name: INTENSET
Offset: 0x16 [ID-00001bb3]
Reset: 0x00
Property: PAC Write-Protection

Value	Description
0	Interrupt disabled.
1	Interrupt enabled.

Bit 26 – WDIE: Watchdog Interrupt Enable

Value	Description
0	Interrupt disabled.
1	Interrupt enabled.

Bit 25 – BOE: Bus_Off Status Interrupt Enable

Value	Description
0	Interrupt disabled.
1	Interrupt enabled.

Bit 24 – EWE: Error Warning Status Interrupt Enable

Value	Description
0	Interrupt disabled.
1	Interrupt enabled.

Bit 23 – EPE: Error Passive Interrupt Enable

Value	Description
0	Interrupt disabled.
1	Interrupt enabled.

Bit 22 – ELOE: Error Logging Overflow Interrupt Enable

Value	Description
0	Interrupt disabled.
1	Interrupt enabled.

Bit 21 – BEUE: Bit Error Uncorrected Interrupt Enable.

Value	Description
0	Interrupt disabled.
1	Interrupt enabled.

Bit 20 – BECE: Bit Error Corrected Interrupt Enable

Value	Description
0	Interrupt disabled.
1	Interrupt enabled.

Bit 19 – DRXE: Message stored to Dedicated Rx Buffer Interrupt Enable

Value	Description
0	Interrupt disabled.
1	Interrupt enabled.

Bit 18 – TOOE: Timeout Occurred Interrupt Enable

Bit 17 – MRAFL: Message RAM Access Failure Interrupt Line

Value	Description
0	Interrupt assigned to CAN interrupt line 0.
1	Interrupt assigned to CAN interrupt line 1.

Bit 16 – TSWL: Timestamp Wraparound Interrupt Line

Value	Description
0	Interrupt assigned to CAN interrupt line 0.
1	Interrupt assigned to CAN interrupt line 1.

Bit 15 – TEFLL: Tx Event FIFO Event Lost Interrupt Line

Value	Description
0	Interrupt assigned to CAN interrupt line 0.
1	Interrupt assigned to CAN interrupt line 1.

Bit 14 – TEFFL: Tx Event FIFO Full Interrupt Line

Value	Description
0	Interrupt assigned to CAN interrupt line 0.
1	Interrupt assigned to CAN interrupt line 1.

Bit 13 – TEFWL: Tx Event FIFO Watermark Reached Interrupt Line

Value	Description
0	Interrupt assigned to CAN interrupt line 0.
1	Interrupt assigned to CAN interrupt line 1.

Bit 12 – TEFNL: Tx Event FIFO New Entry Interrupt Line

Value	Description
0	Interrupt assigned to CAN interrupt line 0.
1	Interrupt assigned to CAN interrupt line 1.

Bit 11 – TFEL: Tx FIFO Empty Interrupt Line

Value	Description
0	Interrupt assigned to CAN interrupt line 0.
1	Interrupt assigned to CAN interrupt line 1.

Bit 10 – TCFL: Transmission Cancellation Finished Interrupt Line

Value	Description
0	Interrupt assigned to CAN interrupt line 0.
1	Interrupt assigned to CAN interrupt line 1.

Bit 9 – TCL: Transmission Completed Interrupt Line

Value	Description
0	Interrupt assigned to CAN interrupt line 0.
1	Interrupt assigned to CAN interrupt line 1.

Bits 16, 17 – CAPTENx: Capture Channel x Enable
Bit x of CAPTEN[1:0] selects whether channel x is a capture or a compare channel.

These bits are not synchronized.

Value	Description
0	CAPTEN disables capture on channel x.
1	CAPTEN enables capture on channel x.

Bit 11 – ALOCK: Auto Lock
When this bit is set, Lock bit update (LUPD) is set to '1' on each overflow/underflow or re-trigger event.

This bit is not synchronized.

Value	Description
0	The LUPD bit is not affected on overflow/underflow, and re-trigger event.
1	The LUPD bit is set on each overflow/underflow or re-trigger event.

Bits 10:8 – PRESCALER[2:0]: Prescaler
These bits select the counter prescaler factor.

These bits are not synchronized.

Value	Name	Description
0x0	DIV1	Prescaler: GCLK_TC
0x1	DIV2	Prescaler: GCLK_TC/2
0x2	DIV4	Prescaler: GCLK_TC/4
0x3	DIV8	Prescaler: GCLK_TC/8
0x4	DIV16	Prescaler: GCLK_TC/16
0x5	DIV64	Prescaler: GCLK_TC/64
0x6	DIV256	Prescaler: GCLK_TC/256
0x7	DIV1024	Prescaler: GCLK_TC/1024

Bit 7 – ONDEMAND: Clock On Demand
This bit selects the clock requirements when the TC is stopped.

In standby mode, if the Run in Standby bit (CTRLA.RUNSTDBY) is '0', ONDEMAND is forced to '0'.

This bit is not synchronized.

Value	Description
0	The On Demand is disabled. If On Demand is disabled, the TC will continue to request the clock when its operation is stopped (STATUS.STOP=1).
1	The On Demand is enabled. When On Demand is enabled, the stopped TC will not request the clock. The clock is requested when a software re-trigger command is applied or when an event with start/re-trigger action is detected.

Bit 6 – RUNSTDBY: Run in Standby
This bit is used to keep the TC running in standby mode.

This bit is not synchronized.

Value	Description
0	The TC is halted in standby.
1	The TC continues to run in standby.

Channel Capture (MCx)	For a capture channel, the request is set when valid data is present in the CCx register, and cleared once the CCx register is read. In this operation mode, the CTRLA.DMAOS bit value is ignored.

DMA Operation with Circular Buffer

When circular buffer operation is enabled, the buffer registers must be written in a correct order and synchronized to the update times of the timer. The DMA triggers of the TCC provide a way to ensure a safe and correct update of circular buffers.

Note: Circular buffer are intended to be used with RAMP2, RAMP2A and DSBOTH operation only.

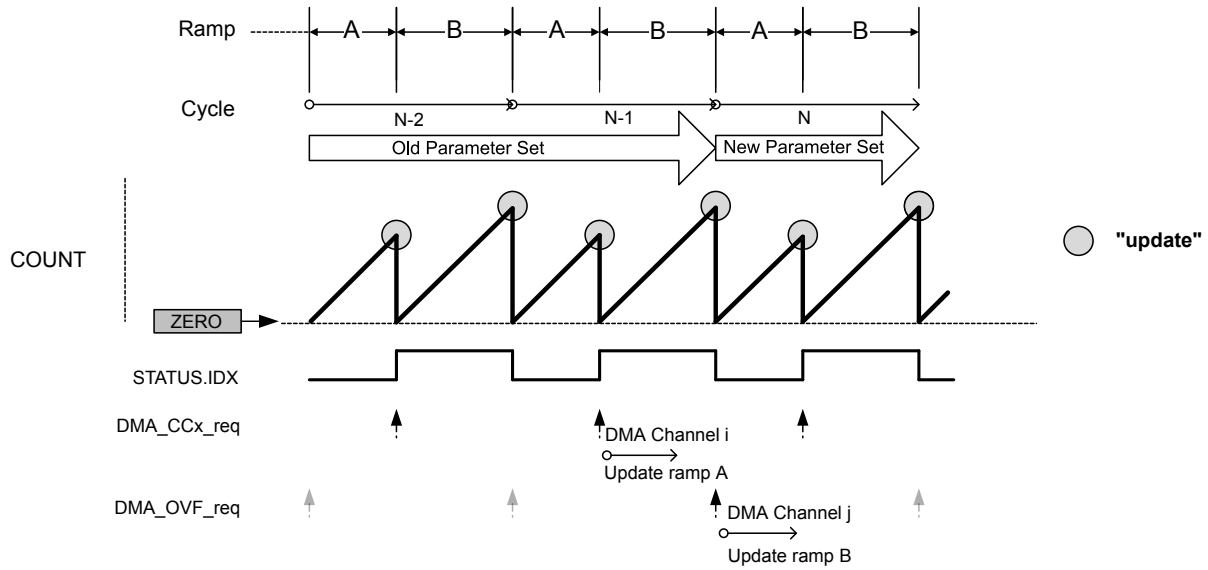
DMA Operation with Circular Buffer in RAMP and RAMP2A Mode

When a CCx channel is selected as a circular buffer, the related DMA request is not set on a compare match detection, but on start of ramp B.

If at least one circular buffer is enabled, the DMA overflow request is conditioned to the start of ramp A with an effective DMA transfer on previous ramp B (DMA acknowledge).

The update of all circular buffer values for ramp A can be done through a DMA channel triggered on a MC trigger. The update of all circular buffer values for ramp B, can be done through a second DMA channel triggered by the overflow DMA request.

Figure 36-37. DMA Triggers in RAMP and RAMP2 Operation Mode and Circular Buffer Enabled



DMA Operation with Circular Buffer in DSBOTH Mode

When a CC channel is selected as a circular buffer, the related DMA request is not set on a compare match detection, but on start of down-counting phase.

If at least one circular buffer is enabled, the DMA overflow request is conditioned to the start of up-counting phase with an effective DMA transfer on previous down-counting phase (DMA acknowledge).

When up-counting, all circular buffer values can be updated through a DMA channel triggered by MC trigger. When down-counting, all circular buffer values can be updated through a second DMA channel, triggered by the OVF DMA request.

Offset	Name	Bit Pos.								
0x2B										
0x2C	ANACTRL	7:0	BUFTEST	ONCHOP		CTLSDADC[4:0]				
0x2D	Reserved									
0x2E	DBGCTRL	7:0								DBGRUN

39.8 Register Description

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16-, and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly.

Some registers are optionally write-protected by the Peripheral Access Controller (PAC). Optional PAC write-protection is denoted by the "PAC Write-Protection" property in each individual register description. For details, refer to

Some registers are synchronized when read and/or written. Synchronization is denoted by the "Write-Synchronized" or the "Read-Synchronized" property in each individual register description. For details, refer to

Some registers are enable-protected, meaning they can only be written when the peripheral is disabled. Enable-protection is denoted by the "Enable-Protected" property in each individual register description.

39.8.1 Control A

Name: CTRLA
Offset: 0x00 [ID-0000243d]
Reset: 0x00
Property: PAC Write-Protection, Write-Synchronized (ENABLE, SWRST)

Bit	7	6	5	4	3	2	1	0
	ONDEMAND	RUNSTDBY					ENABLE	SWRST
Access	R/W	R/W					R/W	R/W
Reset	0	0					0	0

Bit 7 – ONDEMAND: On Demand Control
The On Demand operation modes allows the SDADC to be enabled or disabled, depending on other peripheral request.

In On Demand operation mode, i.e., if the ONDEMAND bit has been previously written to one, the SDADC will only be running when requested by a peripheral. If there is no peripheral requesting the SDADC will be in a disable state.

If On Demand is disable the SDADC will always be running when enabled.

In standby sleep mode, the On Demand operation is still active if the CTRLA.RUNSTDBY bit is one. If CTRLA.RUNSTDBY is zero, the SDADC is disabled.

This bit is not synchronized.