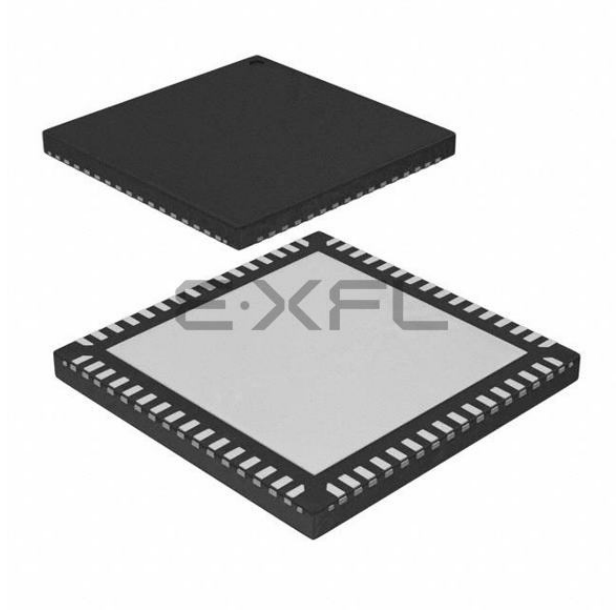

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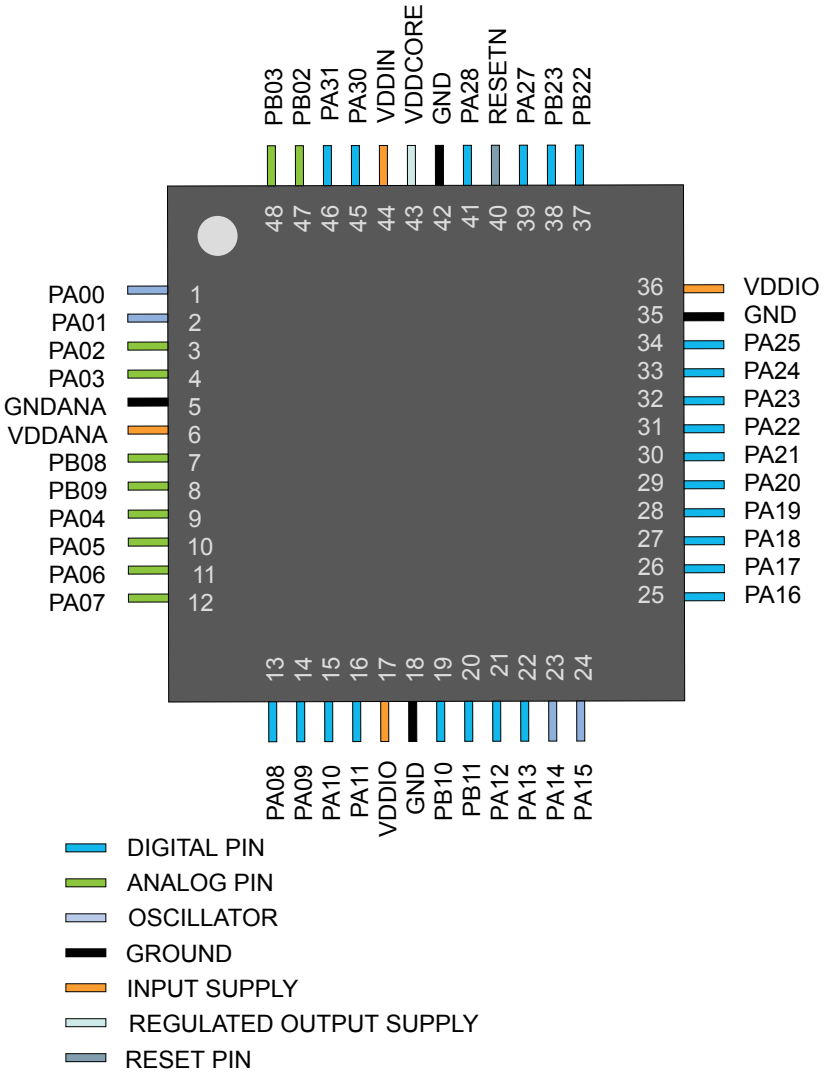
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, WDT
Number of I/O	52
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamc20j18a-mut

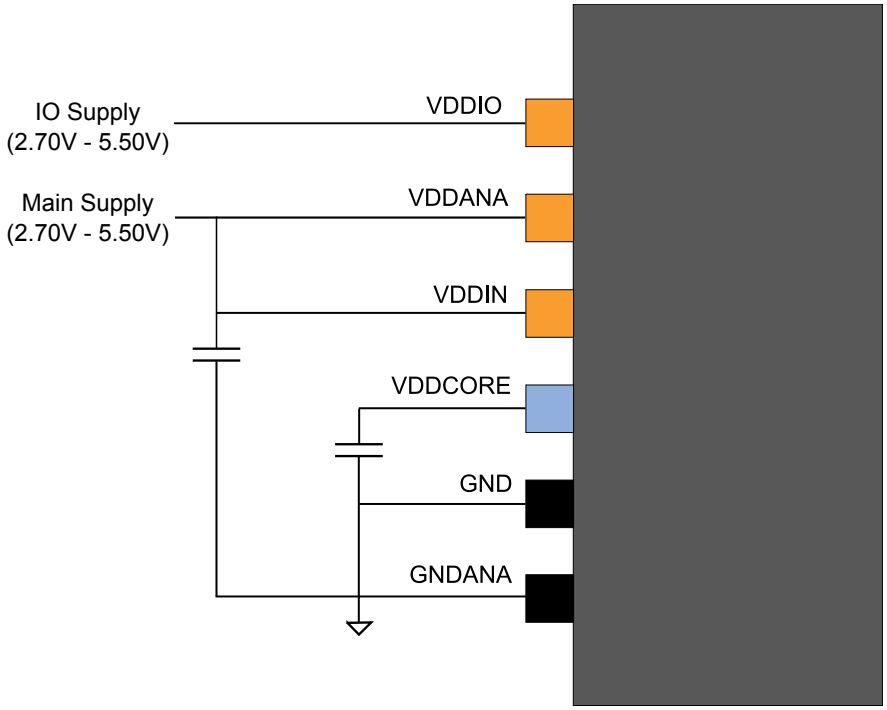
4.2 SAM C21G / SAM C20G

4.2.1 QFN48 / TQFP48



Signal Name	Function	Type	Active Level
Timer Counter - TCCx			
WO[1:0]	Waveform Outputs	Digital	
Peripheral Touch Controller - PTC			
X[15:0]	PTC Input	Analog	
Y[15:0]	PTC Input	Analog	
General Purpose I/O - PORT			
PA25 - PA00	Parallel I/O Controller I/O Port A	Digital	
PA28 - PA27	Parallel I/O Controller I/O Port A	Digital	
PA31 - PA30	Parallel I/O Controller I/O Port A	Digital	
PB17 - PB00	Parallel I/O Controller I/O Port B	Digital	
PB21 - PB19	Parallel I/O Controller I/O Port B	Digital	
PB25 - PB22	Parallel I/O Controller I/O Port B	Digital	
PB31 - PB30	Parallel I/O Controller I/O Port B	Digital	
PC03 - PC-00	Parallel I/O Controller I/O Port C	Digital	
PC21 - PC05	Parallel I/O Controller I/O Port C	Digital	
PC28 - PC24	Parallel I/O Controller I/O Port C	Digital	
Controller Area Network - CAN			
TX	CAN Transmit Line	Digital	
RX	CAN Receive Line	Digital	

Figure 7-4. Power Supply Connection for Dual Supply Mode



7.2.4 Power-Up Sequence

7.2.4.1 Minimum Rise Rate

The integrated Power-on Reset (POR) circuitry, monitoring the VDDIN power supply, requires a minimum rise rate.

7.2.4.2 Maximum Rise Rate

The rise rate of the power supply must not exceed the values described in Electrical Characteristics.

7.3 Power-Up

This section summarizes the power-up sequence of the SAM C20/C21. The behavior after power-up is controlled by the Power Manager.

7.3.1 Starting of Clocks

After power-up, the device is set to its initial state and kept in reset, until the power has stabilized throughout the device. Once the power has stabilized, the device will use a 4MHz clock. This clock is derived from the 48MHz Internal Oscillator (OSC48M), which is configured to provide a 4MHz clock and used as a clock source for generic clock generator 0. Generic clock generator 0 is the main clock for the Power Manager (PM).

Some synchronous system clocks are active, allowing software execution.

Refer to the “Clock Mask Register” in the Power Manager for the list of default peripheral clocks running. Synchronous system clocks that are running are by default not divided and receive a 4MHz clock through generic clock generator 0. Other generic clocks are disabled.

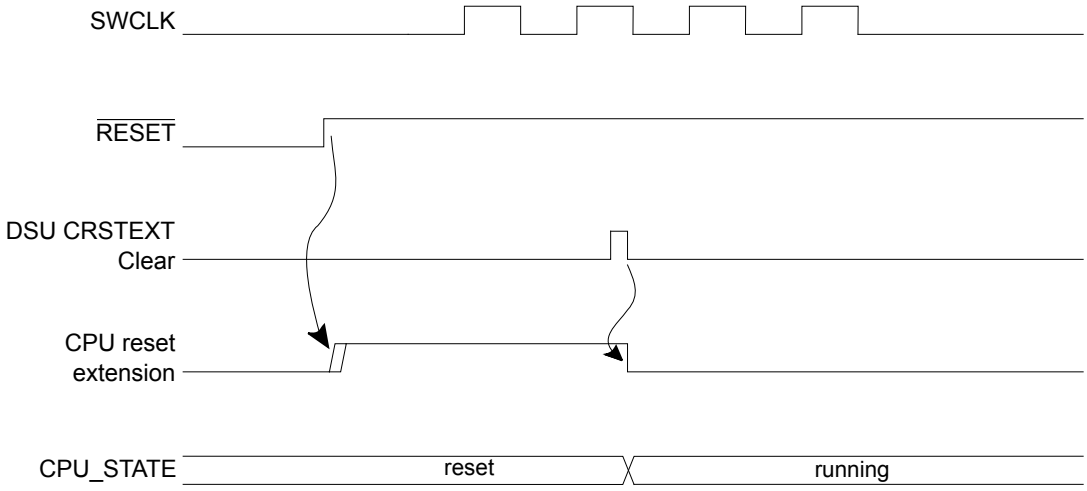
7.3.2 I/O Pins

After power-up, the I/O pins are tri-stated.

13.6.2 CPU Reset Extension

"CPU reset extension" refers to the extension of the reset phase of the CPU core after the external reset is released. This ensures that the CPU is not executing code at startup while a debugger is connects to the system. The debugger is detected on a $\overline{\text{RESET}}$ release event when SWCLK is low. At startup, SWCLK is internally pulled up to avoid false detection of a debugger if the SWCLK pin is left unconnected. When the CPU is held in the reset extension phase, the CPU Reset Extension bit of the Status A register (STATUSA.CRSTEXT) is set. To release the CPU, write a '1' to STATUSA.CRSTEXT. STATUSA.CRSTEXT will then be set to '0'. Writing a '0' to STATUSA.CRSTEXT has no effect. For security reasons, it is not possible to release the CPU reset extension when the device is protected by the NVMCTRL security bit. Trying to do so sets the Protection Error bit (PERR) of the Status A register (STATUSA.PERR).

Figure 13-2. Typical CPU Reset Extension Set and Clear Timing Diagram



Related Links

NVMCTRL – Non-Volatile Memory Controller

Security Bit

13.6.3 Debugger Probe Detection

13.6.3.1 Cold Plugging

Cold-Plugging is the detection of a debugger when the system is in reset. Cold-Plugging is detected when the CPU reset extension is requested, as described above.

13.6.3.2 Hot Plugging

Hot-Plugging is the detection of a debugger probe when the system is not in reset. Hot-Plugging is not possible under reset because the detector is reset when POR or $\overline{\text{RESET}}$ are asserted. Hot-Plugging is active when a SWCLK falling edge is detected. The SWCLK pad is multiplexed with other functions and the user must ensure that its default function is assigned to the debug system. If the SWCLK function is changed, the Hot-Plugging feature is disabled until a power-reset or external reset occurs. Availability of the Hot-Plugging feature can be read from the Hot-Plugging Enable bit of the Status B register (STATUSB.HPE).

21.7 Register Summary

Offset	Name	Bit Pos.								
0x00	INTENCLR	7:0						CLKFAIL	OSC32KRDY	XOSC32KRDY
0x01		15:8								
0x02		23:16								
0x03		31:24								
0x04	INTENSET	7:0						CLKFAIL	OSC32KRDY	XOSC32KRDY
0x05		15:8								
0x06		23:16								
0x07		31:24								
0x08	INTFLAG	7:0						CLKFAIL	OSC32KRDY	XOSC32KRDY
0x09		15:8								
0x0A		23:16								
0x0B		31:24								
0x0C	STATUS	7:0					CLKSW	CLKFAIL	OSC32KRDY	XOSC32KRDY
0x0D		15:8								
0x0E		23:16								
0x0F		31:24								
0x10 ... 0x13	Reserved									
0x14	XOSC32K	7:0	ONDEMAND	RUNSTDBY		EN1K	EN32K	XTALEN	ENABLE	
0x15		15:8				WRTLOCK		STARTUP[2:0]		
0x16	CFDCTRL	7:0						CFDPRESC	SWBACK	CFDEN
0x17	EVCTRL	7:0								CFDEO
0x18	OSC32K	7:0	ONDEMAND	RUNSTDBY			EN1K	EN32K	ENABLE	
0x19		15:8				WRTLOCK		STARTUP[2:0]		
0x1A		23:16		CALIB[6:0]						
0x1B		31:24								
0x1C	OSCULP32K	7:0								
0x1D		15:8	WRTLOCK			CALIB[4:0]				
0x1E		23:16								
0x1F		31:24								

21.8 Register Description

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16-, and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register and the 8-bit halves of a 16-bit register can be accessed directly.

All registers with write-access can be write-protected optionally by the peripheral access controller (PAC). Optional Write-Protection by the Peripheral Access Controller (PAC) is denoted by the "PAC Write-

Each interrupt can be individually enabled by writing a '1' to the corresponding bit in the Interrupt Enable Set register (INTENSET), and disabled by writing a '1' to the corresponding bit in the Interrupt Enable Clear register (INTENCLR).

An interrupt request is generated when the interrupt flag is set and the corresponding interrupt is enabled. The interrupt request remains active until either the interrupt flag is cleared, the interrupt is disabled, or the SUPC is reset. See the INTFLAG register for details on how to clear interrupt flags. The SUPC has one common interrupt request line for all the interrupt sources. The user must read the INTFLAG register to determine which interrupt condition is present.

Note: Interrupts must be globally enabled for interrupt requests to be generated.

Related Links

Nested Vector Interrupt Controller

Sleep Mode Controller

22.6.5 Synchronization

The prescaler counters that are used to trigger brown-out detections operate asynchronously from the peripheral bus. As a consequence, the BODVDD Enable bit (BODVDD.ENABLE) need synchronization when written.

The Write-Synchronization of the Enable bit is triggered by writing a '1' to the Enable bit of the BODVDD Control register. The Synchronization Ready bit (STATUS.BVDDSRDY) in the STATUS register will be cleared when the Write-Synchronization starts, and set again when the Write-Synchronization is complete. Writing to the same register while the Write-Synchronization is ongoing (STATUS.BVDDSRDY is '0') will generate an error without stalling the APB bus.

CMD[6:0]	Group Configuration	Description
0x00-0x01	-	Reserved
0x02	ER	Erase Row - Erases the row addressed by the ADDR register in the NVM main array.
0x03	-	Reserved
0x04	WP	Write Page - Writes the contents of the page buffer to the page addressed by the ADDR register.
0x05	EAR	Erase Auxiliary Row - Erases the auxiliary row addressed by the ADDR register. This command can be given only when the security bit is not set and only to the User Configuration Row.
0x06	WAP	Write Auxiliary Page - Writes the contents of the page buffer to the page addressed by the ADDR register. This command can be given only when the security bit is not set and only to the User Configuration Row.
0x07-0x0E	-	Reserved
0x0F	WL	Write Lockbits- write the LOCK register
0x1A-0x19	-	Reserved
0x1A	RWWEEER	RWWEE Erase Row - Erases the row addressed by the ADDR register in the RWWEE array.
0x1B	-	Reserved
0x1C	RWWEEWP	RWWEE Write Page - Writes the contents of the page buffer to the page addressed by the ADDR register in the RWWEE array.
0x1D-0x3F	-	Reserved
0x40	LR	Lock Region - Locks the region containing the address location in the ADDR register.
0x41	UR	Unlock Region - Unlocks the region containing the address location in the ADDR register.
0x42	SPRM	Sets the Power Reduction Mode.
0x43	CPRM	Clears the Power Reduction Mode.
0x44	PBC	Page Buffer Clear - Clears the page buffer.
0x45	SSB	Set Security Bit - Sets the security bit by writing 0x00 to the first byte in the lockbit row.
0x46	INVALL	Invalidates all cache lines.
0x47	LDR	Lock Data Region - Locks the data region containing the address location in the ADDR register. When the Security Extension is enabled, only secure access can lock secure regions.

Bit	31	30	29	28	27	26	25	24
	OUTCLR[31:24]							
Access	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	OUTCLR[23:16]							
Access	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	OUTCLR[15:8]							
Access	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	OUTCLR[7:0]							
Access	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – OUTCLR[31:0]: PORT Data Output Value Clear
Writing '0' to a bit has no effect.

Writing '1' to a bit will clear the corresponding bit in the OUT register. Pins configured as outputs via the Data Direction register (DIR) will be set to low output drive level. Pins configured as inputs via DIR and with pull enabled via the Pull Enable bit in the Pin Configuration register (PINCFG.PULLEN) will set the input pull direction to an internal pull-down.

Value	Description
0	The corresponding I/O pin in the PORT group will keep its configuration.
1	The corresponding I/O pin output is driven low, or the input is connected to an internal pull-down.

28.9.7 Data Output Value Set

This register allows the user to set one or more output I/O pin drive levels high, without doing a read-modify-write operation. Changes in this register will also be reflected in the Data Output Value (OUT), Data Output Value Toggle (OUTTGL) and Data Output Value Clear (OUTCLR) registers.

Tip: The I/O pins are assembled in pin groups (”PORT groups”) with up to 32 pins. Group 0 consists of the PA pins, group 1 is for the PB pins, etc. Each pin group has its own PORT registers. For example, the register address offset for the Data Direction (DIR) register for group 0 (PA00 to PA31) is 0x00, and the register address offset for the DIR register for group 1 (PB00 to PB31) is 0x80.

Name: OUTSET
Offset: 0x18
Reset: 0x00000000
Property: PAC Write-Protection

Bit 1 – FERR: Frame Error
Reading this bit before reading the Data register will indicate the error status of the next character to be read.

This bit is cleared by writing '1' to the bit or by disabling the receiver.

This bit is set if the received character had a frame error, i.e., when the first stop bit is zero.

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear it.

Bit 0 – PERR: Parity Error
Reading this bit before reading the Data register will indicate the error status of the next character to be read.

This bit is cleared by writing '1' to the bit or by disabling the receiver.

This bit is set if parity checking is enabled (CTRLA.FORM is 0x1, 0x5) and a parity error is detected.

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear it.

31.8.10 Synchronization Busy

Name: SYNCBUSY
Offset: 0x1C [ID-00000fa7]
Reset: 0x00000000
Property: -

All enabled filter elements are used for acceptance filtering of standard frames. Acceptance filtering stops at the first matching enabled filter element or when the end of the filter list is reached. If SFEC = “100”, “101”, or “110” a match sets interrupt flag IR.HPM and, if enabled, an interrupt is generated. In this case register HPMS is updated with the status of the priority match.

Table 34-14. Standard Filter Element Configuration

Value	Name	Description
0x0	DISABLE	Disable filter element
0x1	STF0M	Store in Rx FIFO 0 if filter matches
0x2	STF1M	Store in Rx FIFO 1 if filter matches
0x3	REJECT	Reject ID if filter matches
0x4	PRIORITY	Set priority if filter matches.
0x5	PRIF0M	Set priority and store in FIFO 0 if filter matches.
0x6	PRIF1M	Set priority and store in FIFO 1 if filter matches.
0x7	STRXBUF	Store into Rx Buffer or as debug message, configuration of SFT[1:0] ignored.

- Bits 26:16 - SFID1[10:0]: Standard Filter ID 1

  First ID of standard ID filter element.

  When filtering for Rx Buffers or for debug messages this field defines the ID of a standard mesage to be stored. The received identifiers must match exactly, no masking mechanism is used.
- Bits 15:11 - Reserved
- Bits 10:0 - SFID2[10:0]: Standard Filter ID 2

  This bit field has a different meaning depending on the configuration of SFEC.

  5.1. SFEC = “001” ... “110”: Second ID of standard ID filter element.

  5.2. SFEC = “111”: Filter for Rx Buffers or for debug messages.

  SFID2[10:9] decides whether the received message is stored into an Rx Buffer or treated as message A, B, or C of the debug message sequence.
  00 = Store message into an Rx Buffer
  01 = Debug Message A
  10 = Debug Message B
  11 = Debug Message C

  SFID2[8:6] is used to control the filter event pins at the Extension Interface. A ‘1’ at the respective bit position enables generation of a pulse at the related filter event pin with the duration of one CLK_CAN_APB period in case the filter matches.

  SFID2[5:0] defines the offset to the Rx Buffer Start Address RXBC.RBSA for storage of a matching message.

34.9.6 Extended Message ID Filter Element

Up to 64 filter elements can be configured for 29-bit extended IDs. When accessing an Extended Message ID Filter element, its address is the Filter List Extended Start Address XIDFC.FLESA plus two times the index of the filter element (0…63).

Writing a '1' to this bit resets all registers in the TC, except DBGCTRL, to their initial state, and the TC will be disabled.

Writing a '1' to CTRLA.SWRST will always take precedence; all other writes in the same write-operation will be discarded.

Due to synchronization there is a delay from writing CTRLA.SWRST until the reset is complete. CTRLA.SWRST and SYNCBUSY.SWRST will both be cleared when the reset is complete.

This bit is not enable protected.

Value	Description
0	There is no reset operation ongoing.
1	The reset operation is ongoing.

35.7.3.2 Control B Clear

This register allows the user to clear bits in the CTRLB register without doing a read-modify-write operation. Changes in this register will also be reflected in the Control B Set register (CTRLBSET).

Name: CTRLBCLR
Offset: 0x04
Reset: 0x00
Property: PAC Write-Protection, Read-Synchronized, Write-Synchronized

Bit	7	6	5	4	3	2	1	0
	CMD[2:0]					ONESHOT	LUPD	DIR
Access	R/W	R/W	R/W			R/W	R/W	R/W
Reset	0	0	0			0	0	0

Bits 7:5 – CMD[2:0]: Command
These bits are used for software control of the TC. The commands are executed on the next prescaled GCLK_TC clock cycle. When a command has been executed, the CMD bit group will be read back as zero.

Writing 0x0 to these bits has no effect.

Writing a '1' to any of these bits will clear the pending command.

Bit 2 – ONESHOT: One-Shot on Counter
This bit controls one-shot operation of the TC.

Writing a '0' to this bit has no effect

Writing a '1' to this bit will disable one-shot operation.

Value	Description
0	The TC will wrap around and continue counting on an overflow/underflow condition.
1	The TC will wrap around and stop on the next underflow/overflow condition.

Bit 1 – LUPD: Lock Update
This bit controls the update operation of the TC buffered registers.

When CTRLB.LUPD is set, no any update of the registers with value of its buffered register is performed on hardware UPDATE condition. Locking the update ensures that all buffer registers are valid before an

Bit 3 – PERBUFV: Period Buffer Valid
This bit is set when a new value is written to the PERBUF register. The bit is cleared by writing '1' to the corresponding location when CTRLB.LUPD is set, or automatically cleared by hardware on UPDATE condition. This bit is available only in 8-bit mode and will always read zero in 16- and 32-bit modes.

Bit 1 – SLAVE: Slave Status Flag
This bit is only available in 32-bit mode on the slave TC (i.e., TC1 and/or TC3). The bit is set when the associated master TC (TC0 and TC2, respectively) is set to run in 32-bit mode.

Bit 0 – STOP: Stop Status Flag
This bit is set when the TC is disabled, on a Stop command, or on an overflow/underflow condition when the One-Shot bit in the Control B Set register (CTRLBSET.ONESHOT) is '1'.

Value	Description
0	Counter is running.
1	Counter is stopped.

35.7.3.9 Waveform Generation Control

Name: WAVE
Offset: 0x0C
Reset: 0x00
Property: PAC Write-Protection, Enable-Protected

Bit	7	6	5	4	3	2	1	0
							WAVEGEN[1:0]	
Access							R/W	R/W
Reset							0	0

Bits 1:0 – WAVEGEN[1:0]: Waveform Generation Mode
These bits select the waveform generation operation. They affect the top value, as shown in Waveform Output Operations. They also control whether frequency or PWM waveform generation should be used. The waveform generation operations are explained in Waveform Output Operations.

These bits are not synchronized.

Value	Name	Operation	Top Value	Output Waveform on Match	Output Waveform on Wraparound
0x0	NFRQ	Normal frequency	PER[1] / Max	Toggle	No action
0x1	MFRQ	Match frequency	CC0	Toggle	No action
0x2	NPWM	Normal PWM	PER[1] / Max	Set	Clear
0x3	MPWM	Match PWM	CC0	Set	Clear

1) This depends on the TC mode: In 8-bit mode, the top value is the Period Value register (PER). In 16- and 32-bit mode it is the respective MAX value.

35.7.3.10 Driver Control

38.6.2.3 Operation

In the most basic configuration, the ADC samples values from the configured internal or external sources (INPUTCTRL register). The rate of the conversion depends on the combination of the GCLK_ADCx frequency and the clock prescaler.

To convert analog values to digital values, the ADC needs to be initialized first, as described in the Initialization section. Data conversion can be started either manually by setting the Start bit in the Software Trigger register (SWTRIG.START=1), or automatically by configuring an automatic trigger to initiate the conversions. A free-running mode can be used to continuously convert an input channel. When using free-running mode the first conversion must be started, while subsequent conversions will start automatically at the end of previous conversions.

The result of the conversion is stored in the Result register (RESULT) overwriting the result from the previous conversion.

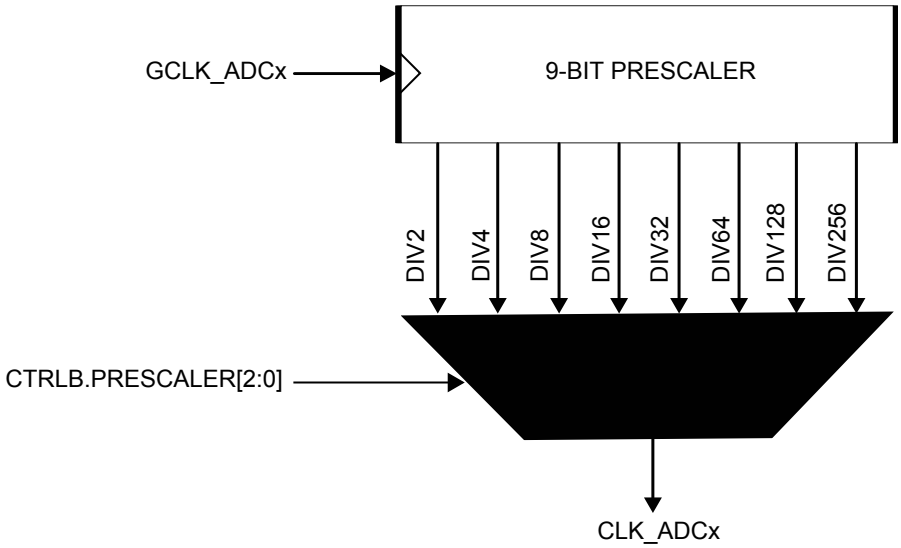
To avoid data loss if more than one channel is enabled, the conversion result must be read as soon as it is available (INTFLAG.RESRDY). Failing to do so will result in an overrun error condition, indicated by the OVERRUN bit in the Interrupt Flag Status and Clear register (INTFLAG.OVERRUN).

To enable one of the available interrupts sources, the corresponding bit in the Interrupt Enable Set register (INTENSET) must be written to '1'.

38.6.2.4 Prescaler Selection

The ADC is clocked by GCLK_ADCx. There is also a prescaler in the ADC to enable conversion at lower clock rates. Refer to CTRLB for details on prescaler settings. Refer to Conversion Timing and Sampling Rate for details on timing and sampling rate.

Figure 38-2. ADC Prescaler



Note: The minimum prescaling factor is DIV2.

38.6.2.5 Reference Configuration

The ADC has various sources for its reference voltage V_{REF}. The Reference Voltage Selection bit field in the Reference Control register (REFCTRL.REFSEL) determines which reference is selected. By default, the internal voltage reference INTREF is selected. Based on customer application requirements, the external or internal reference can be selected. Refer to REFCTRL.REFSEL for further details on available selections.

Related Links

REFCTRL

Number of Accumulated Samples	AVGCTRL. SAMPLENUM	Intermediate Result Precision	Number of Automatic Right Shifts	Division Factor	AVGCTRL.ADJRES	Total Number of Right Shifts	Final Result Precision	Automatic Division Factor
64	0x6	18	2	16	0x4	6	12 bits	4
128	0x7	19	3	16	0x4	7	12 bits	8
256	0x8	20	4	16	0x4	8	12 bits	16
512	0x9	21	5	16	0x4	9	12 bits	32
1024	0xA	22	6	16	0x4	10	12 bits	64
Reserved	0xB –0xF				0x0		12 bits	0

38.6.2.11 Oversampling and Decimation

By using oversampling and decimation, the ADC resolution can be increased from 12 bits up to 16 bits, for the cost of reduced effective sampling rate.

To increase the resolution by n bits, 4^n samples must be accumulated. The result must then be right-shifted by n bits. This right-shift is a combination of the automatic right-shift and the value written to AVGCTRL.ADJRES. To obtain the correct resolution, the ADJRES must be configured as described in the table below. This method will result in n bit extra LSB resolution.

Table 38-3. Configuration Required for Oversampling and Decimation

Result Resolution	Number of Samples to Average	AVGCTRL.SAMPLENUM[3:0]	Number of Automatic Right Shifts	AVGCTRL.ADJRES[2:0]
13 bits	$4^1 = 4$	0x2	0	0x1
14 bits	$4^2 = 16$	0x4	0	0x2
15 bits	$4^3 = 64$	0x6	2	0x1
16 bits	$4^4 = 256$	0x8	4	0x0

38.6.2.12 Automatic Sequences

The ADC has the ability to automatically sequence a series of conversions. This means that each time the ADC receives a start-of-conversion request, it can perform multiple conversions automatically. All of the 32 positive inputs can be included in a sequence by writing to corresponding bits in the Sequence Control register (SEQCTRL). The order of the conversion in a sequence is the lower positive MUX selection to upper positive MUX (AIN0, AIN1, AIN2 ...). In differential mode, the negative inputs selected by MUXNEG field, will be used for the entire sequence.

When a sequence starts, the Sequence Busy status bit in Sequence Status register (SEQSTATUS.SEQBUSY) will be set. When the sequence is complete, the Sequence Busy status bit will be cleared.

Each time a conversion is completed, the Sequence State bit in Sequence Status register (SEQSTATUS.SEQSTATE) will store the input number from which the conversion is done. The result will be stored in the RESULT register, and the Result Ready Interrupt Flag (INTFLAG.RESRDY) is set.

If additional inputs must be scanned, the ADC will automatically start a new conversion on the next input present in the sequence list.

Note that if SEQCTRL register has no bits set to '1', the conversion is done with the selected MUXPOS input.

39. SDADC – Sigma-Delta Analog-to-Digital Converter

39.1 Overview

The Sigma-Delta Analog-to-Digital Converter (SDADC) converts analog signals to digital values. The SDADC has 16-bit resolution, and is capable of converting up to 1.5 Msps divided by the data over sampling ratio (OSR). The input selection is up to three differential analog channels. The SDADC provides signed results.

ADC measurements can be started by either application software or an incoming event from another peripheral in the device. ADC measurements can be started with predictable timing, and without software intervention.

The SDADC also integrates a sleep mode and a conversion sequencer. These features reduce power consumption and processor intervention.

A set of reference voltages is generated internally.

39.2 Features

- 16-bit resolution
- Up to 1,500,000 divided by Over Sampling Ratio (OSR) samples per second
- Three analog differential inputs
  - Up to 3 external analog differential pairs.
- Conversion Range:
  - Differential mode: $-V_{REF}$ to $+V_{REF}$
  - Single-ended mode: 0V to $+V_{REF}$
- Event-triggered conversion (one event input)
- Optional DMA transfer of conversion settings or result
- Single, continuous and sequencing options
- Hardware gain, offset and shift compensation
- Windowing monitor
- Chopper mode (offset reduction)

39.6.2.2 Enabling, Disabling and Resetting

The SDADC is enabled by writing a one to the Enable bit in the Control A register (CTRLA.ENABLE). The SDADC is disabled by writing a zero to CTRLA.ENABLE.

The SDADC is reset by writing a one to the Software Reset bit in the Control A register (CTRLA.SWRST). All registers in the ADC will be reset to their initial state, and the SDADC will be disabled. Refer to CTRLA for details.

39.6.2.3 Operation

In the most basic configuration, the SDADC sample values from the configured external sources (input ctrl register). The rate of the conversion depends on the combination of the GCLK_SDADC frequency, the clock prescaler from CTRLB.PRESCALER and the Over Sampling Ratio from CTRLB.OSR.

To convert analog values to digital values, the SDADC needs to be initialized first, as described in Initialization . Data conversion can be started either manually, by writing a one to the Start bit in the Software Trigger register (SWTRIG.START), or automatically, by configuring an automatic trigger to initiate the conversions. A free-running mode could be used to continuously convert an input channel. There is no need for a trigger to start the conversion. It will start automatically at the end of previous conversion.

The first valid sample starts from the third sample onward. It can skip the first few samples by programming the SKPCNT[3:0] in CTRLB register. The result of the conversion is stored in the Result register (RESULT) overwriting the result from the previous conversion.

To avoid data loss the conversion result must be read as soon as it is available (INTFLAG.RESRDY). Failing to do so will result in an overrun error condition, indicated by the OVERRUN bit in the Interrupt Flag Status and Clear register (INTFLAG.OVERRUN).

To use an interrupt handler, the corresponding bit in the Interrupt Enable Set register (INTENSET) must be written to one.

39.6.2.4 Conversion Reference

The conversion is performed on a full range between 0V and the reference voltage. Analog inputs between these voltages convert to values based on a linear conversion.

39.6.2.5 Prescaler Selection

The SDADC is clocked by GCLK_SDADC. There is also a prescaler in the SDADC to enable conversion at lower clock rates.

Refer to CTRLB for details on prescaler settings.

Bit	7	6	5	4	3	2	1	0
							ENABLE	SWRST
Access							R/W	R/W
Reset							0	0

Bit 1 – ENABLE: Enable
Due to synchronization there is delay from writing CTRLA.ENABLE until the peripheral is enabled/disabled. The value written to CTRLA.ENABLE will read back immediately and the ENABLE bit in the Synchronization Busy register (SYNCBUSY.ENABLE) will be set. SYNCBUSY.ENABLE will be cleared when the operation is complete.

This bit is not enable-protected.

Value	Description
0	The peripheral is disabled.
1	The peripheral is enabled.

Bit 0 – SWRST: Software Reset
Writing a '0' to this bit has no effect.

Writing a '1' to this bit resets all registers in the FREQM to their initial state, and the FREQM will be disabled. Writing a '1' to this bit will always take precedence, meaning that all other writes in the same write-operation will be discarded.

Due to synchronization there is a delay from writing CTRLA.SWRST until the Reset is complete. CTRLA.SWRST and SYNCBUSY.SWRST will both be cleared when the Reset is complete.

This bit is not enable-protected.

Value	Description
0	There is no ongoing Reset operation.
1	The Reset operation is ongoing.

44.8.2 Control B

Name: CTRLB
Offset: 0x01 [ID-00000e03]
Reset: 0x00
Property: –

Bit	7	6	5	4	3	2	1	0
								START
Access								W
Reset								0

Bit 0 – START: Start Measurement

Value	Description
0	Writing a '0' has no effect.
1	Writing a '1' starts a measurement.

44.8.3 Configuration A

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
t_{MOH}	MOSI hold after SCK	Master, VDD>4.5V		2.5	-	-	ns
		Master, VDD>2.7V		2.5	-	-	
t_{SSCK}	Slave SCK Period	Slave	Reception	$2*(t_{SIS}+t_{MASTER\_OUT})$ (5)	-	-	ns
		Slave	Transmission	$2*(t_{SOV}+t_{MASTER\_IN})$ (6)	-	-	
t_{SSCKW}	SCK high/low width	Slave		-	$0.5*t_{SSCK}$	-	ns
t_{SSCKR}	SCK rise time (2)	Slave		-	$0.25*t_{SSCK}$	-	ns
t_{SSCKF}	SCK fall time (2)	Slave		-	$0.25*t_{SSCK}$	-	ns
t_{SIS}	MOSI setup to SCK	Slave, VDD>4.5V		13.6	-	-	ns
		Slave, VDD>2.7V		14.1	-	-	
t_{SIH}	MOSI hold after SCK	Slave, VDD>4.5V		0	-	-	ns
		Slave, VDD>2.7V		0	-	-	
t_{SSS}	SS setup to SCK	Slave	PRELOADEN=1	$t_{SOSS}+t_{EXT\_MIS}+2*t_{APBC}$ (8) (9)	-	-	ns
			PRELOADEN=0	$t_{SOSS}+t_{EXT\_MIS}$ (8)	-	-	
t_{SSH}	SS hold after SCK	Slave		$0.5*t_{SSCK}$	-	-	ns
t_{SOV}	MISO output valid SCK	Slave, VDD>4.5V		-	-	45	ns
		Slave, VDD>2.7V	-	-	55.1		
t_{SOH}	MISO hold after SCK	Slave, VDD>4.5V		11.9	-	-	ns
		Slave, VDD>2.7V	11.9	-	-		
t_{SOSS}	MISO setup after SS low	Slave, VDD>4.5V		-	-	41	ns
		Slave, VDD>2.7V		-	-	50.7	
t_{SOSH}	MISO hold after SS high	Slave, VDD>4.5V		11.1	-	-	ns
		Slave, VDD>2.7V		11.1	-	-	

1. These values are based on simulation. These values are not covered by test limits in production.
2. See I/O pin characteristics.
3. Where t_{SLAVE_OUT} is the slave external device output response time, generally $t_{EXT\_SOV}+t_{LINE\_DELAY}$ (7).
4. Where t_{SLAVE_IN} is the slave external device input constraint, generally $t_{EXT\_SIS}+t_{LINE\_DELAY}$ (7).
5. Where t_{MASTER_OUT} is the master external device output response time, generally $t_{EXT\_MOV}+t_{LINE\_DELAY}$ (7).
6. Where t_{MASTER_IN} is the master external device input constraint, generally $t_{EXT\_MIS}+t_{LINE\_DELAY}$ (7).
7. t_{LINE_DELAY} is the transmission line time delay.
8. t_{EXT_MIS} is the input constraint for the master external device.
9. t_{APBC} is the APB period for SERCOM.

Figure 45-7. SPI Timing Requirements in Master Mode

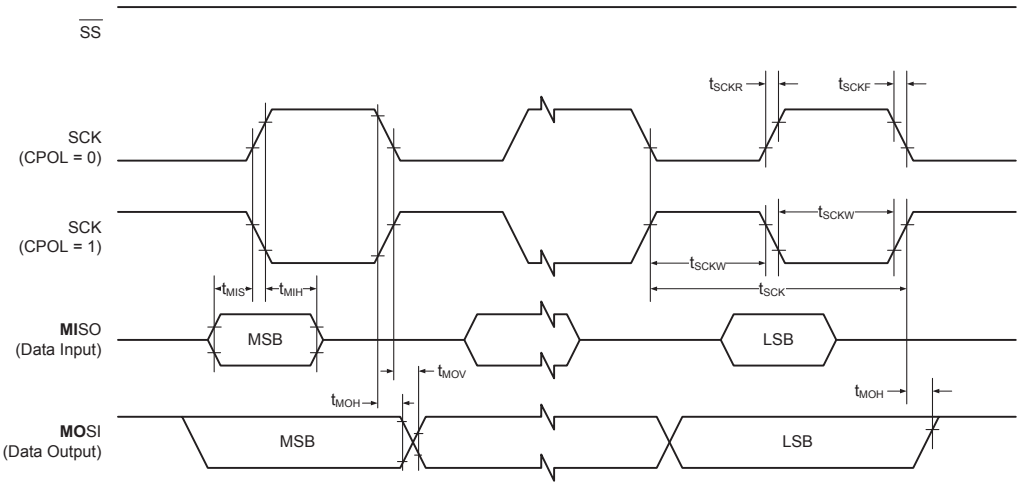
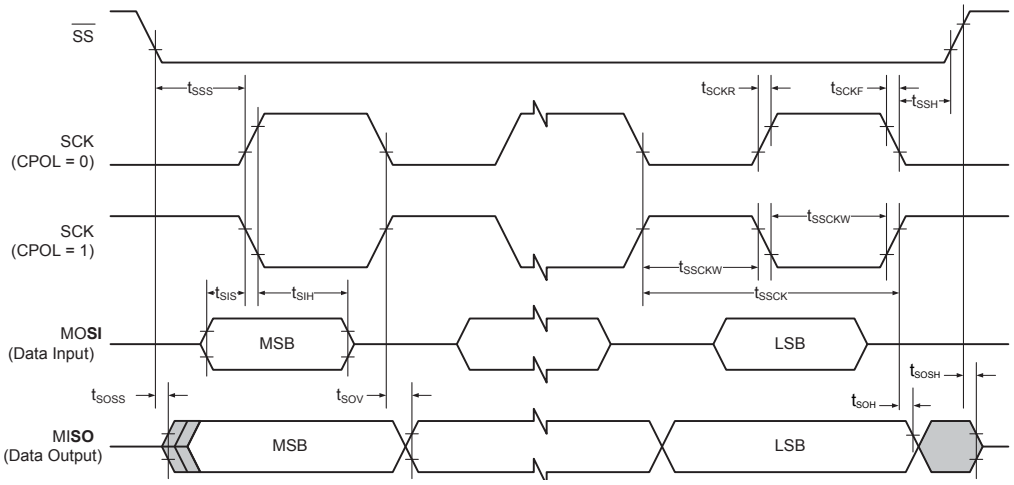


Figure 45-8. SPI Timing Requirements in Slave Mode



45.13.2 External Reset

Table 45-53. External Reset Characteristics(1)

Symbol	Parameter	Min.	Units
t_{EXT}	Minimum reset pulse width	1	µs

1. These are based on simulation. These values are not covered by test or characterization

45.13.3 CAN Timing

Table 45-54. CAN Physical Layer Timing(1)

Parameter	Conditions	Max.	Units
TX_{CAN} output delay	VDD = 2.7V Load = 20pF	13.9	ns

Figure 49-4. External Analog Reference Schematic With One Reference

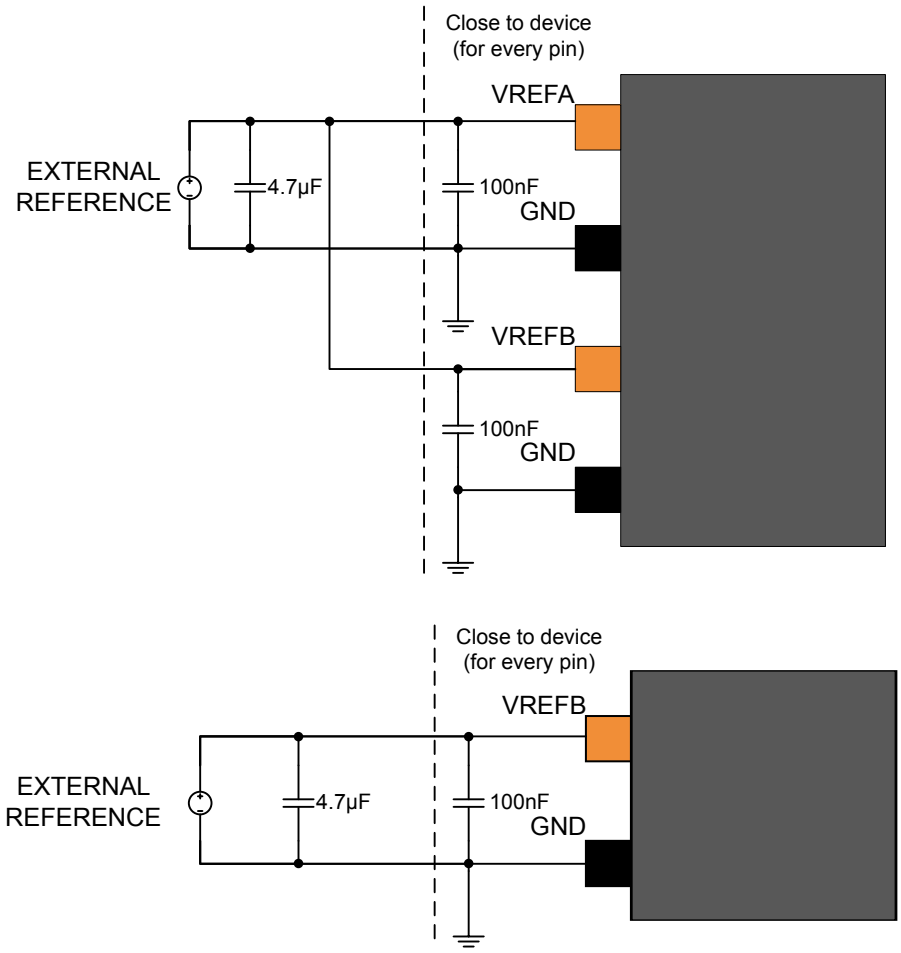


Table 49-2. External Analog Reference Connections

Signal Name	Recommended Pin Connection	Description
VREFA	2.0V to V_{DDANA} - 0.6V for ADC 1.0V to V_{DDANA} - 0.6V for DAC Decoupling/filtering capacitors: 100nF(1)(2) and 4.7µF(1)	External reference from VREFA pin on the analog port.
VREFB	1.0V to 5.5V for SDADC Decoupling/filtering capacitors: 100nF(1)(2) and 4.7µF(1)	External reference from VREFB pin on the analog port.
GND		Ground

Note:

1. These values are given as a typical example.
2. Decoupling capacitor should be placed close to the device for each supply pin pair in the signal group.