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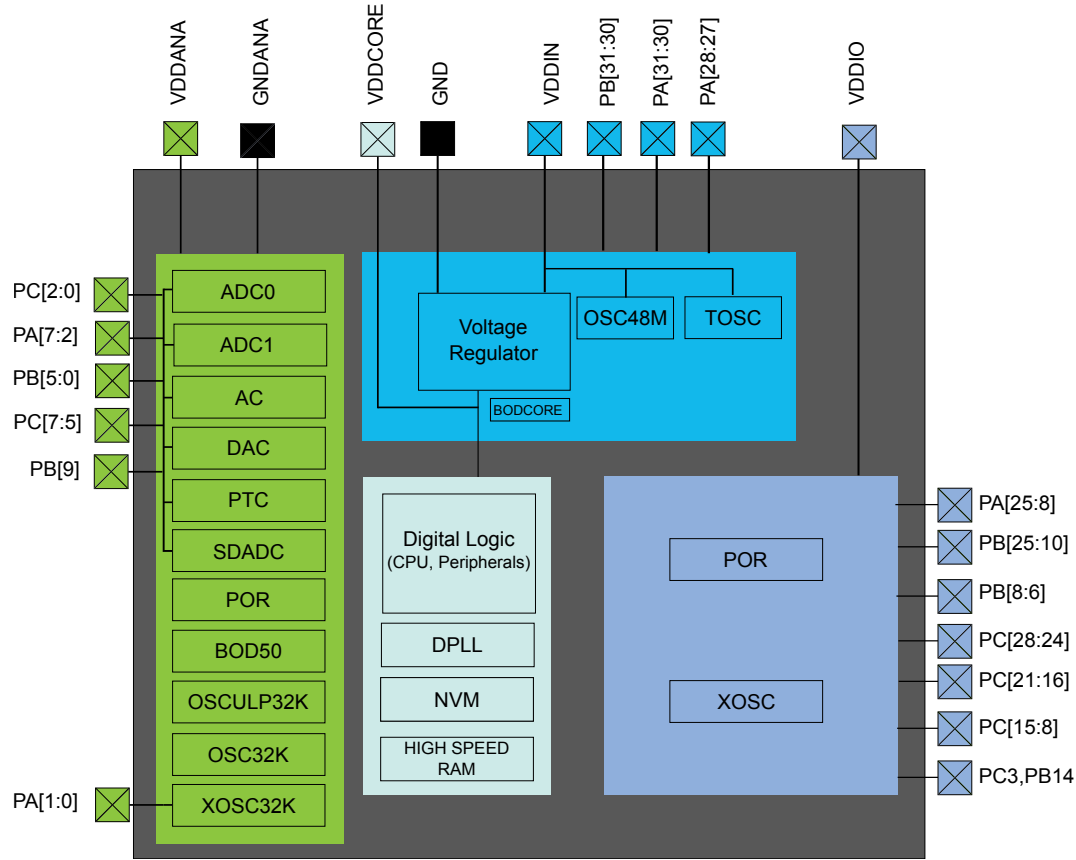
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, WDT
Number of I/O	84
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamc20n18a-ant

Figure 7-2. Power Domain Overview, SAM C20/C21 N



7.2 Power Supply Considerations

7.2.1 Power Supplies, SAM C21/SAM C20

The SAM C21 has the following power supply pins:

- VDDIO: Powers I/O lines and XOSC. Voltage is 2.70V to 5.50V.
- VDDIN: Powers I/O lines and the OSC48M, TOSC and internal regulator. Voltage is 2.70V to 5.50V.
- VDDANA: Powers I/O lines and the ADC, AC, DAC, PTC, SDADC, OSCULP32K, OSC32K, and XOSC32K. Voltage is 2.70V to 5.50V.
- VDDCORE: Internal regulated voltage output. Powers the core, memories, peripherals, and FDPLL96M. Voltage is 1.2V typical.

The same voltage must be applied to both the VDDIN and VDDANA pins. This common voltage is referred to as V_{DD} in the datasheet. VDDIO must always be less than or equal to VDDIN.

The ground pins, GND, are common to VDDCORE, VDDIO and VDDIN. The ground pin for VDDANA is GNDANA.

For decoupling recommendations for the different power supplies, refer to the schematic checklist.

The SAM C20 has the following power supply pins:

- VDDIO: Powers I/O lines and XOSC. Voltage is 2.70V to 5.50V.
- VDDIN: Powers I/O lines and the OSC48M, TOSC and internal regulator. Voltage is 2.70V to 5.50V.

Bit Position	Name	Description
40:19	CAL48M 5V	OSC48M Calibration: VDD range 3.6V to 5.5V. Should be written to the CAL48M register.
62:41	CAL48M 3V3	OSC48M Calibration: VDD range 2.7V to 3.6V. Should be written to the CAL48M register.
63	Reserved	

Table 9-6. SAM C20 NVM Software Calibration Area Mapping

Bit Position	Name	Description
2:0	ADC0 LINEARITY	ADC0 Linearity Calibration. Should be written to the CALIB register.
5:3	ADC0 BIASCAL	ADC0 Bias Calibration. Should be written to the CALIB register.
11:6	Reserved	
18:12	OSC32K CAL	OSC32K Calibration. Should be written to OSC32K register.
40:19	CAL48M 5V	OSC48M Calibration: VDD range 3.6V to 5.5V. Should be written to the CAL48M register.
62:41	CAL48M 3V3	OSC48M Calibration: VDD range 2.7V to 3.6V. Should be written to the CAL48M register.
63	Reserved	

Related Links

[CAL48M](#)

9.5 NVM Temperature Calibration Area Mapping, SAM C21

The NVM Temperature Calibration Area contains calibration data that are measured and written during production test. These calibration values should be read by the application software and written back to the corresponding register.

The NVM Temperature Calibration Area can be read at address 0x806030.

The NVM Temperature Calibration Area can not be written.

Table 9-7. NVM Temperature Calibration Area Mapping, SAM C21

Bit Position	Name	Description
5:0	TSENS TCAL	TSENS Temperature Calibration. Should be written to the TSENS CAL register.
11:6	TSENS FCAL	TSENS Frequency Calibration. Should be written to the TSENS CAL register.
35:12	TSENS GAIN	TSENS Gain Calibration. Should be written to the TSENS GAIN register.

16.5.3 Clocks

The GCLK bus clock (CLK_GCLK_APB) can be enabled and disabled in the Main Clock Controller.

Related Links

[Peripheral Clock Masking](#)

[OSC32KCTRL – 32KHz Oscillators Controller](#)

16.5.4 DMA

Not applicable.

16.5.5 Interrupts

Not applicable.

16.5.6 Events

Not applicable.

16.5.7 Debug Operation

When the CPU is halted in debug mode the GCLK continues normal operation. If the GCLK is configured in a way that requires it to be periodically serviced by the CPU through interrupts or similar, improper operation or data loss may result during debugging.

16.5.8 Register Access Protection

All registers with write-access can be optionally write-protected by the Peripheral Access Controller (PAC).

Note: Optional write-protection is indicated by the "PAC Write-Protection" property in the register description.

When the CPU is halted in debug mode, all write-protection is automatically disabled. Write-protection does not apply for accesses through an external debugger.

Related Links

[PAC - Peripheral Access Controller](#)

16.5.9 Analog Connections

Not applicable.

16.6 Functional Description**16.6.1 Principle of Operation**

The GCLK module is comprised of nine Generic Clock Generators (Generators) sourcing up to 64 Peripheral Channels and the Main Clock signal GCLK_MAIN.

A clock source selected as input to a Generator can either be used directly, or it can be prescaled in the Generator. A generator output is used by one or more Peripheral Channels to provide a peripheral generic clock signal (GCLK_PERIPH) to the peripherals.

16.6.2 Basic Operation**16.6.2.1 Initialization**

Before a Generator is enabled, the corresponding clock source should be enabled. The Peripheral clock must be configured as outlined by the following steps:

Offset	Name	Bit Pos.								
0x41		15:8			RUNSTDBY	DIVSEL	OE	OOV	IDC	GENEN
0x42		23:16	DIV[7:0]							
0x43		31:24	DIV[15:8]							
0x44 ... 0x7F	Reserved									
0x80	PCHCTRL0	7:0	WRTLOCK	CHEN			GEN[3:0]			
0x81		15:8								
0x82		23:16								
0x83		31:24								
0x84	PCHCTRL1	7:0	WRTLOCK	CHEN			GEN[3:0]			
0x85		15:8								
0x86		23:16								
0x87		31:24								
0x88	PCHCTRL2	7:0	WRTLOCK	CHEN			GEN[3:0]			
0x89		15:8								
0x8A		23:16								
0x8B		31:24								
0x8C	PCHCTRL3	7:0	WRTLOCK	CHEN			GEN[3:0]			
0x8D		15:8								
0x8E		23:16								
0x8F		31:24								
0x90	PCHCTRL4	7:0	WRTLOCK	CHEN			GEN[3:0]			
0x91		15:8								
0x92		23:16								
0x93		31:24								
0x94	PCHCTRL5	7:0	WRTLOCK	CHEN			GEN[3:0]			
0x95		15:8								
0x96		23:16								
0x97		31:24								
0x98	PCHCTRL6	7:0	WRTLOCK	CHEN			GEN[3:0]			
0x99		15:8								
0x9A		23:16								
0x9B		31:24								
0x9C	PCHCTRL7	7:0	WRTLOCK	CHEN			GEN[3:0]			
0x9D		15:8								
0x9E		23:16								
0x9F		31:24								
0xA0	PCHCTRL8	7:0	WRTLOCK	CHEN			GEN[3:0]			
0xA1		15:8								
0xA2		23:16								
0xA3		31:24								
0xA4	PCHCTRL9	7:0	WRTLOCK	CHEN			GEN[3:0]			
0xA5		15:8								
0xA6		23:16								
0xA7		31:24								
0xA8	PCHCTRL10	7:0	WRTLOCK	CHEN			GEN[3:0]			

Bit	31	30	29	28	27	26	25	24
	DIV[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	DIV[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
			RUNSTDBY	DIVSEL	OE	OOV	IDC	GENEN
Access								
Reset			0	0	0	0	0	1
Bit	7	6	5	4	3	2	1	0
				SRC[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 31:16 – DIV[15:0]: Division Factor

These bits represent a division value for the corresponding Generator. The actual division factor is dependent on the state of DIVSEL. The number of relevant DIV bits for each Generator can be seen in this table. Written bits outside of the specified range will be ignored.

Table 16-3. Division Factor Bits

Generic Clock Generator	Division Factor Bits
Generator 0	8 division factor bits - DIV[7:0]
Generator 1	16 division factor bits - DIV[15:0]
Generator 2-11	8 division factor bits - DIV[4:0]

Bit 13 – RUNSTDBY: Run in Standby

This bit is used to keep the Generator running in Standby as long as it is configured to output to a dedicated GCLK_IO pin. If GENCTRLn.OE is zero, this bit has no effect and the generator will only be running if a peripheral requires the clock.

Value	Description
0	The Generator is stopped in Standby and the GCLK_IO pin state (one or zero) will be dependent on the setting in GENCTRL.OOV.
1	The Generator is kept running and output to its dedicated GCLK_IO pin during Standby mode.

Bit 12 – DIVSEL: Divide Selection

This bit determines how the division factor of the clock source of the Generator will be calculated from DIV. If the clock source should not be divided, DIVSEL must be 0 and the GENCTRLn.DIV value must be either 0 or 1.

Table 21-1. XOSC32K Sleep Behavior

CPU Mode	XOSC32K. RUNSTDBY	XOSC32K. ONDEMAND	Sleep Behavior of XOSC32K and CFD
Active or Idle	-	0	Always run
Active or Idle	-	1	Run if requested by peripheral
Standby	1	0	Always run
Standby	1	1	Run if requested by peripheral
Standby	0	-	Run if requested by peripheral

As a crystal oscillator usually requires a very long start-up time, the 32KHz External Crystal Oscillator will keep running across resets when XOSC32K.ONDEMAND=0, except for power-on reset (POR). After a reset or when waking up from a sleep mode where the XOSC32K was disabled, the XOSC32K will need a certain amount of time to stabilize on the correct frequency. This start-up time can be configured by changing the Oscillator Start-Up Time bit group (XOSC32K.STARTUP) in the 32KHz External Crystal Oscillator Control register. During the start-up time, the oscillator output is masked to ensure that no unstable clock propagates to the digital logic.

Once the external clock or crystal oscillator is stable and ready to be used as a clock source, the XOSC32K Ready bit in the Status register is set (STATUS.XOSC32KRDY=1). The transition of STATUS.XOSC32KRDY from '0' to '1' generates an interrupt if the XOSC32K Ready bit in the Interrupt Enable Set register is set (INTENSET.XOSC32KRDY=1).

The XOSC32K can be used as a source for Generic Clock Generators (GCLK) or for the Real-Time Counter (RTC). Before enabling the GCLK or the RTC module, the corresponding oscillator output must be enabled (XOSC32K.EN32K or XOSC32K.EN1K) in order to ensure proper operation. In the same way, the GCLK or RTC modules must be disabled before the clock selection is changed. For details on RTC clock configuration, refer also to [Real-Time Counter Clock Selection](#).

Related Links

[GCLK - Generic Clock Controller](#)

[RTC – Real-Time Counter](#)

21.6.3 Clock Failure Detection Operation

The Clock Failure Detector (CFD) allows the user to monitor the external clock or crystal oscillator signal provided by the external oscillator (XOSC32K). The CFD detects failing operation of the XOSC32K clock with reduced latency, and allows to switch to a safe clock source in case of clock failure. The user can also switch from the safe clock back to XOSC32K in case of recovery. The safe clock is derived from the OSCULP32K oscillator with a configurable prescaler. This allows to configure the safe clock in order to fulfill the operative conditions of the microcontroller.

In sleep modes, CFD operation is automatically disabled when the external oscillator is not requested to run by a peripheral. See the Sleep Behavior table above when this is the case.

The user interface registers allow to enable, disable, and configure the CFD. The Status register provides status flags on failure and clock switch conditions. The CFD can optionally trigger an interrupt or an event when a failure is detected.

22.8.1 Interrupt Enable Clear

This register allows the user to disable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Set register (INTENSET).

Name: INTENCLR
Offset: 0x00 [ID-00001e33]
Reset: 0x00000000
Property: PAC Write-Protection

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
						BVDDSRDY	BODVDDDET	BODVDDRDY
Access						R/W	R/W	R/W
Reset						0	0	0

Bit 2 – BVDDSRDY: BODVDD Synchronization Ready Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the BODVDD Synchronization Ready Interrupt Enable bit, which disables the BODVDD Synchronization Ready interrupt.

Value	Description
0	The BODVDD Synchronization Ready interrupt is disabled.
1	The BODVDD Synchronization Ready interrupt is enabled, and an interrupt request will be generated when the BODVDD Synchronization Ready Interrupt flag is set.

Bit 1 – BODVDDDET: BODVDD Detection Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the BODVDD Detection Interrupt Enable bit, which disables the BODVDD Detection interrupt.

Value	Description
0	The BODVDD Detection interrupt is disabled.
1	The BODVDD Detection interrupt is enabled, and an interrupt request will be generated when the BODVDD Detection Interrupt flag is set.

Name: INTENSET
Offset: 0x0A
Reset: 0x0000
Property: PAC Write-Protection

Bit	15	14	13	12	11	10	9	8
	OVF							ALARM0
Access	R/W							R/W
Reset	0							0

Bit	7	6	5	4	3	2	1	0
	PERn	PERn	PERn	PERn	PERn	PERn	PERn	PERn
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – OVF: Overflow Interrupt Enable

Writing a '0' to this bit has no effect. Writing a '1' to this bit will set the Overflow Interrupt Enable bit, which enables the Overflow interrupt.

Value	Description
0	The Overflow interrupt is disabled.
1	The Overflow interrupt is enabled.

Bit 8 – ALARM0: Alarm 0 Interrupt Enable

Writing a '0' to this bit has no effect. Writing a '1' to this bit will set the Alarm 0 Interrupt Enable bit, which enables the Alarm 0 interrupt.

Value	Description
0	The Alarm 0 interrupt is disabled.
1	The Alarm 0 interrupt is enabled.

Bits 7:0 – PERn: Periodic Interval n Interrupt Enable [n = 7..0]

Writing a '0' to this bit has no effect. Writing a '1' to this bit will set the Periodic Interval n Interrupt Enable bit, which enables the Periodic Interval n interrupt.

Value	Description
0	Periodic Interval n interrupt is disabled.
1	Periodic Interval n interrupt is enabled.

24.12.5 Interrupt Flag Status and Clear in Clock/Calendar mode (CTRLA.MODE=2)

Name: INTFLAG
Offset: 0x0C
Reset: 0x0000
Property: -

The corresponding DMAC Enable bit in the Control register is cleared (CTRL.DMAENABLE=0) when the entire DMAC module is disabled.

25.6.3.7 CRC Operation

A cyclic redundancy check (CRC) is an error detection technique used to find errors in data. It is commonly used to determine whether the data during a transmission, or data present in data and program memories has been corrupted or not. A CRC takes a data stream or a block of data as input and generates a 16- or 32-bit output that can be appended to the data and used as a checksum.

When the data is received, the device or application repeats the calculation: If the new CRC result does not match the one calculated earlier, the block contains a data error. The application will then detect this and may take a corrective action, such as requesting the data to be sent again or simply not using the incorrect data.

The CRC engine in DMAC supports two commonly used CRC polynomials: CRC-16 (CRC-CCITT) and CRC-32 (IEEE 802.3). Typically, applying CRC-n (CRC-16 or CRC-32) to a data block of arbitrary length will detect any single alteration that is $\leq n$ bits in length, and will detect the fraction $1-2^{-n}$ of all longer error bursts.

- CRC-16:
 - Polynomial: $x^{16} + x^{12} + x^5 + 1$
 - Hex value: 0x1021
- CRC-32:
 - Polynomial: $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$
 - Hex value: 0x04C11DB7

The data source for the CRC engine can either be one of the DMA channels or the APB bus interface, and must be selected by writing to the CRC Input Source bits in the CRC Control register (CRCCTRL.CRCSRC). The CRC engine then takes data input from the selected source and generates a checksum based on these data. The checksum is available in the CRC Checksum register (CRCCHKSUM). When CRC-32 polynomial is used, the final checksum read is bit reversed and complemented, as shown in [Figure 25-16](#).

The CRC polynomial is selected by writing to the CRC Polynomial Type bit in the CRC Control register (CRCCTRL.CRCPOLY), the default is CRC-16. The CRC engine operates on byte only. When the DMA is used as data source for the CRC engine, the DMA channel beat size setting will be used. When used with APB bus interface, the application must select the CRC Beat Size bit field of CRC Control register (CRCCTRL.CRCBEATSIZE). 8-, 16-, or 32-bit bus transfer access type is supported. The corresponding number of bytes will be written in the [CRCDATAIN](#) register and the CRC engine will operate on the input data in a byte by byte manner.

Bit	31	30	29	28	27	26	25	24
	EXTINT[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	EXTINT[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	EXTINT[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	EXTINT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – EXTINT[31:0]: External Interrupt Enable

The bit x of EXTINT enables the interrupt associated with the EXTINTx pin.

Writing a '0' to bit x has no effect.

Writing a '1' to bit x will set the External Interrupt Enable bit x, which enables the external interrupt EXTINTx.

Value	Description
0	The external interrupt x is disabled.
1	The external interrupt x is enabled.

26.8.8 Interrupt Flag Status and Clear

Name: INTFLAG
Offset: 0x14
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
						ACKACT	CMD[1:0]	
Access						R/W	R/W	R/W
Reset						0	0	0
Bit	15	14	13	12	11	10	9	8
	AMODE[1:0]					AACKEN	GCMD	SMEN
Access	R/W	R/W				R/W	R/W	R/W
Reset	0	0				0	0	0
Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bit 18 – ACKACT: Acknowledge Action

This bit defines the slave's acknowledge behavior after an address or data byte is received from the master. The acknowledge action is executed when a command is written to the CMD bits. If smart mode is enabled (CTRLB.SMEN=1), the acknowledge action is performed when the DATA register is read.

This bit is not enable-protected.

Value	Description
0	Send ACK
1	Send NACK

Bits 17:16 – CMD[1:0]: Command

This bit field triggers the slave operation as the below. The CMD bits are strobe bits, and always read as zero. The operation is dependent on the slave interrupt flags, INTFLAG.DRDY and INTFLAG.AMATCH, in addition to STATUS.DIR.

All interrupt flags (INTFLAG.DRDY, INTFLAG.AMATCH and INTFLAG.PREC) are automatically cleared when a command is given.

This bit is not enable-protected.

Table 33-3. Command Description

CMD[1:0]	DIR	Action
0x0	X	(No action)
0x1	X	(Reserved)
0x2	Used to complete a transaction in response to a data interrupt (DRDY)	
	0 (Master write)	Execute acknowledge action succeeded by waiting for any start (S/Sr) condition
	1 (Master read)	Wait for any start (S/Sr) condition

To leave low power mode, CLK_CANx_APB and GCLK_CANx must be active before writing CCCR.CSR to '0'. The CAN will acknowledge this by resetting CCCR.CSA = 0. Afterwards, the application can restart CAN communication by resetting bit CCCR.INIT.

34.6.10 Synchronization

Due to the asynchronicity between the main clock domain (CLK_CAN_APB) and the peripheral clock domain (GCLK_CAN) some registers are synchronized when written. When a write-synchronized register is written, the read back value will not be updated until the register has completed synchronization.

The following bits and registers are write-synchronized:

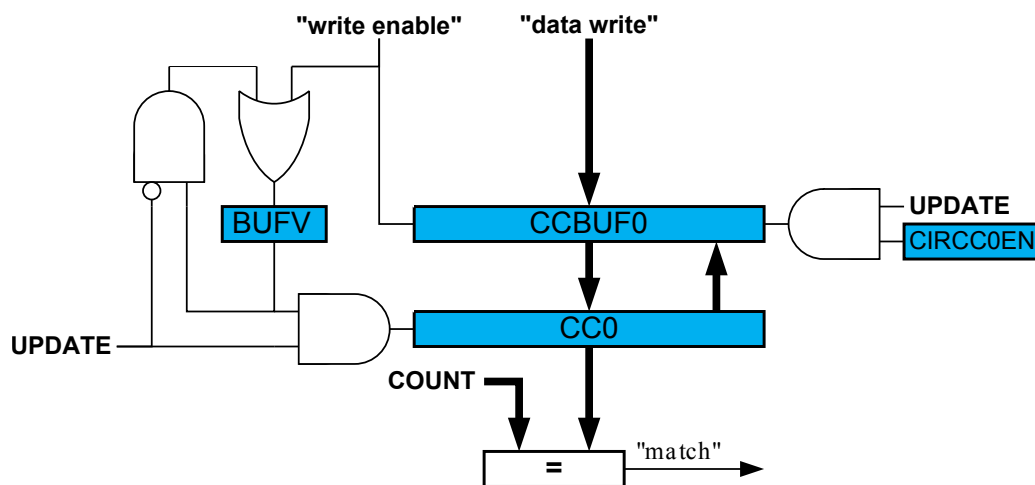
I Initialization bit in CC Control register (CCCR.INIT)

One-shot operation can be enabled by writing a '1' to the One-Shot bit in the Control B Set register (CTRLBSET.ONESHOT) and disabled by writing a '1' to CTRLBCLR.ONESHOT. When enabled, the TCC will count until an overflow or underflow occurs and stop counting. The one-shot operation can be restarted by a re-trigger software command, a re-trigger event or a start event. When the counter restarts its operation, STATUS.STOP is automatically cleared.

36.6.3.2 Circular Buffer

The Period register (PER) and the compare channels register (CC0 to CC3) support circular buffer operation. When circular buffer operation is enabled, the PER or CCx values are copied into the corresponding buffer registers at each update condition. Circular buffering is dedicated to RAMP2, RAMP2A, and DSBOTH operations.

Figure 36-17. Circular Buffer on Channel 0



36.6.3.3 Dithering Operation

The TCC supports dithering on Pulse-width or Period on a 16, 32 or 64 PWM cycles frame.

Dithering consists in adding some extra clocks cycles in a frame of several PWM cycles, and can improve the accuracy of the *average* output pulse width and period. The extra clock cycles are added on some of the compare match signals, one at a time, through a "blue noise" process that minimizes the flickering on the resulting dither patterns.

Dithering is enabled by writing the corresponding configuration in the Enhanced Resolution bits in CTRLA register (CTRLA.RESOLUTION):

- DITH4 enable dithering every 16 PWM frames
- DITH5 enable dithering every 32 PWM frames
- DITH6 enable dithering every 64 PWM frames

The DITHERCY bits of COUNT, PER and CCx define the number of extra cycles to add into the frame (DITHERCY bits from the respective COUNT, PER or CCx registers). The remaining bits of COUNT, PER, CCx define the compare value itself.

The pseudo code, giving the extra cycles insertion regarding the cycle is:

```
int extra_cycle(resolution, dithercy, cycle){
    int MASK;
    int value
    switch (resolution){
        DITH4: MASK = 0x0f;
        DITH5: MASK = 0x1f;
        DITH6: MASK = 0x3f;
    }
}
```

Value	Name	Description
0x3	RAMP2C	Critical RAMP2 operation
0x4		

Bits 2:0 – WAVEGEN[2:0]: Waveform Generation Operation

These bits select the waveform generation operation. The settings impact the top value and control if frequency or PWM waveform generation should be used. These bits are not synchronized.

Value	Name	Description						
		Operation	Top	Update	Waveform Output On Match	Waveform Output On Update	OVFIF/Event Up Down	
0x0	NFRQ	Normal Frequency	PER	TOP/Zero	Toggle	Stable	TOP	Zero
0x1	MFRQ	Match Frequency	CC0	TOP/Zero	Toggle	Stable	TOP	Zero
0x2	NPWM	Normal PWM	PER	TOP/Zero	Set	Clear	TOP	Zero
0x3								
0x4	DSCRITICAL	Dual-slope PWM	PER	Zero	~DIR	Stable	–	Zero
0x5	DSBOTTOM	Dual-slope PWM	PER	Zero	~DIR	Stable	–	Zero
0x6	DSBOTH	Dual-slope PWM	PER	TOP & Zero	~DIR	Stable	TOP	Zero
0x7	DSTOP	Dual-slope PWM	PER	Zero	~DIR	Stable	TOP	–

36.8.17 Period Value

Name: PER
Offset: 0x40 [ID-00002e48]
Reset: 0xFFFFFFFF
Property: Write-Synchronized

Name: CTRL
Offset: 0x00 [ID-00000485]
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
		RUNSTDBY					ENABLE	SWRST
Access		R/W					R/W	W
Reset		0					0	0

Bit 6 – RUNSTDBY: Run in Standby

This bit indicates if the GCLK_CCL clock must be kept running in standby mode. The setting is ignored for configurations where the generic clock is not required. For details refer to [Sleep Mode Operation](#).

Value	Description
0	Generic clock is not required in standby sleep mode.
1	Generic clock is required in standby sleep mode.

Bit 1 – ENABLE: Enable

Value	Description
0	The peripheral is disabled.
1	The peripheral is enabled.

Bit 0 – SWRST: Software Reset

Writing a '0' to this bit has no effect.

Writing a '1' to this bit resets all registers in the CCL to their initial state.

Value	Description
0	There is no reset operation ongoing.
1	The reset operation is ongoing.

37.8.2 Sequential Control x

Name: SEQCTRL
Offset: 0x04 + n*0x01 [n=0..1]
Reset: 0x00
Property: PAC Write-Protection, Enable-Protected

Bit	7	6	5	4	3	2	1	0
					SEQSEL[3:0]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bits 3:0 – SEQSEL[3:0]: Sequential Selection

These bits select the sequential configuration:

Sequential Selection

Name: SHIFTCORR
Offset: 0x1A [ID-0000243d]
Reset: 0x00
Property: PAC Write-Protection, Write-Synchronized

Bit	7	6	5	4	3	2	1	0
					SHIFTCORR[3:0]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bits 3:0 – SHIFTCORR[3:0]: Shift Correction

A specific offset, gain and shift can be applied to SDADC by performing the following operation:

$$(RESULT + OFFSETCORR) * GAINCORR / 2^{SHIFTCORR}$$

39.8.17 Software Trigger

Name: SWTRIG
Offset: 0x1C [ID-0000243d]
Reset: 0x00
Property: PAC Write-Protection, Write-Synchronized

Bit	7	6	5	4	3	2	1	0
							START	FLUSH
Access							W	W
Reset							0	0

Bit 1 – START: SDADC Start Conversion

Writing a one to this bit will start a conversion or sequence. The bit is cleared by hardware when the conversion has started. Setting this bit when it is already set has no effect.

Writing this bit to zero will have no effect.

Bit 0 – FLUSH: SDADC Conversion Flush

Writing a one to this bit will flush the SDADC pipeline. A flush will restart the SDADC conversion and all conversions in progress will be aborted and lost. This bit is cleared until the SDADC has been flushed.

After the flush, the ADC will resume where it left off; i.e., if a conversion was pending, the ADC will start a new conversion.

Writing this bit to zero will have no effect.

39.8.18 Synchronization Busy

Name: SYNCBUSY
Offset: 0x20 [ID-0000243d]
Reset: 0x00000000
Property: -

PAC write-protection does not apply to accesses through an external debugger.

Related Links

[PAC - Peripheral Access Controller](#)

40.5.9 Analog Connections

Each comparator has up to four I/O pins that can be used as analog inputs. Each pair of comparators shares the same four pins. These pins must be configured for analog operation before using them as comparator inputs.

Any internal reference source, such as a bandgap voltage reference, or DAC must be configured and enabled prior to its use as a comparator input.

40.6 Functional Description**40.6.1 Principle of Operation**

Each comparator has one positive input and one negative input. Each positive input may be chosen from a selection of analog input pins. Each negative input may be chosen from a selection of both analog input pins and internal inputs, such as a bandgap voltage reference.

The digital output from the comparator is '1' when the difference between the positive and the negative input voltage is positive, and '0' otherwise.

The individual comparators can be used independently (normal mode) or paired to form a window comparison (window mode).

40.6.2 Basic Operation**40.6.2.1 Initialization**

Some registers are enable-protected, meaning they can only be written when the module is disabled.

The following register is enable-protected:

- Event Control register (EVCTRL)

Enable-protection is denoted by the "Enable-Protected" property in each individual register description.

40.6.2.2 Enabling, Disabling and Resetting

The AC is enabled by writing a '1' to the Enable bit in the Control A register (CTRLA.ENABLE). The AC is disabled writing a '0' to CTRLA.ENABLE.

The AC is reset by writing a '1' to the Software Reset bit in the Control A register (CTRLA.SWRST). All registers in the AC will be reset to their initial state, and the AC will be disabled. Refer to *CTRLA* for details.

40.6.2.3 Comparator Configuration

Each individual comparator must be configured by its respective Comparator Control register (COMPCTRLx) before that comparator is enabled. These settings cannot be changed while the comparator is enabled.

- Select the desired measurement mode with COMPCTRLx.SINGLE. See [Starting a Comparison](#) for more details.
- Select the desired hysteresis with COMPCTRLx.HYSTEN. See [Input Hysteresis](#) for more details.
- Select the comparator speed versus power with COMPCTRLx.SPEED. See [Propagation Delay vs. Power Consumption](#) for more details.

Name: CTRLB
Offset: 0x01
Reset: 0x00
Property: PAC Write-Protection, Write-Synchronized

Bit	7	6	5	4	3	2	1	0
					STARTx	STARTx	STARTx	STARTx
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bits 3,2,1,0 – STARTx: Comparator x Start Comparison

Writing a '0' to this field has no effect.

Writing a '1' to STARTx starts a single-shot comparison on COMPx if both the Single-Shot and Enable bits in the Comparator x Control Register are '1' (COMPCTRLx.SINGLE and COMPCTRLx.ENABLE). If comparator x is not implemented, or if it is not enabled in single-shot mode, Writing a '1' has no effect.

This bit always reads as zero.

40.8.3 Event Control

Name: EVCTRL
Offset: 0x02
Reset: 0x0000
Property: PAC Write-Protection, Enable-Protected

Bit	15	14	13	12	11	10	9	8
	INVEIx	INVEIx	INVEIx	INVEIx	COMPEIx	COMPEIx	COMPEIx	COMPEIx
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			WINEOx	WINEOx	COMPEOx	COMPEOx	COMPEOx	COMPEOx
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 15,14,13,12 – INVEIx: Inverted Event Input Enable x

Value	Description
0	Incoming event is not inverted for comparator x.
1	Incoming event is inverted for comparator x.

Bits 11,10,9,8 – COMPEIx: Comparator x Event Input

Note that several actions can be enabled for incoming events. If several events are connected to the peripheral, the enabled action will be taken for any of the incoming events. There is no way to tell which of the incoming events caused the action.

These bits indicate whether a comparison will start or not on any incoming event.

Name: INTENCLR
Offset: 0x04 [ID-00001f13]
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
					OVF	WINMON	OVERRUN	RESRDY
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 3 – OVF: Overflow Interrupt Enable

Writing a zero to this bit has no effect.

Writing a one to this bit will clear the Overflow Interrupt Enable bit, which disables the corresponding interrupt request.

Value	Description
0	The overflow interrupt is disabled.
1	The overflow interrupt is enabled, and an interrupt request will be generated when the Overflow interrupt flag is set.

Bit 2 – WINMON: Window Monitor Interrupt Enable

Writing a zero to this bit has no effect.

Writing a one to this bit will clear the Window Monitor Interrupt Enable bit, which disables the corresponding interrupt request.

Value	Description
0	The window monitor interrupt is disabled.
1	The window monitor interrupt is enabled, and an interrupt request will be generated when the Window Monitor interrupt flag is set.

Bit 1 – OVERRUN: Overrun Interrupt Enable

Writing a zero to this bit has no effect.

Writing a one to this bit will clear the Overrun Interrupt Enable bit, which disables the corresponding interrupt request.

Value	Description
0	The Overrun interrupt is disabled.
1	The Overrun interrupt is enabled, and an interrupt request will be generated when the Overrun interrupt flag is set.

Bit 0 – RESRDY: Result Ready Interrupt Enable

Writing a zero to this bit has no effect.

Writing a one to this bit will clear the Result Ready Interrupt Enable bit, which disables the corresponding interrupt request.

Value	Description
0	The Result Ready interrupt is disabled.
1	The Result Ready interrupt is enabled, and an interrupt request will be generated when the Result Ready interrupt flag is set.

44.6.2.3 Measurement

In the Configuration A register, the Number of Reference Clock Cycles field ([CFG.A.REFNUM](#)) selects the duration of the measurement. The measurement is given in number of GCLK_FREQM_REF periods.

Note: The REFNUM field must be written before the FREQM is enabled.

After the FREQM is enabled, writing a '1' to the START bit in the Control B register ([CTRL.B.START](#)) starts the measurement. The BUSY bit in Status register ([STATUS.BUSY](#)) is set when the measurement starts, and cleared when the measurement is complete.

There is also an interrupt request for Measurement Done: When the Measurement Done bit in Interrupt Enable Set register ([INTENSET.DONE](#)) is '1' and a measurement is finished, the Measurement Done bit in the Interrupt Flag Status and Clear register ([INTFLAG.DONE](#)) will be set and an interrupt request is generated.

The result of the measurement can be read from the Value register ([VALUE.VALUE](#)). The frequency of the measured clock GCLK_FREQM_MSR is then:

$$f_{\text{CLK_MSR}} = \left(\frac{\text{VALUE}}{\text{REFNUM}} \right) f_{\text{CLK_REF}}$$

Note: In order to make sure the measurement result ([VALUE.VALUE\[23:0\]](#)) is valid, the overflow status ([STATUS.OVF](#)) should be checked.

In case an overflow condition occurred, indicated by the Overflow bit in the STATUS register ([STATUS.OVF](#)), either the number of reference clock cycles must be reduced ([CFG.A.REFNUM](#)), or a faster reference clock must be configured. Once the configuration is adjusted, clear the overflow status by writing a '1' to [STATUS.OVF](#). Then another measurement can be started by writing a '1' to [CTRL.B.START](#).

44.6.3 DMA Operation

Not applicable.

44.6.4 Interrupts

The FREQM has one interrupt source:

- DONE: A frequency measurement is done.

The interrupt flag in the Interrupt Flag Status and Clear ([INTFLAG](#)) register is set when the interrupt condition occurs. The interrupt can be enabled by writing a '1' to the corresponding bit in the Interrupt Enable Set ([INTENSET](#)) register, and disabled by writing a '1' to the corresponding bit in the Interrupt Enable Clear ([INTENCLR](#)) register.

An interrupt request is generated when the interrupt flag is set and the corresponding interrupt is enabled. The interrupt request remains active until the interrupt flag is cleared, the interrupt is disabled, or the FREQM is reset. See [INTFLAG](#) for details on how to clear interrupt flags. All interrupt requests from the peripheral are ORed together on system level to generate one combined interrupt request to the NVIC. The user must read the [INTFLAG](#) register to determine which interrupt condition is present.

This interrupt is a synchronous wake-up source.

Note that interrupts must be globally enabled for interrupt requests to be generated.

44.6.5 Events

Not applicable.

44.6.6 Sleep Mode Operation

The FREQM will continue to operate in idle sleep mode where the selected source clock is running. The FREQM's interrupts can be used to wake up the device from idle sleep mode.