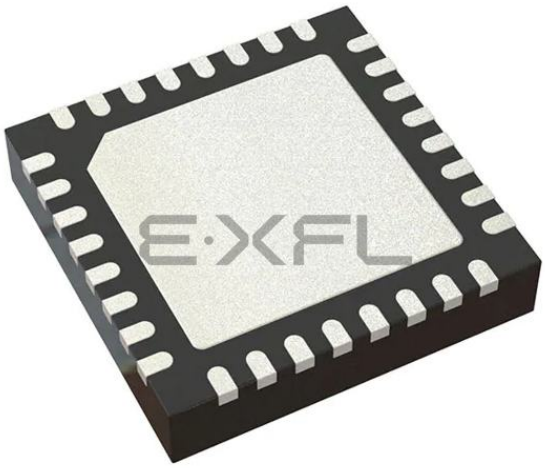

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, WDT
Number of I/O	26
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 10x12b, 1x16b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-VQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamc21e15a-mnt

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	FKBC[3:0]				JEPCC[3:0]			
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 7:4 – FKBC[3:0]: 4KB Count
These bits will always return zero when read, indicating that this debug component occupies one 4KB block.

Bits 3:0 – JEPCC[3:0]: JEP-106 Continuation Code
These bits will always return zero when read.

13.13.15 Peripheral Identification 0

Name: PID0
Offset: 0x1FE0
Reset: 0x00000000
Property: -

20.6.2 External Multipurpose Crystal Oscillator (XOSC) Operation

The XOSC can operate in two different modes:

- External clock, with an external clock signal connected to the XIN pin
- Crystal oscillator, with an external 0.4-32MHz crystal

The XOSC can be used as a clock source for generic clock generators. This is configured by the Generic Clock Controller.

At reset, the XOSC is disabled, and the XIN/XOUT pins can be used as General Purpose I/O (GPIO) pins or by other peripherals in the system. When XOSC is enabled, the operating mode determines the GPIO usage. When in crystal oscillator mode, the XIN and XOUT pins are controlled by the OSCCTRL, and GPIO functions are overridden on both pins. When in external clock mode, only the XIN pin will be overridden and controlled by the OSCCTRL, while the XOUT pin can still be used as a GPIO pin.

The XOSC is enabled by writing a '1' to the Enable bit in the External Multipurpose Crystal Oscillator Control register (XOSCCTRL.ENABLE).

To enable XOSC as an external crystal oscillator, the XTAL Enable bit (XOSCCTRL.XTALEN) must be written to '1'. If XOSCCTRL.XTALEN is zero, the external clock input on XIN will be enabled.

When in crystal oscillator mode (XOSCCTRL.XTALEN=1), the External Multipurpose Crystal Oscillator Gain (XOSCCTRL.GAIN) must be set to match the external crystal oscillator frequency. If the External Multipurpose Crystal Oscillator Automatic Amplitude Gain Control (XOSCCTRL.AMPGC) is '1', the oscillator amplitude will be automatically adjusted, and in most cases result in a lower power consumption.

The XOSC will behave differently in different sleep modes, based on the settings of XOSCCTRL.RUNSTDBY, XOSCCTRL.ONDEMAND, and XOSCCTRL.ENABLE. If XOSCCTRL.ENABLE=0, the XOSC will be always stopped. For XOSCCTRL.ENABLE=1, this table is valid:

Table 20-1. XOSC Sleep Behavior

CPU Mode	XOSCCTRL.RUNSTDBY	XOSCCTRL.ONDEMAND	Sleep Behavior
Active or Idle	-	0	Always run
Active or Idle	-	1	Run if requested by peripheral
Standby	1	0	Always run
Standby	1	1	Run if requested by peripheral
Standby	0	-	Run if requested by peripheral

After a hard reset, or when waking up from a sleep mode where the XOSC was disabled, the XOSC will need a certain amount of time to stabilize on the correct frequency. This start-up time can be configured by changing the Oscillator Start-Up Time bit group (XOSCCTRL.STARTUP) in the External Multipurpose Crystal Oscillator Control register. During the start-up time, the oscillator output is masked to ensure that no unstable clock propagates to the digital logic.

The External Multipurpose Crystal Oscillator Ready bit in the Status register (STATUS.XOSCRDY) is set once the external clock or crystal oscillator is stable and ready to be used as a clock source. An interrupt is generated on a zero-to-one transition on STATUS.XOSCRDY if the External Multipurpose Crystal Oscillator Ready bit in the Interrupt Enable Set register (INTENSET.XOSCRDY) is set.

Value	Description
0000	48MHz
0001	24MHz
0010	16MHz
0011	12MHz
0100	9.6MHz
0101	8MHz
0110	6.86MHz
0111	6MHz
1000	5.33MHz
1001	4.8MHz
1010	4.36MHz
1011	4MHz
1100	3.69MHz
1101	3.43MHz
1110	3.2MHz
1111	3MHz

20.8.10 OSC48M Startup

Name: OSC48MSTUP
Offset: 0x16 [ID-00001eee]
Reset: 0x07
Property: -

Bit	7	6	5	4	3	2	1	0
						STARTUP[2:0]		
Access						R/W	R/W	R/W
Reset						1	1	1

Bits 2:0 – STARTUP[2:0]: Oscillator Startup Delay
These bits select the oscillator start-up delay in oscillator cycles.

Table 20-6. Oscillator Divider Selection

STARTUP[2:0]	Number of OSCM48M Clock Cycles	Approximate Equivalent Time
0x0	8	166ns
0x1	16	333ns
0x2	32	667ns
0x3	64	1.333µs
0x4	128	2.667µs
0x5	256	5.333µs
0x6	512	10.667µs
0x7	1024	21.333µs

Value	Description
0	The DPLL Lock signal is cleared, when the DPLL is disabled or when the DPLL is trying to reach the target frequency.
1	The DPLL Lock signal is asserted when the desired frequency is reached.

20.8.18 OSC48M Calibration

This register (bits 0 to 21) must be updated with the corresponding data in the NVM Software Calibration Area: CAL48M 5V or CAL48M 3V3, depending on the VDD range. Refer to NVM Software Calibration Area Mapping.

Note: This register is only available for Rev D silicon.

Name: CAL48M
Offset: 0x38 [ID-00001eee]
Reset: Calibrated value for VDD range 3.6 V to 5.5 V
Property: PAC Write-Protection

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
			TCAL[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			x	x	x	x	x	x

Bit	15	14	13	12	11	10	9	8
							FRANGE[1:0]	
Access							R/W	R/W
Reset							x	x

Bit	7	6	5	4	3	2	1	0
			FCAL[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			x	x	x	x	x	x

Bits 21:16 – TCAL[5:0]: Temperature Calibration

Bits 9:8 – FRANGE[1:0]: Frequency Range

Bits 5:0 – FCAL[5:0]: Frequency Calibration

Related Links

NVM Software Calibration Area Mapping

Value	Description
0	In active mode, the BODVDD operates in continuous mode.
1	In active mode, the BODVDD operates in sampling mode.

Bit 6 – RUNSTDBY: Run in Standby
This bit is not synchronized.

Value	Description
0	In standby sleep mode, the BODVDD is disabled.
1	In standby sleep mode, the BODVDD is enabled.

Bit 5 – STDBYCFG: BODVDD Configuration in Standby Sleep Mode
If the RUNSTDBY bit is set to '1', the STDBYCFG bit sets the BODVDD configuration in standby sleep mode.

This bit is not synchronized.

Value	Description
0	In standby sleep mode, the BODVDD is enabled and configured in continuous mode.
1	In standby sleep mode, the BODVDD is enabled and configured in sampling mode.

Bits 4:3 – ACTION[1:0]: BODVDD Action
These bits are used to select the BODVDD action when the supply voltage crosses below the BODVDD threshold.

These bits are loaded from NVM User Row at start-up.

This bit field is not synchronized.

Value	Name	Description
0x0	NONE	No action
0x1	RESET	The BODVDD generates a reset
0x2	INT	The BODVDD generates an interrupt
0x3	-	Reserved

Bit 2 – HYST: Hysteresis
This bit indicates whether hysteresis is enabled for the BODVDD threshold voltage.

This bit is loaded from NVM User Row at start-up.

This bit is not synchronized.

Value	Description
0	No hysteresis.
1	Hysteresis enabled.

Bit 1 – ENABLE: Enable
This bit is loaded from NVM User Row at start-up.

This bit is not enable-protected.

Value	Description
0	The EIC is clocked by GCLK_EIC.
1	The EIC is clocked by CLK_ULP32K.

Bit 1 – ENABLE: Enable
Due to synchronization there is a delay between writing to CTRLA.ENABLE until the peripheral is enabled/disabled. The value written to CTRLA.ENABLE will read back immediately and the Enable bit in the Synchronization Busy register will be set (SYNCBUSY.ENABLE=1). SYNCBUSY.ENABLE will be cleared when the operation is complete.

This bit is not Enable-Protected.

This bit is Write-Synchronized.

Value	Description
0	The EIC is disabled.
1	The EIC is enabled.

Bit 0 – SWRST: Software Reset
Writing a '0' to this bit has no effect.

Writing a '1' to this bit resets all registers in the EIC to their initial state, and the EIC will be disabled.

Writing a '1' to CTRLA.SWRST will always take precedence, meaning that all other writes in the same write operation will be discarded.

Due to synchronization there is a delay from writing CTRLA.SWRST until the Reset is complete. CTRLA.SWRST and SYNCBUSY.SWRST will both be cleared when the Reset is complete.

This bit is not Enable-Protected.

This bit is Write-Synchronized.

Value	Description
0	There is no ongoing reset operation.
1	The reset operation is ongoing.

26.8.2 Non-Maskable Interrupt Control

Name: NMICTRL
Offset: 0x01
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
				NMIASYNCH	NMIFILTEN	NMISENSE[2:0]		
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit 4 – NMIASYNCH: Asynchronous Edge Detection Mode
The NMI edge detection can be operated synchronously or asynchronously to the EIC clock.

27.4 Signal Description

Not applicable.

27.5 Product Dependencies

In order to use this peripheral, other parts of the system must be configured correctly, as described in the following sections.

27.5.1 Power Management

The NVMCTRL will continue to operate in any sleep mode where the selected source clock is running. The NVMCTRL interrupts can be used to wake up the device from sleep modes.

The Power Manager will automatically put the NVM block into a low-power state when entering sleep mode. This is based on the Control B register (CTRLB) SLEEPPRM bit setting. Refer to the CTRLB.SLEEPPRM register description for more details. The NVM block goes into low-power mode automatically when the device enters STANDBY mode regardless of SLEEPPRM. The NVM Page Buffer is lost when the NVM goes into low power mode therefore a write command must be issued prior entering the NVM low power mode. NVMCTRL SLEEPPRM can be disabled to avoid such loss when the CPU goes into sleep except if the device goes into STANDBY mode for which there is no way to retain the Page Buffer.

Related Links

PM – Power Manager

27.5.2 Clocks

Two synchronous clocks are used by the NVMCTRL. One is provided by the AHB bus (CLK_NVMCTRL_AHB) and the other is provided by the APB bus (CLK_NVMCTRL_APB). For higher system frequencies, a programmable number of wait states can be used to optimize performance. When changing the AHB bus frequency, the user must ensure that the NVM Controller is configured with the proper number of wait states. Refer to the Electrical Characteristics for the exact number of wait states to be used for a particular frequency range.

Related Links

Electrical Characteristics 85°C (SAM C20/C21 E/G/J)

27.5.3 Interrupts

The NVM Controller interrupt request line is connected to the interrupt controller. Using the NVMCTRL interrupt requires the interrupt controller to be programmed first.

27.5.4 Debug Operation

When an external debugger forces the CPU into debug mode, the peripheral continues normal operation.

Access to the NVM block can be protected by the security bit. In this case, the NVM block will not be accessible. See the section on the NVMCTRL Security Bit for details.

27.5.5 Register Access Protection

All registers with write-access are optionally write-protected by the Peripheral Access Controller (PAC), except the following registers:

- Interrupt Flag Status and Clear register (INTFLAG)
- Status register (STATUS)

has control over the output state of the pad, as well as the ability to read the current physical pad state. Refer to *I/O Multiplexing and Considerations* for details.

Device-specific configurations may cause some lines (and the corresponding Pxy pin) not to be implemented.

Related Links

I/O Multiplexing and Considerations

28.5.2 Power Management

During Reset, all PORT lines are configured as inputs with input buffers, output buffers and pull disabled.

The PORT peripheral will continue operating in any sleep mode where its source clock is running.

28.5.3 Clocks

The PORT bus clock (CLK_PORT_APB) can be enabled and disabled in the Main Clock module, and the default state of CLK_PORT_APB can be found in the *Peripheral Clock Masking* section in *MCLK – Main Clock*.

The EVSYS and APB will insert wait states in the event of concurrent PORT accesses.

The PORT input synchronizers use the CPU main clock so that the resynchronization delay is minimized with respect to the APB clock.

Related Links

MCLK – Main Clock

28.5.4 DMA

Not applicable.

28.5.5 Interrupts

Not applicable.

28.5.6 Events

The events of this peripheral are connected to the Event System.

Related Links

EVSYS – Event System

28.5.7 Debug Operation

When the CPU is halted in debug mode, this peripheral will continue normal operation. If the peripheral is configured to require periodical service by the CPU through interrupts or similar, improper operation or data loss may result during debugging. This peripheral can be forced to halt operation during debugging - refer to the Debug Control (DBGCTRL) register for details.

28.5.8 Register Access Protection

All registers with write-access can be optionally write-protected by the Peripheral Access Controller (PAC).

Note: Optional write-protection is indicated by the "PAC Write-Protection" property in the register description.

When the CPU is halted in debug mode, all write-protection is automatically disabled. Write-protection does not apply for accesses through an external debugger.

Related Links

31.5.8 Register Access Protection

Registers with write-access can be write-protected optionally by the peripheral access controller (PAC).

PAC Write-Protection is not available for the following registers:

- Interrupt Flag Clear and Status register (INTFLAG)
- Status register (STATUS)
- Data register (DATA)

Optional PAC Write-Protection is denoted by the "PAC Write-Protection" property in each individual register description.

Write-protection does not apply to accesses through an external debugger.

Related Links

PAC - Peripheral Access Controller

31.5.9 Analog Connections

Not applicable.

31.6 Functional Description

31.6.1 Principle of Operation

The USART uses the following lines for data transfer:

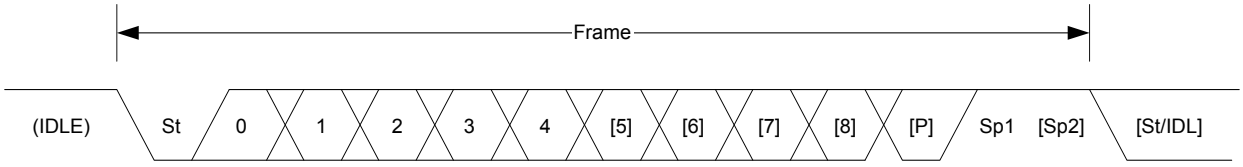
- RxD for receiving
- TxD for transmitting
- XCK for the transmission clock in synchronous operation

USART data transfer is frame based. A serial frame consists of:

- 1 start bit
- From 5 to 9 data bits (MSB or LSB first)
- No, even or odd parity bit
- 1 or 2 stop bits

A frame starts with the start bit followed by one character of data bits. If enabled, the parity bit is inserted after the data bits and before the first stop bit. After the stop bit(s) of a frame, either the next frame can follow immediately, or the communication line can return to the idle (high) state. The figure below illustrates the possible frame formats. Brackets denote optional bits.

Figure 31-2. Frame Formats



St Start bit. Signal is always low.

n, [n] Data bits. 0 to [5..9]

[P] Parity bit. Either odd or even.

Offset	Name	Bit Pos.								
0xB6		23:16			F1PI[5:0]					
0xB7		31:24	DMS[1:0]						RF1L	F1F
0xB8	RXF1A	7:0			F1AI[5:0]					
0xB9		15:8								
0xBA		23:16								
0xBB		31:24								
0xBC	RXESC	7:0		F1DS[2:0]				F0DS[2:0]		
0xBD		15:8						RBDS[2:0]		
0xBE		23:16								
0xBF		31:24								
0xC0	TXBC	7:0	TBSA[7:0]							
0xC1		15:8	TBSA[15:8]							
0xC2		23:16			NDTB[5:0]					
0xC3		31:24		TFQM	TFQS[5:0]					
0xC4	TXFQS	7:0			TFFL[5:0]					
0xC5		15:8				TFGI[4:0]				
0xC6		23:16			TFQF	TFQPI[4:0]				
0xC7		31:24								
0xC8	TXESC	7:0						TBDS[2:0]		
0xC9		15:8								
0xCA		23:16								
0xCB		31:24								
0xCC	TXBRP	7:0	TRPn	TRPn	TRPn	TRPn	TRPn	TRPn	TRPn	TRPn
0xCD		15:8	TRPn	TRPn	TRPn	TRPn	TRPn	TRPn	TRPn	TRPn
0xCE		23:16	TRPn	TRPn	TRPn	TRPn	TRPn	TRPn	TRPn	TRPn
0xCF		31:24	TRPn	TRPn	TRPn	TRPn	TRPn	TRPn	TRPn	TRPn
0xD0	TXBAR	7:0	ARn	ARn	ARn	ARn	ARn	ARn	ARn	ARn
0xD1		15:8	ARn	ARn	ARn	ARn	ARn	ARn	ARn	ARn
0xD2		23:16	ARn	ARn	ARn	ARn	ARn	ARn	ARn	ARn
0xD3		31:24	ARn	ARn	ARn	ARn	ARn	ARn	ARn	ARn
0xD4	TXBCR	7:0	CRn	CRn	CRn	CRn	CRn	CRn	CRn	CRn
0xD5		15:8	CRn	CRn	CRn	CRn	CRn	CRn	CRn	CRn
0xD6		23:16	CRn	CRn	CRn	CRn	CRn	CRn	CRn	CRn
0xD7		31:24	CRn	CRn	CRn	CRn	CRn	CRn	CRn	CRn
0xD8	TXBTO	7:0	TOn	TOn	TOn	TOn	TOn	TOn	TOn	TOn
0xD9		15:8	TOn	TOn	TOn	TOn	TOn	TOn	TOn	TOn
0xDA		23:16	TOn	TOn	TOn	TOn	TOn	TOn	TOn	TOn
0xDB		31:24	TOn	TOn	TOn	TOn	TOn	TOn	TOn	TOn
0xDC	TXBCF	7:0	CFn	CFn	CFn	CFn	CFn	CFn	CFn	CFn
0xDD		15:8	CFn	CFn	CFn	CFn	CFn	CFn	CFn	CFn
0xDE		23:16	CFn	CFn	CFn	CFn	CFn	CFn	CFn	CFn
0xDF		31:24	CFn	CFn	CFn	CFn	CFn	CFn	CFn	CFn
0xE0	TXBTIE	7:0	TIEn	TIEn	TIEn	TIEn	TIEn	TIEn	TIEn	TIEn
0xE1		15:8	TIEn	TIEn	TIEn	TIEn	TIEn	TIEn	TIEn	TIEn
0xE2		23:16	TIEn	TIEn	TIEn	TIEn	TIEn	TIEn	TIEn	TIEn
0xE3		31:24	TIEn	TIEn	TIEn	TIEn	TIEn	TIEn	TIEn	TIEn
0xE4	TXBCIE	7:0	CFIEn	CFIEn	CFIEn	CFIEn	CFIEn	CFIEn	CFIEn	CFIEn

Bit	31	30	29	28	27	26	25	24
	CFn	CFn	CFn	CFn	CFn	CFn	CFn	CFn
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	CFn	CFn	CFn	CFn	CFn	CFn	CFn	CFn
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CFn	CFn	CFn	CFn	CFn	CFn	CFn	CFn
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CFn	CFn	CFn	CFn	CFn	CFn	CFn	CFn
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – CFn: Cancellation Finished
Each Tx Buffer has its own Cancellation Finished bit.

The bits are set when the corresponding TXBRP bit is cleared after a cancellation was requested via TXBCR. In case the corresponding TXBRP bit was not set at the point of cancellation, CF is set immediately.

The bits are reset when a new transmission is requested by writing ‘1’ to the corresponding bit of register TXBAR.

34.8.43 Tx Buffer Transmission Interrupt Enable

Name: TXBTIE
Offset: 0xE0 [ID-0000a4bb]
Reset: 0x00000000
Property: -

Name: DBGCTRL
Offset: 0x0F
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
								DBGRUN
Access								R/W
Reset								0

Bit 0 – DBGRUN: Run in Debug Mode
This bit is not affected by a software Reset, and should not be changed by software while the TC is enabled.

Value	Description
0	The TC is halted when the device is halted in debug mode.
1	The TC continues normal operation when the device is halted in debug mode.

35.7.1.12 Synchronization Busy

Name: SYNCBUSY
Offset: 0x10
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
		CCx	PER	COUNT	STATUS	CTRLB	ENABLE	SWRST
Access		R	R	R	R	R	R	R
Reset		0	0	0	0	0	0	0

Bit 6 – CCx: Compare/Capture Channel x Synchronization Busy
For details on CC channels number, refer to each TC feature list.

This bit is set when the synchronization of CCx between clock domains is started.

hardware update is performed. After all the buffer registers are loaded correctly, the buffered registers can be unlocked.

This bit has no effect when input capture operation is enabled.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the LUPD bit.

Value	Description
0	The CCBUFx and PERBUF buffer registers value are copied into CCx and PER registers on hardware update condition.
1	The CCBUFx and PERBUF buffer registers value are not copied into CCx and PER registers on hardware update condition.

Bit 0 – DIR: Counter Direction
This bit is used to change the direction of the counter.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the bit and make the counter count up.

Value	Description
0	The timer/counter is counting up (incrementing).
1	The timer/counter is counting down (decrementing).

35.7.3.3 Control B Set

This register allows the user to set bits in the CTRLB register without doing a read-modify-write operation. Changes in this register will also be reflected in the Control B Clear register (CTRLBCLR).

Name: CTRLBSET
Offset: 0x05
Reset: 0x00
Property: PAC Write-Protection, Read-synchronized, Write-Synchronized

Bit	7	6	5	4	3	2	1	0
	CMD[2:0]					ONESHOT	LUPD	DIR
Access	R/W	R/W	R/W			R/W	R/W	R/W
Reset	0	0	0			0	0	0

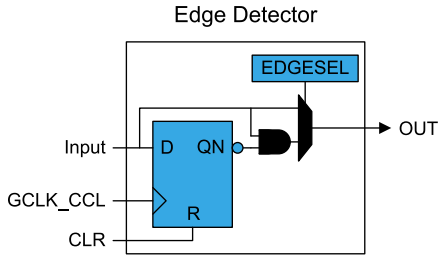
Bits 7:5 – CMD[2:0]: Command
These bits are used for software control of the TC. The commands are executed on the next prescaled GCLK_TC clock cycle. When a command has been executed, the CMD bit group will be read back as zero.

Writing 0x0 to these bits has no effect.

Writing a value different from 0x0 to these bits will issue a command for execution.

Value	Name	Description
0x0	NONE	No action
0x1	RETRIGGER	Force a start, restart or retrigger
0x2	STOP	Force a stop

Figure 37-13. Edge Detector



37.6.2.7 Sequential Logic

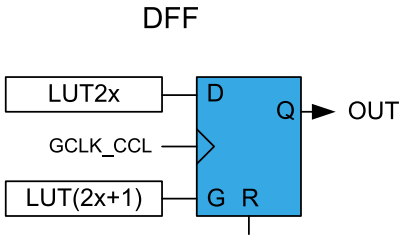
Each LUT pair can be connected to the internal sequential logic which can be configured to work as D flip flop, JK flip flop, gated D-latch or RS-latch by writing the Sequential Selection bits on the corresponding Sequential Control x register (SEQCTRLx.SEQSEL). Before using sequential logic, the GCLK_CCL clock and optionally each LUT filter or edge detector must be enabled.

Note: While configuring the sequential logic, the even LUT must be disabled. When configured the even LUT must be enabled.

Gated D Flip-Flop (DFF)

When the DFF is selected, the D-input is driven by the even LUT output (LUT0 and LUT2), and the G-input is driven by the odd LUT output (LUT1 and LUT3), as shown in Figure 37-14.

Figure 37-14. D Flip Flop



When the even LUT is disabled (LUTCTRL0.ENABLE=0 / LUTCTRL2.ENABLE=0), the flip-flop is asynchronously cleared. The reset command (R) is kept enabled for one APB clock cycle. In all other cases, the flip-flop output (OUT) is refreshed on rising edge of the GCLK_CCL, as shown in Table 37-2.

Table 37-2. DFF Characteristics

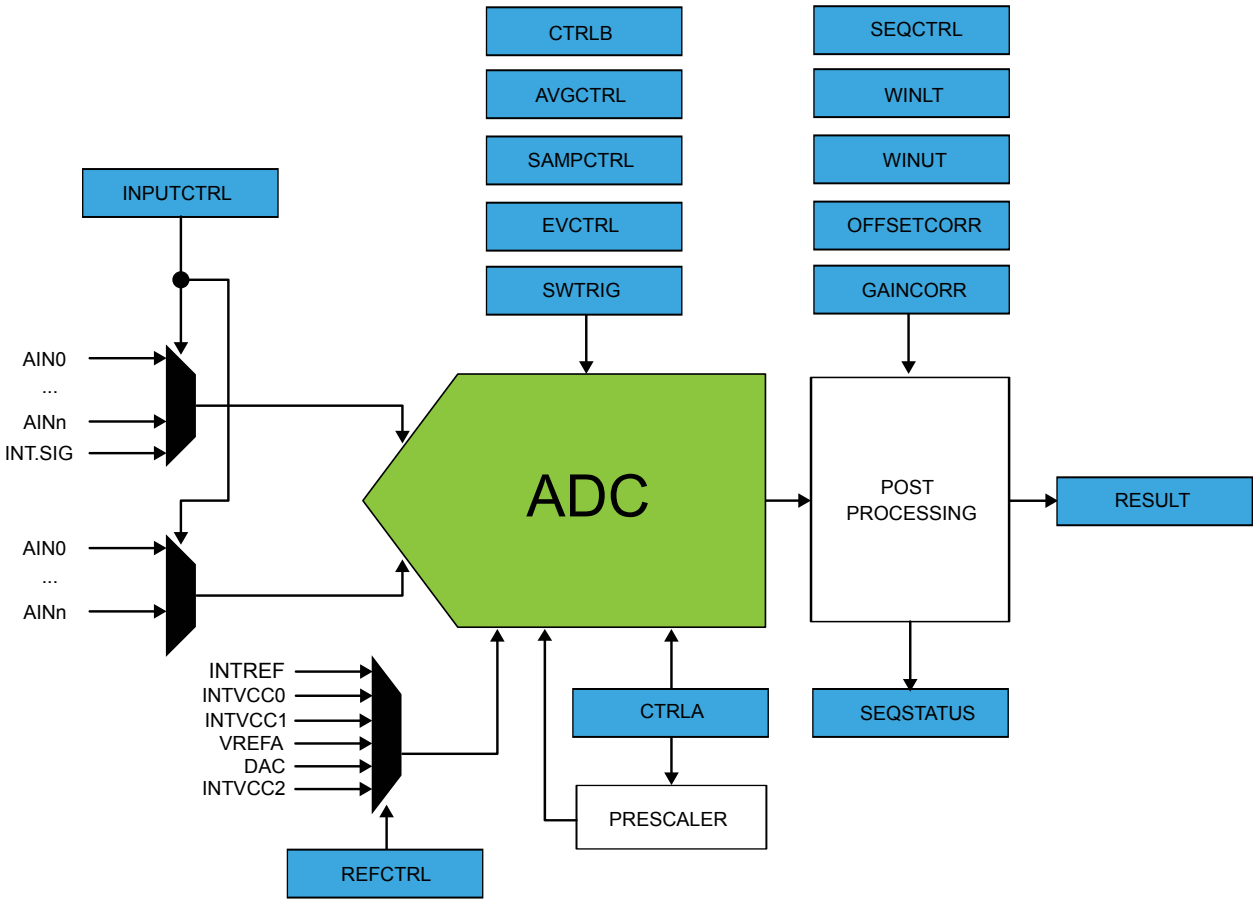
R	G	D	OUT
1	X	X	Clear
0	1	1	Set
		0	Clear
	0	X	Hold state (no change)

JK Flip-Flop (JK)

When this configuration is selected, the J-input is driven by the even LUT output (LUT0 and LUT2), and the K-input is driven by the odd LUT output (LUT1 and LUT3), as shown in Figure 37-15.

38.3 Block Diagram

Figure 38-1. ADC Block Diagram



38.4 Signal Description

Signal	Description	Type
VREFA	Analog input	External reference voltage
AIN[11..0]	Analog input	Analog input channels

Note: One signal can be mapped on several pins.

Related Links

Configuration Summary

I/O Multiplexing and Considerations

38.5 Product Dependencies

In order to use this peripheral, other parts of the system must be configured correctly, as described below.

38.5.1 I/O Lines

Using the ADC's I/O lines requires the I/O pins to be configured using the port configuration (PORT).

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	OFFSETCORR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	OFFSETCORR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	OFFSETCORR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 23:0 – OFFSETCORR[23:0]: Offset Correction
The OFFSETCORR is a signed integer value.

A specific offset, gain and shift can be applied to SDADC by performing the following operation:

```
(RESULT + OFFSETCORR)*GAINCORR/2^SHIFTCORR
```

39.8.15 Gain Correction

Name: GAINCORR
Offset: 0x18 [ID-0000243d]
Reset: 0x0001
Property: PAC Write-Protection, Write-Synchronized

Bit	15	14	13	12	11	10	9	8
			GAINCORR[13:8]					
Access			R	R	R	R	R	R
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	GAINCORR[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	1	0	0	0	0	0	0	0

Bits 13:0 – GAINCORR[13:0]: Gain Correction
A specific offset, gain and shift can be applied to SDADC by performing the following operation:

```
(RESULT + OFFSETCORR)*GAINCORR/2^SHIFTCORR
```

39.8.16 Shift Correction

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
			TCAL[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			FCAL[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 13:8 – TCAL[5:0]: Temperature Calibration
This value from production test must be loaded from the NVM software calibration row into the CAL register by software to achieve the specified accuracy. The value must be copied only, and must not be changed.

Bits 5:0 – FCAL[5:0]: Frequency Calibration
This value from production test must be loaded from the NVM software calibration row into the CAL register by software to achieve the specified accuracy. The value must be copied only, and must not be changed.

43.8.16 Debug Control

Name: DBGCTRL
Offset: 0x24 [ID-00001f13]
Reset: 0x00
Property: –

Bit	7	6	5	4	3	2	1	0
								DBGRUN
Access								R/W
Reset								0

Bit 0 – DBGRUN: Debug Run
This bit is not reset by a software reset.

This bits controls the functionality when the CPU is halted by an external debugger.

Bit	7	6	5	4	3	2	1	0
							ENABLE	SWRST
Access							R/W	R/W
Reset							0	0

Bit 1 – ENABLE: Enable
Due to synchronization there is delay from writing CTRLA.ENABLE until the peripheral is enabled/disabled. The value written to CTRLA.ENABLE will read back immediately and the ENABLE bit in the Synchronization Busy register (SYNCBUSY.ENABLE) will be set. SYNCBUSY.ENABLE will be cleared when the operation is complete.

This bit is not enable-protected.

Value	Description
0	The peripheral is disabled.
1	The peripheral is enabled.

Bit 0 – SWRST: Software Reset
Writing a '0' to this bit has no effect.

Writing a '1' to this bit resets all registers in the FREQM to their initial state, and the FREQM will be disabled. Writing a '1' to this bit will always take precedence, meaning that all other writes in the same write-operation will be discarded.

Due to synchronization there is a delay from writing CTRLA.SWRST until the Reset is complete. CTRLA.SWRST and SYNCBUSY.SWRST will both be cleared when the Reset is complete.

This bit is not enable-protected.

Value	Description
0	There is no ongoing Reset operation.
1	The Reset operation is ongoing.

44.8.2 Control B

Name: CTRLB
Offset: 0x01 [ID-00000e03]
Reset: 0x00
Property: –

Bit	7	6	5	4	3	2	1	0
								START
Access								W
Reset								0

Bit 0 – START: Start Measurement

Value	Description
0	Writing a '0' has no effect.
1	Writing a '1' starts a measurement.

44.8.3 Configuration A

$C_{LEXT}=2(C_L-C_{STRAY}-C_{SHUNT})$

where C_{STRAY} is the capacitance of the pins and PCB and CSHUNT is the shunt capacitance of the crystal.

Table 45-43. 32kHz Crystal Oscillator Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
f_{OUT} (1)	Crystal oscillator frequency		-	32768	-	Hz
C_L (1)	Crystal load capacitance		-	-	12.5	pF
C_{SHUNT} (1)	Crystal shunt capacitance		-	-	1.75	
Cm (1)	Motional capacitance		-	1.25	-	fF
ESR	Crystal Equivalent Series Resistance - SF = 3	F = 32.768kHz, C_L=12.5 pF	-	-	79	kΩ
Cxin32k	Parasitic capacitor load		-	2.9	-	pF
Cxout32k			-	3.2	-	
Tstart	Startup time	F = 32.768kHz, C_L=12.5 pF	-	16	24	Kcycles

1. These are based on simulation. These values are not covered by test or characterization

Table 45-44. Power Consumption(1)

Symbol	Parameters	Conditions	Ta	Typ.	Max	Units
I_{DD}	Current consumption	VDD = 5.0V	Max 85°C Typ 25°C	1528	1720	nA

1. These are based on characterization.

45.12.3 Digital Phase Locked Loop (DPLL) Characteristics

Table 45-45. Fractional Digital Phase Locked Loop Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f_{IN}(1)	Input frequency		32		2000	KHz
f_{OUT}(1)	Output frequency		48		96	MHz
Jp(2)	Period jitter (Peak-Peak value)	f_{IN}= 32 kHz, f_{OUT}= 48 MHz	-	1.5	3.0	%
		f_{IN}= 32 kHz, f_{OUT}= 96 MHz	-	2.7	8.0	
		f_{IN}= 2 MHz, f_{OUT}= 48 MHz	-	1.8	4.0	
		f_{IN}= 2 MHz, f_{OUT}= 96 MHz	-	2.5	6.0	
t_{LOCK}(2)	Lock Time	After startup, time to get lock signal. f_{IN}= 32 kHz, f_{OUT}= 96 MHz	-	1.1	1.5	ms
		After startup, time to get lock signal.	-	25	35	µs

Figure 49-4. External Analog Reference Schematic With One Reference

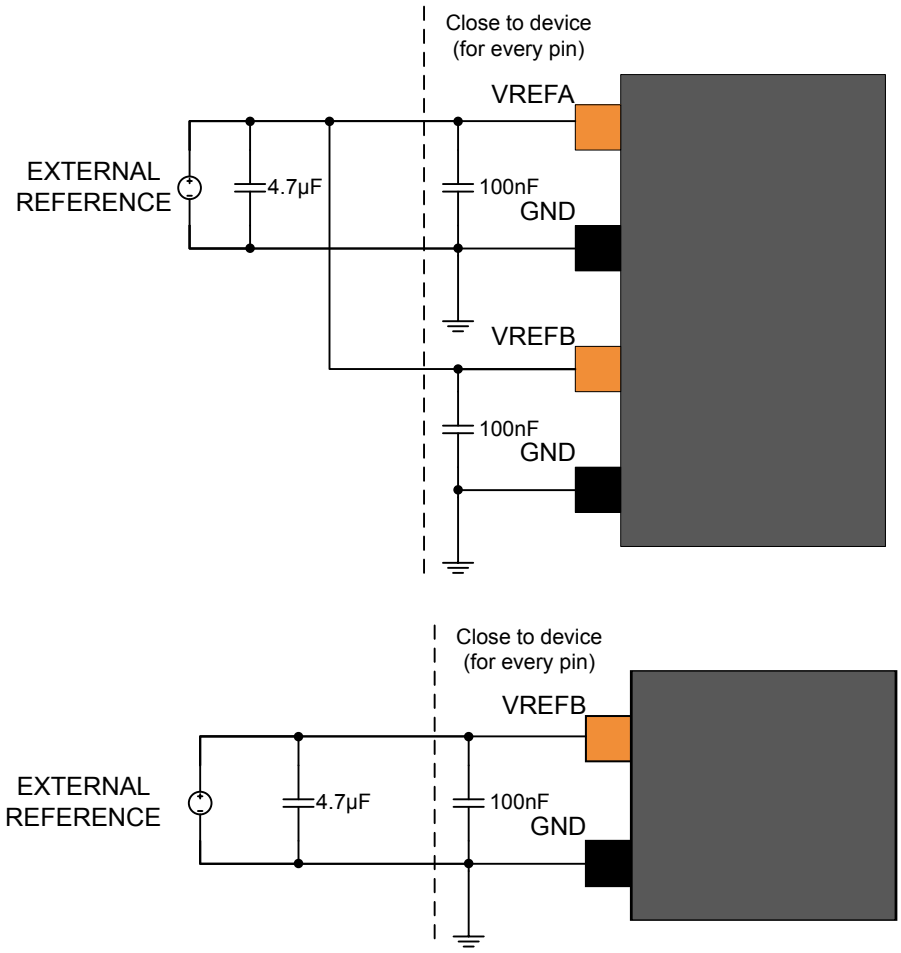


Table 49-2. External Analog Reference Connections

Signal Name	Recommended Pin Connection	Description
VREFA	2.0V to V_{DDANA} - 0.6V for ADC 1.0V to V_{DDANA} - 0.6V for DAC Decoupling/filtering capacitors: 100nF(1)(2) and 4.7µF(1)	External reference from VREFA pin on the analog port.
VREFB	1.0V to 5.5V for SDADC Decoupling/filtering capacitors: 100nF(1)(2) and 4.7µF(1)	External reference from VREFB pin on the analog port.
GND		Ground

Note:

1. These values are given as a typical example.
2. Decoupling capacitor should be placed close to the device for each supply pin pair in the signal group.