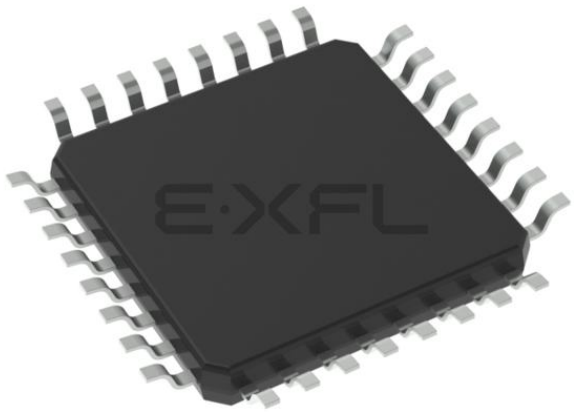

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, WDT
Number of I/O	26
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 10x12b, 1x16b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-TQFP
Supplier Device Package	32-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamc21e16a-ant

Peripheral Name	Base Address	IRQ Line	AHB Clock		APB Clock		Generic Clock	PAC		Events		DMA	
			Index	Enabled at Reset	Index	Enabled at Reset	Index	Index	Prot at Reset	User	Generator	Index	Sleep Walking
DAC	0x42005400	28			21	N	36	21	N	38: START	78: EMPTY	45: EMPTY	Y
PTC	0x42005800	30			22	N	37	22	N	39: STCONV	79: EOC 80: WCOMP	EOC: 46 WCOMP: 47 SEQ: 48	
CCL	0x42005C00				23	N	38	23	N	40-43 : LUTIN0-3	781-84: LUTOUT0-3		Y
DIVAS	0x48000000		12	Y									N/A

Table 12-4. Peripherals Configuration Summary SAM C20 E/G/J

Peripheral Name	Base Address	IRQ Line	AHB Clock		APB Clock		Generic Clock	PAC		Events		DMA	
			Index	Enabled at Reset	Index	Enabled at Reset	Index	Index	Prot at Reset	User	Generator	Index	Sleep Walking
AHB-APB Bridge A	0x40000000		0	Y									N/A
PAC	0x44000000	0	10	Y	0	Y		0	N		85 : ACCERR		N/A
PM	0x40000400	0			1	Y		1	N				N/A
MCLK	0x40000800	0			2	Y		2	N				Y
RSTC	0x40000C00				3	Y		3	N				N/A
OSCCTRL	0x40001000	0			4	Y	0: FDPLL96M clk source 1: FDPLL96M 32kHz	4	N		0: XOSC_FAIL		Y
OSC32KCTRL	0x40001400	0			5	Y		5	N		1: XOSC32K_FAIL		Y
SUPC	0x40001800	0			6	Y		6	N				N/A
GCLK	0x40001C00				7	Y		7	N				N/A
WDT	0x40002000	1			8	Y		8	N				Y
RTC	0x40002400	2			9	Y		9	N		2: CMP0/ALARM0 3: CMP1 4: OVF 5-12: PER0-7		Y
EIC	0x40002800	3, NMI			10	Y	2	10	N		13-28: EXTINT0-15		Y
FREQM	0x40002C00	4			11	Y	3: Measure 4: Reference	11	N				N/A
AHB-APB Bridge B	0x41000000		1	Y									N/A
PORT	0x41000000				0	Y		0	N	1-4 : EV0-3			Y
DSU	0x41002000		3	Y	1	Y		1	Y				N/A
NVMCTRL	0x41004000	6	5	Y	2	Y	39	2	N				Y
DMAC	0x41006000	7	7	Y				3	N	5-8: CH0-3	30-33: CH0-3		Y
MTB	0x41008000								N	44: START 45: STOP			N/A
AHB-APB Bridge C	0x42000000		2	Y									N/A
EVSYS	0x42000000	8			0	N	6-17: one per CHANNEL	0	N				Y
SERCOM0	0x42000400	9			1	N	19: CORE 18: SLOW	1	N			2: RX 3: TX	Y
SERCOM1	0x42000800	10			2	N	20: CORE 18: SLOW	2	N			4: RX 5: TX	Y
SERCOM2	0x42000C00	11			3	N	21: CORE 18: SLOW	3	N			6: RX 7: TX	Y

18.7 Register Summary

Offset	Name	Bit Pos.								
0x00	RCAUSE	7:0		SYST	WDT	EXT		BODVDD	BODCORE	POR

18.8 Register Description

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16- and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly.

Some registers are optionally write-protected by the Peripheral Access Controller (PAC). Optional PAC write-protection is denoted by the "PAC Write-Protection" property in each individual register description. For details, refer to Register Access Protection.

18.8.1 Reset Cause

When a Reset occurs, the bit corresponding to the Reset source is set to '1' and all other bits are written to '0'.

Name: RCAUSE
Offset: 0x00
Property: –

Bit	7	6	5	4	3	2	1	0
		SYST	WDT	EXT		BODVDD	BODCORE	POR
Access		R	R	R		R	R	R
Reset		x	x	x		x	x	x

Bit 6 – SYST: System Reset Request
This bit is set if a System Reset Request has occurred. Refer to the Cortex processor documentation for more details.

Bit 5 – WDT: Watchdog Reset
This bit is set if a Watchdog Timer Reset has occurred.

Bit 4 – EXT: External Reset
This bit is set if an external Reset has occurred.

Bit 2 – BODVDD: Brown Out VDD Detector Reset
This bit is set if a BODVDD Reset has occurred.

Bit 1 – BODCORE: Brown Out CORE Detector Reset
This bit is set if a BODCORE Reset has occurred.

Bit 0 – POR: Power On Reset
This bit is set if a POR has occurred.

Related Links

MCLK – Main Clock

Peripheral Clock Masking

20.5.4 DMA

Not applicable.

20.5.5 Interrupts

The interrupt request line is connected to the Interrupt Controller. Using the OSCCTRL interrupts requires the interrupt controller to be configured first.

Related Links

Nested Vector Interrupt Controller

INTFLAG

Sleep Mode Controller

20.5.6 Events

The events of this peripheral are connected to the Event System.

Related Links

EVSYS – Event System

20.5.7 Debug Operation

When the CPU is halted in debug mode the OSCCTRL continues normal operation. If the OSCCTRL is configured in a way that requires it to be periodically serviced by the CPU through interrupts or similar, improper operation or data loss may result during debugging.

20.5.8 Register Access Protection

All registers with write-access can be write-protected optionally by the Peripheral Access Controller (PAC), except for the following registers:

- Interrupt Flag Status and Clear register (INTFLAG)

Note: Optional write-protection is indicated by the "PAC Write-Protection" property in the register description.

When the CPU is halted in debug mode, all write-protection is automatically disabled. Write-protection does not apply for accesses through an external debugger.

20.5.9 Analog Connections

The 0.4-32MHz crystal must be connected between the XIN and XOUT pins, along with any required load capacitors.

20.6 Functional Description

20.6.1 Principle of Operation

XOSCn, OSC48M, and FDPLL96M. are configured via OSCCTRL control registers. Through this interface, the oscillators are enabled, disabled, or have their calibration values updated.

The Status register gathers different status signals coming from the oscillators controlled by the OSCCTRL. The status signals can be used to generate system interrupts, and in some cases wake up the system from Sleep mode, provided the corresponding interrupt is enabled.

Value	Name	Description
0x2	GCLK	GCLK clock reference
0x3	Reserved	

Bit 3 – WUF: Wake Up Fast

Value	Description
0	DPLL clock is output after startup and lock time.
1	DPLL clock is output after startup time.

Bit 2 – LPEN: Low-Power Enable

Value	Description
0	The low-power mode is disabled. Time to Digital Converter is enabled.
1	The low-power mode is enabled. Time to Digital Converter is disabled. This will improve power consumption but increase the output jitter.

Bits 1:0 – FILTER[1:0]: Proportional Integral Filter Selection
These bits select the DPLL filter type:

Value	Name	Description
0x0	DEFAULT	Default filter mode
0x1	LBFILT	Low bandwidth filter
0x2	HBFILT	High bandwidth filter
0x3	HDFILT	High damping filter

20.8.15 DPLL Prescaler

Name: DPLLPRESC
Offset: 0x28 [ID-00001eee]
Reset: 0x00
Property: PAC Write-Protection, Write-Synchronized

Bit	7	6	5	4	3	2	1	0
							PRESC[1:0]	
Access							R/W	R/W
Reset							0	0

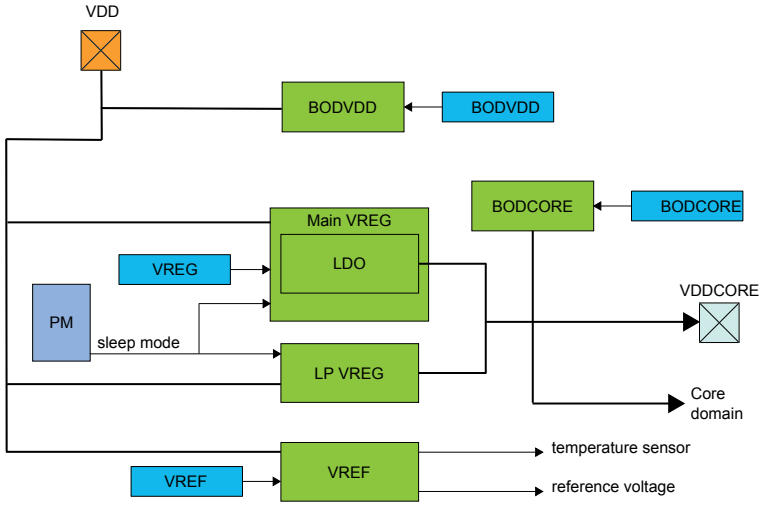
Bits 1:0 – PRESC[1:0]: Output Clock Prescaler
These bits define the output clock prescaler setting.

Value	Name	Description
0x0	DIV1	DPLL output is divided by 1
0x1	DIV2	DPLL output is divided by 2
0x2	DIV4	DPLL output is divided by 4
0x3	Reserved	

20.8.16 DPLL Synchronization Busy

22.3 Block Diagram

Figure 22-1. SUPC Block Diagram



22.4 Signal Description

Not appclicable.

Related Links

I/O Multiplexing and Considerations

22.5 Product Dependencies

In order to use this peripheral, other parts of the system must be configured correctly, as described below.

22.5.1 I/O Lines

Not applicable.

22.5.2 Power Management

The SUPC can operate in all sleep modes.

Related Links

PM – Power Manager

22.5.3 Clocks

The SUPC bus clock (CLK_SUPC_APB) can be enabled and disabled in the Main Clock module.

A 32KHz clock, asynchronous to the user interface clock (CLK_SUPC_APB), is required to run BODVDD and BODCORE in sampled mode. Due to this asynchronicity, writing to certain registers will require synchronization between the clock domains. Refer to Synchronization for further details.

Related Links

OSC32KCTRL – 32KHz Oscillators Controller

Peripheral Clock Masking

22.5.4 DMA

Not applicable.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
						BVDDSRDY	BODVDDDET	BODVDDRDY
Access						R	R	R
Reset						0	0	y

Bit 2 – BVDDSRDY: BODVDD Synchronization Ready

Value	Description
0	BODVDD synchronization is ongoing.
1	BODVDD synchronization is complete.

Bit 1 – BODVDDDET: BODVDD Detection

Value	Description
0	No BODVDD detection.
1	BODVDD has detected that the I/O power supply is going below the BODVDD reference value.

Bit 0 – BODVDDRDY: BODVDD Ready

The BODVDD can be enabled at start-up from NVM User Row.

Value	Description
0	BODVDD is not ready.
1	BODVDD is ready.

Related Links

NVM User Row Mapping

22.8.5 VDD Brown-Out Detector (BODVDD) Control

Name: BODVDD
Offset: 0x10 [ID-00001e33]
Reset: X determined from NVM User Row
Property: Write-Synchronized, Enable-Protected, PAC Write-Protection

PM – Power Manager

24.5.3 Clocks

The RTC bus clock (CLK_RTC_APB) can be enabled and disabled in the Main Clock module MCLK, and the default state of CLK_RTC_APB can be found in Peripheral Clock Masking section.

A 32KHz or 1KHz oscillator clock (CLK_RTC_OSC) is required to clock the RTC. This clock must be configured and enabled in the 32KHz oscillator controller (OSC32KCTRL) before using the RTC.

This oscillator clock is asynchronous to the bus clock (CLK_RTC_APB). Due to this asynchronicity, writing to certain registers will require synchronization between the clock domains. Refer to Synchronization for further details.

Related Links

OSC32KCTRL – 32KHz Oscillators Controller

Peripheral Clock Masking

24.5.4 DMA

Not applicable.

Related Links

DMAC – Direct Memory Access Controller

24.5.5 Interrupts

The interrupt request line is connected to the Interrupt Controller. Using the RTC interrupt requires the Interrupt Controller to be configured first.

Related Links

Nested Vector Interrupt Controller

24.5.6 Events

The events are connected to the *Event System*.

Related Links

EVSYS – Event System

24.5.7 Debug Operation

When the CPU is halted in debug mode the RTC will halt normal operation. The RTC can be forced to continue operation during debugging. Refer to DBGCTRL for details.

24.5.8 Register Access Protection

All registers with write-access are optionally write-protected by the peripheral access controller (PAC), except the following registers:

- Interrupt Flag Status and Clear (INTFLAG) register

Write-protection is denoted by the "PAC Write-Protection" property in the register description.

Write-protection does not apply to accesses through an external debugger. Refer to the PAC - Peripheral Access Controller for details.

Related Links

PAC - Peripheral Access Controller

Name: INTENCLR
Offset: 0x08
Reset: 0x0000
Property: PAC Write-Protection

Bit	15	14	13	12	11	10	9	8
	OVF							CMP0
Access	R/W							R/W
Reset	0							0

Bit	7	6	5	4	3	2	1	0
	PERn	PERn	PERn	PERn	PERn	PERn	PERn	PERn
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – OVF: Overflow Interrupt Enable
Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Overflow Interrupt Enable bit, which disables the Overflow interrupt.

Value	Description
0	The Overflow interrupt is disabled.
1	The Overflow interrupt is enabled.

Bit 8 – CMP0: Compare 0 Interrupt Enable
Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Compare 0 Interrupt Enable bit, which disables the Compare 0 interrupt.

Value	Description
0	The Compare 0 interrupt is disabled.
1	The Compare 0 interrupt is enabled.

Bits 7:0 – PERn: Periodic Interval n Interrupt Enable [n = 7..0]
Writing a '0' to this bit has no effect.

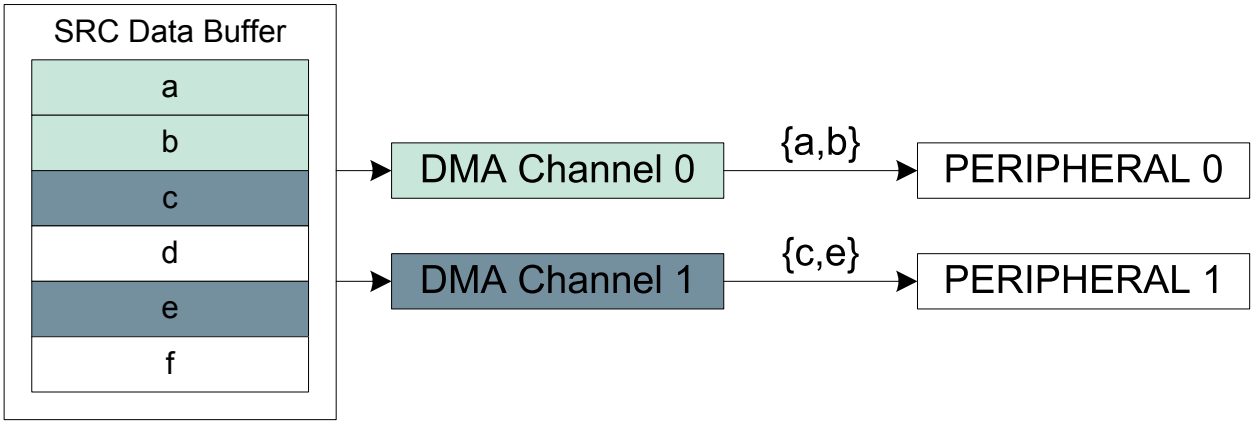
Writing a '1' to this bit will clear the Periodic Interval n Interrupt Enable bit, which disables the Periodic Interval n interrupt.

Value	Description
0	Periodic Interval n interrupt is disabled.
1	Periodic Interval n interrupt is enabled.

24.8.4 Interrupt Enable Set in COUNT32 mode (CTRLA.MODE=0)

This register allows the user to enable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Clear (INTENCLR) register.

Figure 25-8. Source Address Increment



Incrementation for the destination address of a block transfer is enabled by setting the Destination Address Incrementation Enable bit in the Block Transfer Control register (BTCTRL.DSTINC=1). The step size of the incrementation is configurable by clearing BTCTRL.STEPSEL=0 and writing BTCTRL.STEPSIZE to the desired step size. If BTCTRL.STEPSEL=1, the step size for the destination incrementation will be the size of one beat.

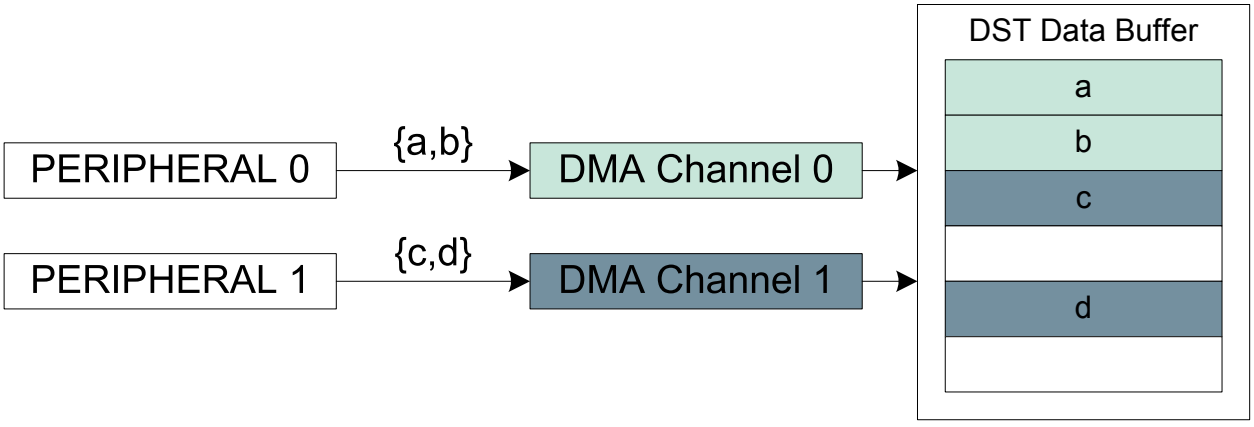
When the destination address incrementation is configured (BTCTRL.DSTINC=1), SRCADDR must be set and calculated as follows:

$DSTADDR = DSTADDR_{START} + BTCNT \bullet \left(BEATSIZE + 1\right) \bullet 2^{STEPSIZE}$	where BTCTRL.STEPSEL is zero
$DSTADDR = DSTADDR_{START} + BTCNT \bullet (BEATSIZE + 1)$	where BTCTRL.STEPSEL is one

- $DSTADDR_{START}$ is the destination address of the first beat transfer in the block transfer
- BTCNT is the initial number of beats remaining in the block transfer
- BEATSIZE is the configured number of bytes in a beat
- STEPSIZE is the configured number of beats for each incrementation

Figure 25-9shows an example where DMA channel 0 is configured to increment destination address by one beat (BTCTRL.DSTINC=1) and DMA channel 1 is configured to increment destination address by two beats (BTCTRL.DSTINC=1, BTCTRL.STEPSEL=0, and BTCTRL.STEPSIZE=0x1). As the source address for both channels are peripherals, source incrementation is disabled (BTCTRL.SRCINC=0).

Figure 25-9. Destination Address Increment



Offset	Name	Bit Pos.								
0x2C ... 0x2F	Reserved									
0x30	DEBOUNCEN	7:0	DEBOUNCEN[7:0]							
0x31		15:8	DEBOUNCEN[15:8]							
0x32		23:16	DEBOUNCEN[23:16]							
0x33		31:24	DEBOUNCEN[31:24]							
0x34	DPRESCALER	7:0	STATESx	PRESCALERx[2:0]			STATESx	PRESCALERx[2:0]		
0x35		15:8	STATESx	PRESCALERx[2:0]			STATESx	PRESCALERx[2:0]		
0x36		23:16								TICKON
0x37		31:24								
0x38	PINSTATE	7:0	PINSTATE[7:0]							
0x39		15:8	PINSTATE[15:8]							
0x3A		23:16	PINSTATE[23:16]							
0x3B		31:24	PINSTATE[31:24]							

26.8 Register Description

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16-, and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly.

Some registers require synchronization when read and/or written. Synchronization is denoted by the "Read-Synchronized" and/or "Write-Synchronized" property in each individual register description.

Some registers are enable-protected, meaning they can only be written when the module is disabled. Enable-protection is denoted by the "Enable-Protected" property in each individual register description.

26.8.1 Control A

Name: CTRLA
Offset: 0x00
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
				CKSEL			ENABLE	SWRST
Access				RW			RW	W
Reset				0			0	0

Bit 4 – CKSEL: Clock Selection
The EIC can be clocked either by GCLK_EIC (when a frequency higher than 32KHz is required for filtering) or by CLK_ULP32K (when power consumption is the priority).

This bit is not Write-Synchronized.

Bit	31	30	29	28	27	26	25	24
	EXTINT[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	EXTINT[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	EXTINT[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	EXTINT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – EXTINT[31:0]: External Interrupt Enable
The bit x of EXTINT enables the interrupt associated with the EXTINTx pin.

Writing a '0' to bit x has no effect.

Writing a '1' to bit x will clear the External Interrupt Enable bit x, which disables the external interrupt EXTINTx.

Value	Description
0	The external interrupt x is disabled.
1	The external interrupt x is enabled.

26.8.7 Interrupt Enable Set

This register allows the user to enable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Clear (INTENCLR) register.

Name: INTENSET
Offset: 0x10
Reset: 0x00000000
Property: PAC Write-Protection

Figure 28-6. I/O Configuration - Totem-Pole Output with Disabled Input

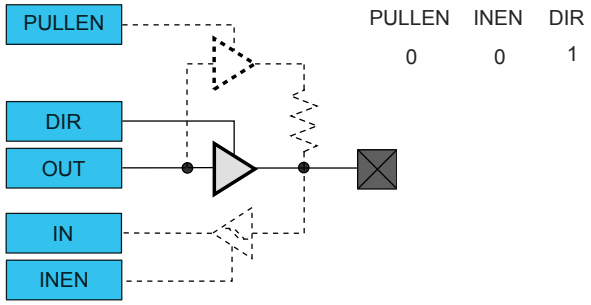


Figure 28-7. I/O Configuration - Totem-Pole Output with Enabled Input

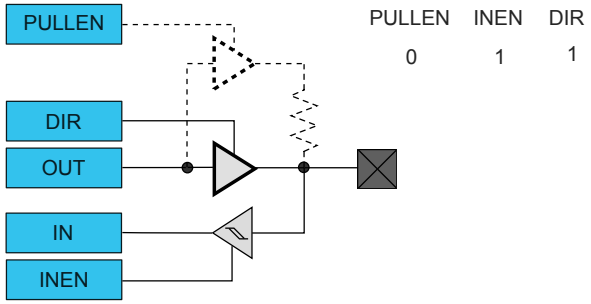
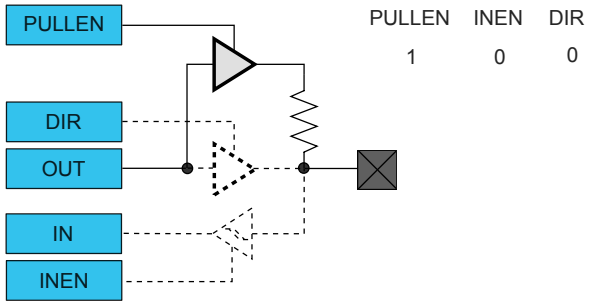


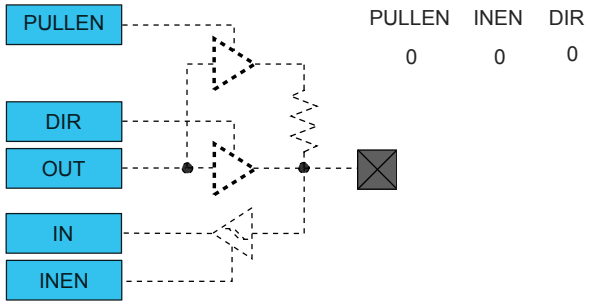
Figure 28-8. I/O Configuration - Output with Pull



28.6.3.4 Digital Functionality Disabled

Neither Input nor Output functionality are enabled.

Figure 28-9. I/O Configuration - Reset or Analog I/O: Digital Output, Input and Pull Disabled



28.6.4 Events

The PORT allows input events to control individual I/O pins. These input events are generated by the EVSYS module and can originate from a different clock domain than the PORT module.

The PORT can perform the following actions:

Value	Description
0	The peripheral multiplexer selection is disabled, and the PORT registers control the direction and output drive value.
1	The peripheral multiplexer selection is enabled, and the selected peripheral function controls the direction and output drive value.

Value	Description
0x00 - 0x7F	Valid values are 0 to 127. The actual interpretation by the hardware of this value is such that one more than the programmed value is used.

Bits 24:16 – NBRP[8:0]: Nominal Baud Rate Prescaler

Value	Description
0x000 - 0x1FF	The value by which the oscillator frequency is divided for generating the bit time quanta. The bit time is built up from a multiple of this quanta. Valid values for the Baud Rate Prescaler are 0 to 511. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used.

Bits 15:8 – NTSEG1[7:0]: Nominal Time segment before sample point

Value	Description
0x00 - 0x7F	Valid values are 1 to 255. The actual interpretation by the hardware of this value is such that one more than the programmed value is used. NTSEG1 is the sum of Prop_Seg and Phase_Seg1.

Bits 6:0 – NTSEG2[6:0]: Time segment after sample point

Value	Description
0x00 - 0x7F	Valid values are 0 to 127. The actual interpretation by the hardware of this value is such that one more than the programmed value is used. NTSEG2 is Phase_Seg2.

34.8.9 Timestamp Counter Configuration

This register is write-restricted and only writable if bit fields CCCR.CCE = 1 and CCCR.INIT = 1.

Name: TSCC
Offset: 0x20 [ID-0000a4bb]
Reset: 0x00000000
Property: Write-restricted

36. TCC – Timer/Counter for Control Applications

36.1 Overview

The device provides three instances of the Timer/Counter for Control applications (TCC) peripheral, TCC[2:0].

Each TCC instance consists of a counter, a prescaler, compare/capture channels and control logic. The counter can be set to count events or clock pulses. The counter together with the compare/capture channels can be configured to time stamp input events, allowing capture of frequency and pulse-width. It can also perform waveform generation such as frequency generation and pulse-width modulation.

Waveform extensions are featured for motor control, ballast, LED, H-bridge, power converters, and other types of power control applications. They allow for low- and high-side output with optional dead-time insertion. Waveform extensions can also generate a synchronized bit pattern across the waveform output pins. The fault options enable fault protection for safe and deterministic handling, disabling and/or shut down of external drivers.

Figure 36-1 shows all features in TCC.

Note: The TCC configurations, such as channel numbers and features, may be reduced for some of the TCC instances.

Related Links

TCC Configurations

36.2 Features

- Up to four compare/capture channels (CC) with:
  - Double buffered period setting
  - Double buffered compare or capture channel
  - Circular buffer on period and compare channel registers
- Waveform generation:
  - Frequency generation
  - Single-slope pulse-width modulation (PWM)
  - Dual-slope pulse-width modulation with half-cycle reload capability
- Input capture:
  - Event capture
  - Frequency capture
  - Pulse-width capture
- Waveform extensions:
  - Configurable distribution of compare channels outputs across port pins
  - Low- and high-side output with programmable dead-time insertion
  - Waveform swap option with double buffer support
  - Pattern generation with double buffer support
  - Dithering support
- Fault protection for safe disabling of drivers:
  - Two recoverable fault sources

Symbol	Parameter	Conditions		Measurement			Unit
				Min	Typ	Max	
			Vddana=5.0V Vref=Vddana		+/-0.2	+/-23	
Tco	Offset Drift	Fadc = 1 Msps	Vddana=5.0V Vref=Vddana	20	80	120	µV/°C
SFDR		Spurious Free Dynamic Range	Fs = 1Msps / Fin = 14 kHz / Full range Input signal Vddana=5.0V Vref=Vddana	71	75	81	dB
SINAD		Signal to Noise and Distortion ratio		65	67	68	
SNR		Signal to Noise ratio		67	68	69	
THD				-77	-74	-70	
		Noise RMS	External Reference voltage	-	0.5	2.0	mV

1. These values are based on characterization. These values are not covered by test limits in production.
2. For best ENOB with external reference, comparator offset cancellation is recommended to be turned off (SAMPCTRL.OFFCOMP=0).

Table 45-20. Single-Ended Mode(1)

Symbol	Parameter	Conditions		Measurement			Unit
				Min	Typ	Max	
ENOB(2)	Effective Number of bits	Fadc = 500 ksps	Vddana=5.0V Vref=Vddana	9.1	9.7	10.0	bits
			Vddana=2.7V Vref=2.0V	9.1	9.4	9.8	
		Fadc = 1 Msps	Vddana=5.0V Vref=Vddana	9.1	9.7	9.9	
			Vddana=2.7V Vref=2.0V	9.0	9.2	9.6	
TUE	Total Unadjusted Error	Fadc = 500 ksps	Vddana=5.0V Vref=Vddana	-	18.0	65.0	LSB
			Vddana=2.7V Vref=2.0V	-	30.2	62.0	
		Fadc = 1 Msps	Vddana=5.0V Vref=Vddana	-	18.4	60.0	

Symbol	Parameters	Conditions	Ta	Typ.	Max	Units
		fs = 10 ksps / Reference buffer disabled / BIASREFBUF = '111', BIASREFCOMP = '111' VDDANA=Vref= 5.5V		437	528	
		fs = 10 ksps / Reference buffer enabled / BIASREFBUF = '111', BIASREFCOMP = '111' VDDANA=Vref= 5.5V		553	675	

1. These are based on characterization.

45.10.5 Sigma-Delta Analog-to-Digital Converter (SDADC) Characteristics

Table 45-22. Operating Conditions(1)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
Res	Resolution	Differential mode	-	16	-	bits
		Single-Ended mode	-	15	-	
CLK_SDADC	Sampling Clock Speed		1	-	6	MHz
CLK_SDADC_FS	Conversion rate		CLK_SDADC/4			
fs	Output Data Rate	Free running mode	CLK_SDADC_FS / OSR			
		Single conversion mode SKPCNT = N	(CLK_SDADC_FS / OSR) x (N+1)			
OSR	Oversampling ratio	Differential mode	64	256	1024	Cycles
	Input Conversion range	Differential mode Gaincorr = 0x1	-0.7xVREF	-	0.7xVREF	V
		Single-Ended mode Gaincorr = 0x1	0	-	0.7xVREF	
Vref	Reference voltage range		1	-	5.5	V
Vcom	Common mode voltage	Differential mode	0	-	AVDD	V
Cin	Input capacitance		0.425	0,5	0.575	pF
Zin	Input impedance	Differential mode	1/(Cin x CLK_SDADC_FS)			kΩ

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
t_{MOH}	MOSI hold after SCK	Master, VDD>4.5V		2.5	-	-	ns
		Master, VDD>2.7V		2.5	-	-	
t_{SSCK}	Slave SCK Period	Slave	Reception	$2*(t_{SIS}+t_{MASTER\_OUT})$ (5)	-	-	ns
		Slave	Transmission	$2*(t_{SOV}+t_{MASTER\_IN})$ (6)	-	-	
t_{SSCKW}	SCK high/low width	Slave		-	$0.5*t_{SSCK}$	-	ns
t_{SSCKR}	SCK rise time (2)	Slave		-	$0.25*t_{SSCK}$	-	ns
t_{SSCKF}	SCK fall time (2)	Slave		-	$0.25*t_{SSCK}$	-	ns
t_{SIS}	MOSI setup to SCK	Slave, VDD>4.5V		13.6	-	-	ns
		Slave, VDD>2.7V		14.1	-	-	
t_{SIH}	MOSI hold after SCK	Slave, VDD>4.5V		0	-	-	ns
		Slave, VDD>2.7V		0	-	-	
t_{SSS}	SS setup to SCK	Slave	PRELOADEN=1	$t_{SOSS}+t_{EXT\_MIS}+2*t_{APBC}$ (8) (9)	-	-	ns
			PRELOADEN=0	$t_{SOSS}+t_{EXT\_MIS}$ (8)	-	-	
t_{SSH}	SS hold after SCK	Slave		$0.5*t_{SSCK}$	-	-	ns
t_{SOV}	MISO output valid SCK	Slave, VDD>4.5V		-	-	45	ns
		Slave, VDD>2.7V	-	-	55.1		
t_{SOH}	MISO hold after SCK	Slave, VDD>4.5V		11.9	-	-	ns
		Slave, VDD>2.7V	11.9	-	-		
t_{SOSS}	MISO setup after SS low	Slave, VDD>4.5V		-	-	41	ns
		Slave, VDD>2.7V		-	-	50.7	
t_{SOSH}	MISO hold after SS high	Slave, VDD>4.5V		11.1	-	-	ns
		Slave, VDD>2.7V		11.1	-	-	

1. These values are based on simulation. These values are not covered by test limits in production.
2. See I/O pin characteristics.
3. Where t_{SLAVE_OUT} is the slave external device output response time, generally $t_{EXT\_SOV}+t_{LINE\_DELAY}$ (7).
4. Where t_{SLAVE_IN} is the slave external device input constraint, generally $t_{EXT\_SIS}+t_{LINE\_DELAY}$ (7).
5. Where t_{MASTER_OUT} is the master external device output response time, generally $t_{EXT\_MOV}+t_{LINE\_DELAY}$ (7).
6. Where t_{MASTER_IN} is the master external device input constraint, generally $t_{EXT\_MIS}+t_{LINE\_DELAY}$ (7).
7. t_{LINE_DELAY} is the transmission line time delay.
8. t_{EXT_MIS} is the input constraint for the master external device.
9. t_{APBC} is the APB period for SERCOM.

1. The EEPROM emulation is a software emulation described in the application note AT03265.
2. An endurance cycle is a write and an erase operation.

46.6 Oscillator Characteristics

46.6.1 Crystal Oscillator (XOSC) Characteristics

Table 46-12. Power Consumption(1)

Symbol	Parameters	Conditions		T_A	Typ.	Max	Units
IDD	Current consumption	F = 2MHz CL=20pF XOSC.GAIN=0 VDD = 5.0V	AGC=OFF	Max 105°C Typ 25°C	150	206	µA
			AGC=ON		138	198	
		F = 4MHz CL=20pF XOSC.GAIN=1 VDD = 5.0V	AGC=OFF		220	293	
			AGC=ON		175	267	
		F = 8MHz CL=20pF XOSC.GAIN=2 VDD = 5.0V	AGC=OFF		350	425	
			AGC=ON		247	331	
		F = 16MHz CL=20pF XOSC.GAIN=3 VDD = 5.0V	AGC=OFF		663	861	
			AGC=ON		429	725	
		F = 32MHz CL=20pF XOSC.GAIN=4 VDD = 5.0V	AGC=OFF		1975	2397	
			AGC=ON		874	1252	

1. These are based on characterization

46.6.2 External 32kHz Crystal Oscillator (XOSC32K) Characteristics

Table 46-13. Power Consumption(1)

Symbol	Parameters	Conditions	Ta	Typ.	Max	Units
IDD	Current consumption	V_{DD} = 5.0V	Max 105°C Typ 25°C	1528	1740	nA

47.6 Oscillator Characteristics

47.6.1 Crystal Oscillator (XOSC) Characteristics

The following table describes the characteristics for the oscillator when a digital clock is applied on XIN.

Table 47-18. Digital Clock Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{CPXIN}	XIN clock frequency	Digital mode	-	-	48	MHz
DC_{XIN}(1)	XIN clock duty cycle	Digital mode	40	50	60	%

1. These are based on simulation. These values are not covered by test or characterization

The following table describes the characteristics for the oscillator when a crystal is connected between XIN and XOUT as shown in the figure belwo. The user must choose a crystal oscillator where the crystal load capacitance C_L is within the range given in the table. The exact value of C_L can be found in the crystal datasheet. The capacitance of the external capacitors (C_{LEXT}) can then be computed as follows:

$$C_{LEXT} = 2(C_L + - C_{STRAY} - C_{SHUNT})$$

where C_{STRAY} is the capacitance of the pins and PCB, C_{SHUNT} is the shunt capacitance of the crystal.

Figure 47-5. Oscillator Connection

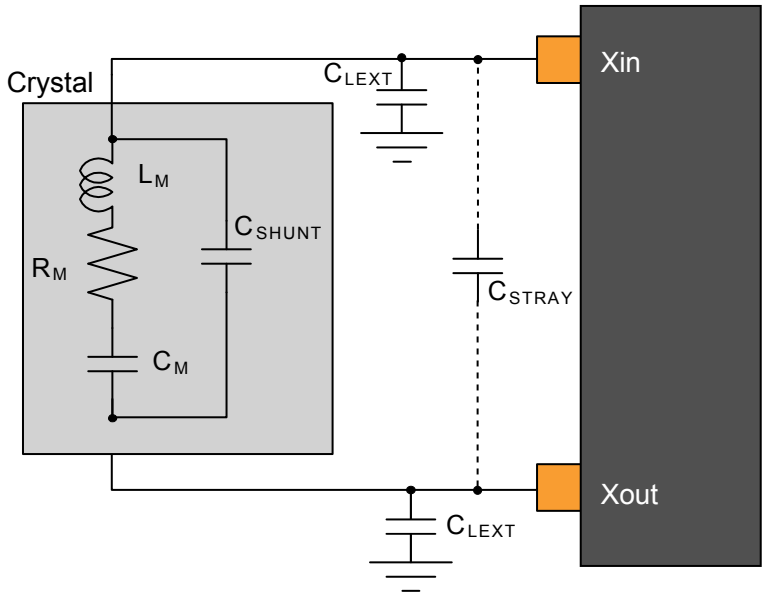


Table 47-19. Multi Crystal Oscillator Electrical Characteristics (1)

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
Fout	Crystal oscillator frequency		0.4	-	32	MHz
ESR	Crystal Equivalent Series Resistance - SF = 3	F = 0.455 MHz CL = 100pF XOSC.GAIN = 0	-	-	443	Ω
		F = 2MHz CL=20pF	-	-	383	