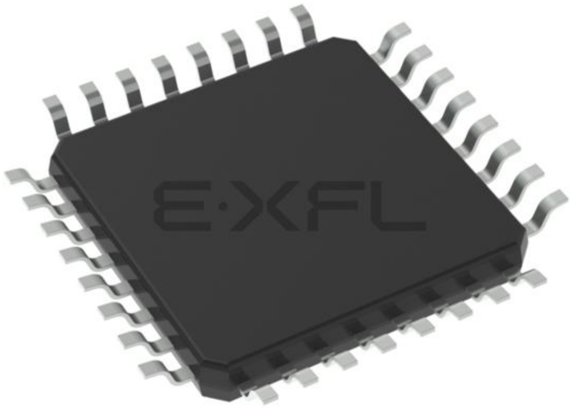

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, WDT
Number of I/O	26
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 10x12b, 1x16b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-TQFP
Supplier Device Package	32-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamc21e16a-aut

Pin	I/O Pin	Supply	A		B	B(1)(2)		C	D	E	F	G	H	I
			EIC	REF	ADC0	AC	PTC	SERCOM	SERCOM-ALT	TC	TCC	COM	AC/GCLK	CCL
71	PA21	VDDIO	EXTINT[5]				X[9]/Y[25]	SERCOM5/PAD[3]	SERCOM3/PAD[3]	TC7/WO[1]	TCC2/WO[1]		GCLK_IO[5]	
72	PA22	VDDIO	EXTINT[6]				X[10]/Y[26]	SERCOM3/PAD[0]	SERCOM5/PAD[0]	TC4/WO[0]	TCC1/WO[0]		GCLK_IO[6]	CCL2/IN[6]
73	PA23	VDDIO	EXTINT[7]				X[11]/Y[27]	SERCOM3/PAD[1]	SERCOM5/PAD[1]	TC4/WO[1]	TCC1/WO[1]		GCLK_IO[7]	CCL2/IN[7]
74	PA24	VDDIO	EXTINT[12]					SERCOM3/PAD[2]	SERCOM5/PAD[2]	TC5/WO[0]	TCC2/WO[0]		CMP[2]	CCL2/IN[8]
75	PA25	VDDIO	EXTINT[13]					SERCOM3/PAD[3]	SERCOM5/PAD[3]	TC5/WO[1]	TCC2/WO[1]		CMP[3]	CCL2/OUT[2]
78	PB22	VDDIO	EXTINT[6]					SERCOM0/PAD[2]	SERCOM5/PAD[2]	TC7/WO[0]	TCC1/WO[2]		GCLK_IO[0]	CCL0/IN[0]
79	PB23	VDDIO	EXTINT[7]					SERCOM0/PAD[3]	SERCOM5/PAD[3]	TC7/WO[1]	TCC1/WO[3]		GCLK_IO[1]	CCL0/OUT[0]
80	PB24	VDDIO	EXTINT[8]					SERCOM0/PAD[0]	SERCOM4/PAD[0]				CMP[0]	
81	PB25	VDDIO	EXTINT[9]					SERCOM0/PAD[1]	SERCOM4/PAD[1]				CMP[1]	
82	PC24	VDDIO	EXTINT[0]					SERCOM0/PAD[2]	SERCOM4/PAD[2]					
83	PC25	VDDIO	EXTINT[1]					SERCOM0/PAD[3]	SERCOM4/PAD[3]					
84	PC26	VDDIO	EXTINT[2]											
85	PC27	VDDIO	EXTINT[3]						SERCOM1/PAD[0]					CCL1/IN[4]
86	PC28	VDDIO	EXTINT[4]						SERCOM1/PAD[1]					CCL1/IN[5]
87	PA27	VDDIN	EXTINT[15]										GCLK_IO[0]	
89	PA28	VDDIN	EXTINT[8]										GCLK_IO[0]	
93	PA30	VDDIN	EXTINT[10]						SERCOM1/PAD[2]	TC1/WO[0]		CORTEX_M0P/SWCLK	GCLK_IO[0]	CCL1/IN[3]
94	PA31	VDDIN	EXTINT[11]						SERCOM1/PAD[3]	TC1/WO[1]		CORTEX_M0P/SWDIO		CCL1/OUT[1]
95	PB30	VDDIN	EXTINT[14]					SERCOM1/PAD[0]	SERCOM5/PAD[0]	TC0/WO[0]			CMP[2]	
96	PB31	VDDIN	EXTINT[15]					SERCOM1/PAD[1]	SERCOM5/PAD[1]	TC0/WO[1]			CMP[3]	
97	PB00	VDDANA	EXTINT[0]				Y[6]		SERCOM5/PAD[2]	TC7/WO[0]				CCL0/IN[1]
98	PB01	VDDANA	EXTINT[1]				Y[7]		SERCOM5/PAD[3]	TC7/WO[1]				CCL0/IN[2]
99	PB02	VDDANA	EXTINT[2]				Y[8]		SERCOM5/PAD[0]	TC6/WO[0]				CCL0/OUT[0]
100	PB03	VDDANA	EXTINT[3]				Y[9]		SERCOM5/PAD[1]	TC6/WO[1]				

1. All analog pin functions are on peripheral function B. Peripheral function B must be selected to disable the digital control of the pin.
2. Only some pins can be used in SERCOM I2C mode. Refer to SERCOM I2C Pins.

Table 6-4. PORT Function Multiplexing for SAM C20 E/G/J

	Pin(1)		I/O Pin	Supply	A			B(2)(3)		C	D	E	F	G	H	I
SAM C20E	SAM C20G	SAM C20J			EIC	REF	ADC0	AC	PTC	SERCOM(2)(3)(4)	SERCOM-ALT(4)	TC TCC	TCC	COM	AC/GCLK	CCL
1	1	1	PA00	VDDANA	EXTINT[0]						SERCOM1/PAD[0]	TCC2/WO[0]			CMP[2]	
2	2	2	PA01	VDDANA	EXTINT[1]						SERCOM1/PAD[1]	TCC2/WO[1]			CMP[3]	
3	3	3	PA02	VDDANA	EXTINT[2]		AIN[0]	AIN[4]	Y[0]							
4	4	4	PA03	VDDANA	EXTINT[3]	ADC/VREFA	AIN[1]	AIN[5]	Y[1]							
		5	PB04	VDDANA	EXTINT[4]				Y[10]							
		6	PB05	VDDANA	EXTINT[5]			AIN[6]	Y[11]							
		9	PB06	VDDANA	EXTINT[6]			AIN[7]	Y[12]							CCL2/IN[6]
		10	PB07	VDDANA	EXTINT[7]				Y[13]							CCL2/IN[7]
	7	11	PB08	VDDANA	EXTINT[8]		AIN[2]		Y[14]		SERCOM4/PAD[0]	TC0/WO[0]				CCL2/IN[8]
	8	12	PB09	VDDANA	EXTINT[9]		AIN[3]		Y[15]		SERCOM4/PAD[1]	TC0WO[1]				CCL2/OUT[2]
5	9	13	PA04	VDDANA	EXTINT[4]		AIN[4]	AIN[0]	Y[2]		SERCOM0/PAD[0]	TCC0/WO[0]				CCL0/IN[0]
6	10	14	PA05	VDDANA	EXTINT[5]		AIN[5]	AIN[1]	Y[3]		SERCOM0/PAD[1]	TCC0/WO[1]				CCL0/IN[1]
7	11	15	PA06	VDDANA	EXTINT[6]		AIN[6]	AIN[2]	Y[4]		SERCOM0/PAD[2]	TCC1/WO[0]				CCL0/IN[2]
8	12	16	PA07	VDDANA	EXTINT[7]		AIN[7]	AIN[3]	Y[5]		SERCOM0/PAD[3]	TCC1/WO[1]				CCL0/OUT[0]
11	13	17	PA08	VDDIO	NMI		AIN[8]		X[0]/Y[16]	SERCOM0/PAD[0]	SERCOM2/PAD[0]	TCC0/WO[0]	TCC1/WO[2]			CCL1/IN[3]
12	14	18	PA09	VDDIO	EXTINT[9]		AIN[9]		X[1]/Y[17]	SERCOM0/PAD[1]	SERCOM2/PAD[1]	TCC0/WO[1]	TCC1/WO[3]			CCL1/IN[4]
13	15	19	PA10	VDDIO	EXTINT[10]		AIN[10]		X[2]/Y[18]	SERCOM0/PAD[2]	SERCOM2/PAD[2]	TCC1/WO[0]	TCC0/WO[2]		GCLK_IO[4]	CCL1/IN[5]
14	16	20	PA11	VDDIO	EXTINT[11]		AIN[11]		X[3]/Y[19]	SERCOM0/PAD[3]	SERCOM2/PAD[3]	TCC1/WO[1]	TCC0/WO[3]		GCLK_IO[5]	CCL1/OUT[1]
	19	23	PB10	VDDIO	EXTINT[10]						SERCOM4/PAD[2]	TC1/WO[0]	TCC0/WO[4]		GCLK_IO[4]	CCL1/IN[5]
	20	24	PB11	VDDIO	EXTINT[11]						SERCOM4/PAD[3]	TC1/WO[1]	TCC0/WO[5]		GCLK_IO[5]	CCL1/OUT[1]

This flag is cleared by writing a one to the flag.

This flag is set when a Peripheral Access Error occurs while accessing the peripheral associated with the respective INTFLAGD bit, and will generate an interrupt request if INTENCLR/SET.ERR is one.

Writing a zero to this bit has no effect.

Writing a one to this bit will clear the corresponding INTFLAGD interrupt flag.

Name: INTFLAGD
Offset: 0x20 [ID-00000a18]
Reset: 0x000000
Property: –

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
				TC7	TC6	TC5	SERCOM7	SERCOM6
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 2, 3, 4 – TC5, TC6, TC7: Interrupt Flag for TCn [n = 7..5]

Bits 0, 1 – SERCOM6, SERCOM7: Interrupt Flag for SERCOMn [n = 7..6]

11.7.10 Peripheral Write Protection Status A

Writing to this register has no effect.

Reading STATUS register returns peripheral write protection status:

Value	Description
0	Peripheral is not write protected.
1	Peripheral is write protected.

Value	Description
0	Peripheral is not write protected.
1	Peripheral is write protected.

Name: STATUSC
Offset: 0x3C [ID-00000a18]
Reset: 0x000000
Property: –

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	CCL	PTC	DAC	AC	SDADC	ADC1	ADC0	TC4
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TC3	TC2	TC1	TC0	TCC2	TC2	TC1	TC0
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CAN0	SERCOM5	SERCOM4	SERCOM3	SERCOM2	SERCOM1	SERCOM0	EVSYS
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit 23 – CCL: Peripheral CCL Write Protection Status

Bit 22 – PTC: Peripheral PTC Write Protection Status

Bit 21 – DAC: Peripheral DAC Write Protection Status

Bit 20 – AC: Peripheral AC Write Protection Status

Bit 19 – SDADC: Peripheral SDADC Write Protection Status

Bits 17, 18 – ADC: Peripheral ADCn [n=1..0] Write Protection Status

Bits 12, 13, 14, 15, 16 – TC: Peripheral TCn Write Protection Status [n = 4..0]

Bits 9, 10, 11 – TCC: Peripheral TCCn [n = 2..0] Write Protection Status TCCn [n = 2..0]

Bits 8, 9, 10 – TC: Peripheral TCn Write Protection Status [n = 2..0]

Bit 7 – CAN: Peripheral CAN Write Protection Status

13.13 Register Description

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16- and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly.

Some registers are optionally write-protected by the Peripheral Access Controller (PAC). Optional PAC write-protection is denoted by the "PAC Write-Protection" property in each individual register description. For details, refer to Register Access Protection.

13.13.1 Control

Name: CTRL
Offset: 0x0000 [ID-00001c14]
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
				CE	MBIST		CRC	SWRST
Access				W	W		W	W
Reset				0	0		0	0

Bit 4 – CE: Chip-Erase
Writing a '0' to this bit has no effect.

Writing a '1' to this bit starts the Chip-Erase operation.

Bit 3 – MBIST: Memory Built-In Self-Test
Writing a '0' to this bit has no effect.

Writing a '1' to this bit starts the memory BIST algorithm.

Bit 1 – CRC: 32-bit Cyclic Redundancy Check
Writing a '0' to this bit has no effect.

Writing a '1' to this bit starts the cyclic redundancy check algorithm.

Bit 0 – SWRST: Software Reset
Writing a '0' to this bit has no effect.

Writing a '1' to this bit resets the module.

13.13.2 Status A

Name: STATUSA
Offset: 0x0001
Reset: 0x00
Property: PAC Write-Protection

Value	Description
0	The APBB clock for the NVMCTRL is stopped
1	The APBB clock for the NVMCTRL is enabled

Bit 1 – DSU: DSU APBB Clock Enable

Value	Description
0	The APBB clock for the DSU is stopped
1	The APBB clock for the DSU is enabled

Bit 0 – PORT: PORT APBB Clock Enable

Value	Description
0	The APBB clock for the PORT is stopped.
1	The APBB clock for the PORT is enabled.

17.8.9 APBC Mask

Name: APBCMASK
Offset: 0x1C
Reset: 0x00000000
Property: PAC Write-Protection

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	CCL	PTC	DAC	AC	SDADC	ADC1	ADC0	TC4
Access	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TC3	TC2	TC1	TC0	TCC2	TCC1	TCC0	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	

Bit	7	6	5	4	3	2	1	0
		SERCOM5	SERCOM4	SERCOM3	SERCOM2	SERCOM1	SERCOM0	EVSYS
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit 23 – CCL: CCL APBC Clock Enable

Value	Description
0	The APBC clock for the CCL is stopped.
1	The APBC clock for the CCL is enabled.

Bit 22 – PTC: PTC APBC Mask Clock Enable

19.5.3 DMA

Not applicable.

19.5.4 Interrupts

The interrupt request line is connected to the interrupt controller. Using the PM interrupt requires the interrupt controller to be configured first.

19.5.5 Events

Not applicable.

19.5.6 Debug Operation

When the CPU is halted in debug mode, the PM continues normal operation. If standby sleep mode is requested by the system while in debug mode, the power domains are not turned off. As a consequence, power measurements while in debug mode are not relevant.

Hot plugging in standby mode is supported.

19.5.7 Register Access Protection

Registers with write-access can be write-protected optionally by the peripheral access controller (PAC).

Optional PAC Write-Protection is denoted by the "PAC Write-Protection" property in each individual register description.

Write-protection does not apply to accesses through an external debugger.

19.5.8 Analog Connections

Not applicable.

19.6 Functional Description

19.6.1 Terminology

The following is a list of terms used to describe the Power Managemement features of this microcontroller.

19.6.1.1 Sleep Modes

The device can be set in a sleep mode. In sleep mode, the CPU is stopped and the peripherals are either active or idle, according to the sleep mode depth:

- Idle sleep mode: The CPU is stopped. Synchronous clocks are stopped except when requested. The logic is retained.
- Standby sleep mode: The CPU is stopped as well as the peripherals.

19.6.2 Principle of Operation

In active mode, all clock domains and power domains are active, allowing software execution and peripheral operation. The PM Sleep Mode Controller allows to save power by choosing between different sleep modes depending on application requirements, see Sleep Mode Controller.

The PM Power Domain Controller allows to reduce the power consumption in standby mode even further.

19.6.3 Basic Operation

19.6.3.1 Initialization

After a power-on reset, the PM is enabled, the device is in ACTIVE mode.

Bit 8 – DPLLLCKR: DPLL Lock Rise Interrupt Enable
Writing '0' to this bit has no effect.

Writing '1' to this bit will set the DPLL Lock Rise Interrupt Enable bit, which enables the DPLL Lock Rise interrupt.

Value	Description
0	The DPLL Lock Rise interrupt is disabled.
1	The DPLL Lock Rise interrupt is enabled, and an interrupt request will be generated when the DPLL Lock Rise Interrupt flag is set.

Bit 4 – OSC48MRDY: OSC48M Ready Interrupt Enable
Writing '0' to this bit has no effect.

Writing '1' to this bit will set the OSC48M Ready Interrupt Enable bit, which enables the OSC48M Ready interrupt.

Value	Description
0	The OSC48M Ready interrupt is disabled.
1	The OSC48M Ready interrupt is enabled, and an interrupt request will be generated when the OSC48M Ready Interrupt flag is set.

Bit 1 – CLKFAIL: XOSC Clock Failure Interrupt Enable
Writing '0' to this bit has no effect.

Writing '1' to this bit will set the XOSC Clock Failure Interrupt Enable bit, which enables the XOSC Clock Failure Interrupt.

Value	Description
0	The XOSC Clock Failure Interrupt is disabled.
1	The XOSC Clock Failure Interrupt is enabled, and an interrupt request will be generated when the XOSC Clock Failure Interrupt flag is set.

Bit 0 – XOSCRDY: XOSC Ready Interrupt Enable
Writing '0' to this bit has no effect.

Writing '1' to this bit will set the XOSC Ready Interrupt Enable bit, which enables the XOSC Ready interrupt.

Value	Description
0	The XOSC Ready interrupt is disabled.
1	The XOSC Ready interrupt is enabled, and an interrupt request will be generated when the XOSC Ready Interrupt flag is set.

20.8.3 Interrupt Flag Status and Clear

Name: INTFLAG
Offset: 0x08 [ID-00001eee]
Reset: 0x00000000
Property: -

Event

If the Event Output Enable bit in the Event Control register (EVCTRL.CFDEO) is set, the CFD clock failure will be output on the Event Output. When the CFD is switched to the safe clock, the CFD clock failure will not be output on the Event Output.

Sleep Mode

The CFD is halted depending on configuration of the XOSC32K and the peripheral clock request. For further details, refer to the Sleep Behavior table above. The CFD interrupt can be used to wake up the device from sleep modes.

21.6.4 32KHz Internal Oscillator (OSC32K) Operation

The OSC32K provides a tunable, low-speed, and low-power clock source.

At reset, the OSC32K is disabled. It can be enabled by setting the Enable bit in the 32KHz Internal Oscillator Control register (OSC32K.ENABLE=1). The OSC32K is disabled by clearing the Enable bit in the 32KHz Internal Oscillator Control register (OSC32K.ENABLE=0).

The frequency of the OSC32K oscillator is controlled by OSC32K.CALIB, which is a calibration value in the 32KHz Internal Oscillator Calibration bits in the 32KHz Internal Oscillator Control register. The CALIB value must be must be loaded with production calibration values from the NVM Software Calibration Area. When writing the Calibration bits, the user must wait for the STATUS.OSC32KRDY bit to go high before the new value is committed to the oscillator.

The OSC32K has a 32.768kHz output which is enabled by setting the 32KHz Output Enable bit in the 32KHz Internal Oscillator Control register (OSC32K.EN32K=1). The OSC32K also has a 1.024kHz clock output. This is enabled by setting the 1KHz Output Enable bit in the 32KHz Internal Oscillator Control register (OSC32K.EN1K).

Before using the OSC32K, the Calibration field in the OSC32K register (OSC32K.CALIB) must be loaded with production calibration values from the NVM Software Calibration Area.

The OSC32K will behave differently in different sleep modes based on the settings of OSC32K.RUNSTDBY, OSC32K.ONDEMAND, and OSC32K.ENABLE. If OSC32KCTRL.ENABLE=0, the OSC32K will be always stopped. For OS32KCTRL.ENABLE=1, this table is valid:

Table 21-2. OSC32K Sleep Behavior

CPU Mode	OSC32KCTRL.RUNSTDBY	OSC32KCTRL.ONDEMAND	Sleep Behavior
Active or Idle	-	0	Always run
Active or Idle	-	1	Run if requested by peripheral
Standby	1	0	Always run
Standby	1	1	Run if requested by peripheral
Standby	0	-	Run if requested by peripheral

The OSC32K requires a start-up time. For this reason, OSC32K will keep running across resets when OSC32K.ONDEMAND=0, except for power-on reset (POR).

After such a reset, or when waking up from a sleep mode where the OSC32K was disabled, the OSC32K will need a certain amount of time to stabilize on the correct frequency.

Bit 7 – ONDEMAND: On Demand Control
This bit controls how the XOSC32K behaves when a peripheral clock request is detected. For details, refer to XOSC32K Sleep Behavior.

Bit 6 – RUNSTDBY: Run in Standby
This bit controls how the XOSC32K behaves during standby sleep mode. For details, refer to XOSC32K Sleep Behavior.

Bit 4 – EN1K: 1KHz Output Enable

Value	Description
0	The 1KHz output is disabled.
1	The 1KHz output is enabled.

Bit 3 – EN32K: 32KHz Output Enable

Value	Description
0	The 32KHz output is disabled.
1	The 32KHz output is enabled.

Bit 2 – XTALEN: Crystal Oscillator Enable
This bit controls the connections between the I/O pads and the external clock or crystal oscillator.

Value	Description
0	External clock connected on XIN32. XOUT32 can be used as general-purpose I/O.
1	Crystal connected to XIN32/XOUT32.

Bit 1 – ENABLE: Oscillator Enable

Value	Description
0	The oscillator is disabled.
1	The oscillator is enabled.

21.8.6 Clock Failure Detector Control

Name: CFDCTRL
Offset: 0x16
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
						CFDPRESC	SWBACK	CFDEN
Access						R/W	R/W	R/W
Reset						0	0	0

Bit 2 – CFDPRESC: Clock Failure Detector Prescaler
This bit selects the prescaler for the Clock Failure Detector.

Value	Description
0	The CFD safe clock frequency is the OSCULP32K frequency
1	The CFD safe clock frequency is the OSCULP32K frequency divided by 2

24.7 Register Summary - COUNT32

Offset	Name	Bit Pos.								
0x00	CTRLA	7:0	MATCHCLR				MODE[1:0]		ENABLE	SWRST
0x01		15:8	COUNTSYNC				PRESCALER[3:0]			
0x02 ... 0x03	Reserved									
0x04	EVCTRL	7:0	PEREOn	PEREOn	PEREOn	PEREOn	PEREOn	PEREOn	PEREOn	PEREOn
0x05		15:8	OVFEO							CMPEO0
0x06		23:16								
0x07		31:24								
0x08	INTENCLR	7:0	PERn	PERn	PERn	PERn	PERn	PERn	PERn	PERn
0x09		15:8	OVF							CMP0
0x0A	INTENSET	7:0	PERn	PERn	PERn	PERn	PERn	PERn	PERn	PERn
0x0B		15:8	OVF							CMP0
0x0C	INTFLAG	7:0	PERn	PERn	PERn	PERn	PERn	PERn	PERn	PERn
0x0D		15:8	OVF							CMP0
0x0E	DBGCTRL	7:0								DBGRUN
0x0F	Reserved									
0x10	SYNCBUSY	7:0			COMP0		COUNT	FREQCORR	ENABLE	SWRST
0x11		15:8	COUNTSYNC							
0x12		23:16								
0x13		31:24								
0x14	FREQCORR	7:0	SIGN	VALUE[6:0]						
0x15 ... 0x17	Reserved									
0x18	COUNT	7:0	COUNT[7:0]							
0x19		15:8	COUNT[15:8]							
0x1A		23:16	COUNT[23:16]							
0x1B		31:24	COUNT[31:24]							
0x1C ... 0x1F	Reserved									
0x20	COMP0	7:0	COMP[7:0]							
0x21		15:8	COMP[15:8]							
0x22		23:16	COMP[23:16]							
0x23		31:24	COMP[31:24]							

24.8 Register Description - COUNT32

This Register Description section is valid if the RTC is in COUNT32 mode (CTRLA.MODE=0).

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16-, and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly.

Bit	31	30	29	28	27	26	25	24
	EXTINT[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	EXTINT[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	EXTINT[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	EXTINT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – EXTINT[31:0]: External Interrupt Enable
The bit x of EXTINT enables the interrupt associated with the EXTINTx pin.

Writing a '0' to bit x has no effect.

Writing a '1' to bit x will set the External Interrupt Enable bit x, which enables the external interrupt EXTINTx.

Value	Description
0	The external interrupt x is disabled.
1	The external interrupt x is enabled.

26.8.8 Interrupt Flag Status and Clear

Name: INTFLAG
Offset: 0x14
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
					EVDn	EVDn	EVDn	EVDn
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	23	22	21	20	19	18	17	16
	EVDn	EVDn	EVDn	EVDn	EVDn	EVDn	EVDn	EVDn
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
					OVRn	OVRn	OVRn	OVRn
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	OVRn	OVRn	OVRn	OVRn	OVRn	OVRn	OVRn	OVRn
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 27:16 – EVDn: Event Detected Channel n [n=11..0]
This flag is set on the next CLK_EVSYS_APB cycle when an event is being propagated through the channel, and an interrupt request will be generated if INTENCLR/SET.EVDn is '1'.

When the event channel path is asynchronous, the EVDn interrupt flag will not be set.

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the Event Detected Channel n interrupt flag.

Bits 11:0 – OVRn: Overrun Channel n [n=11..0]
This flag is set on the next CLK_EVSYS_APB cycle after an overrun channel condition occurs, and an interrupt request will be generated if INTENCLR/SET.OVRn is '1'.

There are two possible overrun channel conditions:

- One or more of the event users on channel n are not ready when a new event occurs.
- An event happens when the previous event on channel n has not yet been handled by all event users.

When the event channel path is asynchronous, the OVRn interrupt flag will not be set.

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the Overrun Detected Channel n interrupt flag.

Related Links

PAC - Peripheral Access Controller

29.8.6 Software Event

Value	Description
0	Hardware $\overline{SS}$ control is disabled.
1	Hardware $\overline{SS}$ control is enabled.

Bit 9 – SSDE: Slave Select Low Detect Enable
This bit enables wake up when the slave select ($\overline{SS}$) pin transitions from high to low.

Value	Description
0	$\overline{SS}$ low detector is disabled.
1	$\overline{SS}$ low detector is enabled.

Bit 6 – PLOADEN: Slave Data Preload Enable
Setting this bit will enable preloading of the slave shift register when there is no transfer in progress. If the $\overline{SS}$ line is high when DATA is written, it will be transferred immediately to the shift register.

Bits 2:0 – CHSIZE[2:0]: Character Size

CHSIZE[2:0]	Name	Description
0x0	8BIT	8 bits
0x1	9BIT	9 bits
0x2-0x7	-	Reserved

32.8.3 Baud Rate

Name: BAUD
Offset: 0x0C [ID-00000e74]
Reset: 0x00
Property: PAC Write-Protection, Enable-Protected

Bit	7	6	5	4	3	2	1	0
	BAUD[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – BAUD[7:0]: Baud Register
These bits control the clock generation, as described in the *SERCOM Clock Generation – Baud-Rate Generator*.

Related Links

Clock Generation – Baud-Rate Generator

Asynchronous Arithmetic Mode BAUD Value Selection

32.8.4 Interrupt Enable Clear

This register allows the user to disable an interrupt without read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Set register (INTENSET).

Due to the synchronization mechanism between GCLK_CAN and GCLK_CAN_APB domains, there may be a delay of several GCLK_CAN_APB periods between writing to TEST.TX until the new configuration is visible at output pin CAN_TX. This applies also when reading input pin CAN_RX via TEST.RX.

Note: Test modes should be used for production tests or self test only. The software control for pin CAN_TX interferes with all CAN protocol functions. It is not recommended to use test modes for application.

External Loop Back Mode

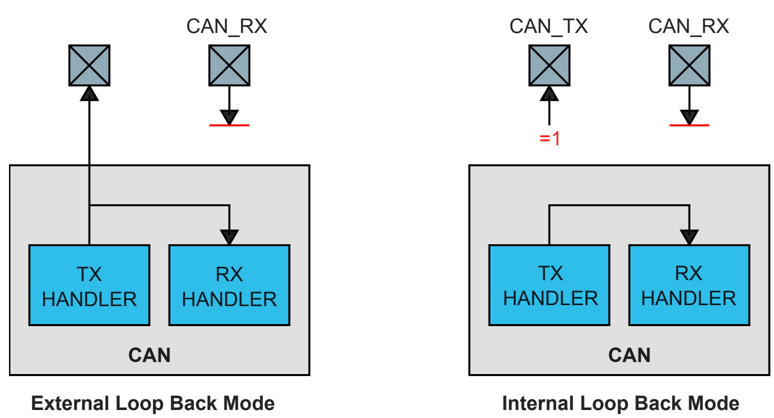
The CAN can be set in External Loop Back Mode by programming TEST.LBCK to ‘1’. In Loop Back Mode, the CAN treats its own transmitted messages as received messages and stores them (if they pass acceptance filtering) into an Rx Buffer or an Rx FIFO. The figure below shows the connection of signals CAN_TX and CAN_RX to the CAN in External Loop Back Mode.

This mode is provided for hardware self-test. To be independent from external stimulation, the CAN ignores acknowledge errors (recessive bit sampled in the acknowledge slot of a data/remote frame) in Loop Back Mode. In this mode the CAN performs an internal feedback from its Tx output to its Rx input. The actual value of the CAN_RX input pin is disregarded by the CAN. The transmitted messages can be monitored at the CAN_TX pin.

Internal Loop Back Mode

Internal Loop Back Mode is entered by programming bits TEST.LBCK and CCCR.MON to ‘1’. This mode can be used for a “Hot Selftest”, meaning the CAN can be tested without affecting a running CAN system connected to the pins CAN_TX and CAN_RX. In this mode pin CAN_RX is disconnected from the CAN and pin CAN_TX is held recessive. The figure below shows the connection of CAN_TX and CAN_RX to the CAN in case of Internal Loop Back Mode.

Figure 34-4. Pin Control in Loop Back Modes



34.6.3 Timestamp Generation

For timestamp generation the CAN supplies a 16-bit wrap-around counter. A prescaler TSCC.TCP can be configured to clock the counter in multiples of CAN bit times (1…16). The counter is readable via TSCV.TSC. A write access to register TSCV resets the counter to zero. When the timestamp counter wraps around interrupt flag IR.TSW is set.

On start of frame reception / transmission the counter value is captured and stored into the timestamp section of an Rx Buffer / Rx FIFO (RXTS[15:0]) or Tx Event FIFO (TXTS[15:0]) element.

To leave low power mode, CLK_CANx_APB and GCLK_CANx must be active before writing CCCR.CSR to '0'. The CAN will acknowledge this by resetting CCCR.CSA = 0. Afterwards, the application can restart CAN communication by resetting bit CCCR.INIT.

34.6.10 Synchronization

Due to the asynchronicity between the main clock domain (CLK_CAN_APB) and the peripheral clock domain (GCLK_CAN) some registers are synchronized when written. When a write-synchronized register is written, the read back value will not be updated until the register has completed synchronization.

The following bits and registers are write-synchronized:

l Initialization bit in CC Control register (CCCR.INIT)

Offset	Name	Bit Pos.								
0x2C	TOCV	7:0	TOC[7:0]							
0x2D		15:8	TOC[15:8]							
0x2E		23:16								
0x2F		31:24								
0x30 ... 0x3F	Reserved									
0x40	ECR	7:0	TEC[7:0]							
0x41		15:8	RP	REC[6:0]						
0x42		23:16	CEL[7:0]							
0x43		31:24								
0x44	PSR	7:0	BO	EW	EP	ACT[1:0]		LEC[2:0]		
0x45		15:8		PXE	RFDF	RBRS	RESI	DLEC[2:0]		
0x46		23:16		TDCV[6:0]						
0x47		31:24								
0x48	TDCR	7:0		TDCF[6:0]						
0x49		15:8		TDCO[6:0]						
0x4A		23:16								
0x4B		31:24								
0x4C ... 0x4F	Reserved									
0x50	IR	7:0	RF1L	RF1F	RF1W	RF1N	RF0L	RF0F	RF0W	RF0N
0x51		15:8	TEFL	TEFF	TEFW	TEFN	TFE	TCF	TC	HPM
0x52		23:16	EP	ELO	BEU	BEC	DRX	TOO	MRAF	TSW
0x53		31:24			ARA	PED	PEA	WDI	BO	EW
0x54	IE	7:0	RF1LE	RF1FE	RF1WE	RF1NE	RF0LE	RF0FE	RF0WE	RF0NE
0x55		15:8	TEFLE	TEFFE	TEFWE	TEFNE	TFEE	TCFE	TCE	HPME
0x56		23:16	EPE	ELOE	BEUE	BECE	DRXE	TOOE	MRAFE	TSWE
0x57		31:24			ARAE	PEDE	PEAE	WDIE	BOE	EWE
0x58	ILS	7:0	RF1LL	RF1FL	RF1WL	RF1NL	RF0LL	RF0FL	RF0WL	RF0NL
0x59		15:8	TEFLL	TEFFL	TEFWL	TEFNL	TFEL	TCFL	TCL	HPML
0x5A		23:16	EPL	ELOL	BEUL	BECL	DRXL	TOOL	MRAFL	TSWL
0x5B		31:24			ARAL	PEDL	PEAL	WDIL	BOL	EWL
0x5C	ILE	7:0							EINTn	EINTn
0x5D		15:8								
0x5E		23:16								
0x5F		31:24								
0x60 ... 0x7F	Reserved									
0x80	GFC	7:0			ANFS[1:0]		ANFE[1:0]		RRFS	RRFE
0x81		15:8								
0x82		23:16								
0x83		31:24								
0x84	SIDFC	7:0	FLSSA[7:0]							
0x85		15:8	FLSSA[15:8]							

Channel Capture (MCx)	For a capture channel, the request is set when valid data is present in the CCx register, and cleared once the CCx register is read. In this operation mode, the CTRLA.DMAOS bit value is ignored.

DMA Operation with Circular Buffer

When circular buffer operation is enabled, the buffer registers must be written in a correct order and synchronized to the update times of the timer. The DMA triggers of the TCC provide a way to ensure a safe and correct update of circular buffers.

Note: Circular buffer are intended to be used with RAMP2, RAMP2A and DSBOTH operation only.

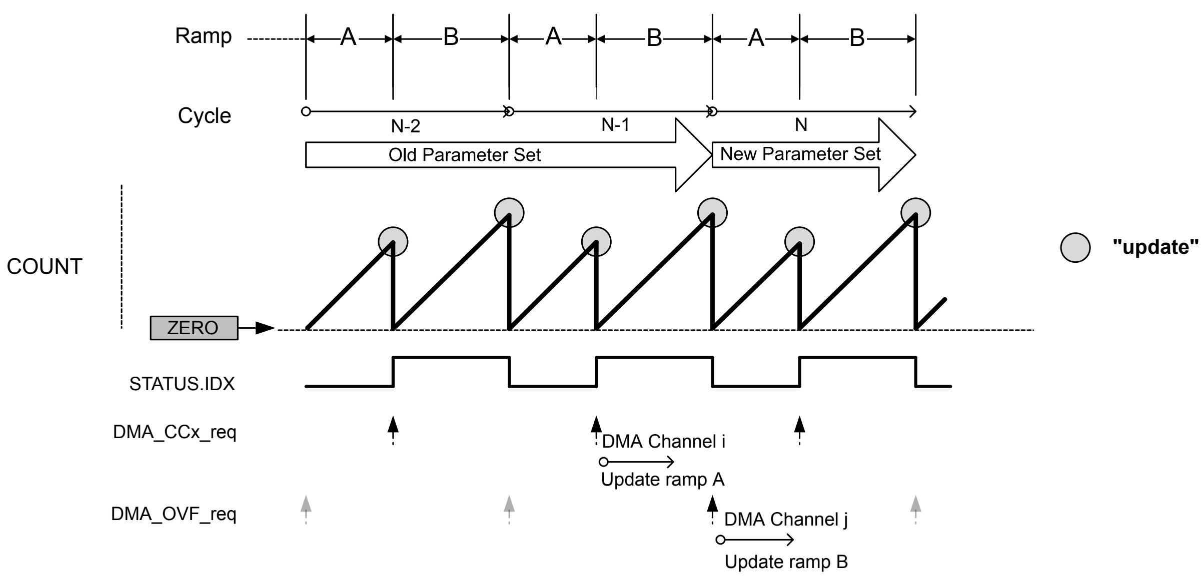
DMA Operation with Circular Buffer in RAMP and RAMP2A Mode

When a CCx channel is selected as a circular buffer, the related DMA request is not set on a compare match detection, but on start of ramp B.

If at least one circular buffer is enabled, the DMA overflow request is conditioned to the start of ramp A with an effective DMA transfer on previous ramp B (DMA acknowledge).

The update of all circular buffer values for ramp A can be done through a DMA channel triggered on a MC trigger. The update of all circular buffer values for ramp B, can be done through a second DMA channel triggered by the overflow DMA request.

Figure 36-37. DMA Triggers in RAMP and RAMP2 Operation Mode and Circular Buffer Enabled



DMA Operation with Circular Buffer in DSBOTH Mode

When a CC channel is selected as a circular buffer, the related DMA request is not set on a compare match detection, but on start of down-counting phase.

If at least one circular buffer is enabled, the DMA overflow request is conditioned to the start of up-counting phase with an effective DMA transfer on previous down-counting phase (DMA acknowledge).

When up-counting, all circular buffer values can be updated through a DMA channel triggered by MC trigger. When down-counting, all circular buffer values can be updated through a second DMA channel, triggered by the OVF DMA request.

Bit	31	30	29	28	27	26	25	24
					MCEOx	MCEOx	MCEOx	MCEOx
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	23	22	21	20	19	18	17	16
					MCEIx	MCEIx	MCEIx	MCEIx
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TCEIx	TCEIx	TCINVx	TCINVx		CNTEO	TRGEO	OVFEO
Access	R/W	R/W	R/W	R/W		R/W	R/W	R/W
Reset	0	0	0	0		0	0	0

Bit	7	6	5	4	3	2	1	0
	CNTSEL[1:0]		EVACT1[2:0]			EVACT0[2:0]		
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 27,26,25,24 – MCEOx: Match or Capture Channel x Event Output Enable
These bits control if the Match/capture event on channel x is enabled and will be generated for every match or capture.

Value	Description
0	Match/capture x event is disabled and will not be generated.
1	Match/capture x event is enabled and will be generated for every compare/capture on channel x.

Bits 19,18,17,16 – MCEIx: Match or Capture Channel x Event Input Enable
These bits indicate if the Match/capture x incoming event is enabled

These bits are used to enable match or capture input events to the CCx channel of TCC.

Value	Description
0	Incoming events are disabled.
1	Incoming events are enabled.

Bits 15,14 – TCEIx: Timer/Counter Event Input x Enable
This bit is used to enable input event x to the TCC.

Value	Description
0	Incoming event x is disabled.
1	Incoming event x is enabled.

Bits 13,12 – TCINVx: Timer/Counter Event x Invert Enable
This bit inverts the event x input.

Value	Description
0	Input event source x is not inverted.
1	Input event source x is inverted.

Number of Accumulated Samples	AVGCTRL. SAMPLENUM	Number of Automatic Right Shifts	Final Result Precision	Automatic Division Factor
4	0x2	0	14 bits	0
8	0x3	0	15 bits	0
16	0x4	0	16 bits	0
32	0x5	1	16 bits	2
64	0x6	2	16 bits	4
128	0x7	3	16 bits	8
256	0x8	4	16 bits	16
512	0x9	5	16 bits	32
1024	0xA	6	16 bits	64
Reserved	0xB –0xF		12 bits	0

38.6.2.10 Averaging

Averaging is a feature that increases the sample accuracy, at the cost of a reduced sampling rate. This feature is suitable when operating in noisy conditions.

Averaging is done by accumulating m samples, as described in Accumulation, and dividing the result by m. The averaged result is available in the RESULT register. The number of samples to be accumulated is specified by writing to AVGCTRL.SAMPLENUM as shown in Table 38-2.

The division is obtained by a combination of the automatic right shift described above, and an additional right shift that must be specified by writing to the Adjusting Result/Division Coefficient field in AVGCTRL (AVGCTRL.ADJRES), as described in Table 38-2.

Note: To perform the averaging of two or more samples, the Conversion Result Resolution field in the Control C register (CTRLC.RESSEL) must be set.

Averaging AVGCTRL.SAMPLENUM samples will reduce the un-averaged sampling rate by a factor $\frac{1}{\mathrm{AVGCTRL.SAMPLENUM}}$.

When the averaged result is available, the INTFLAG.RESRDY bit will be set.

Table 38-2. Averaging

Number of Accumulated Samples	AVGCTRL. SAMPLENUM	Intermediate Result Precision	Number of Automatic Right Shifts	Division Factor	AVGCTRL.ADJRES	Total Number of Right Shifts	Final Result Precision	Automatic Division Factor
1	0x0	12 bits	0	1	0x0		12 bits	0
2	0x1	13	0	2	0x1	1	12 bits	0
4	0x2	14	0	4	0x2	2	12 bits	0
8	0x3	15	0	8	0x3	3	12 bits	0
16	0x4	16	0	16	0x4	4	12 bits	0
32	0x5	17	1	16	0x4	5	12 bits	2

Bit	15	14	13	12	11	10	9	8
						SWTRIG	OFFSETCORR	GAINCORR
Access						R	R	R
Reset						0	0	0

Bit	7	6	5	4	3	2	1	0
	WINUT	WINLT	SAMPCTRL	AVGCTRL	CTRLC	INPUTCTRL	ENABLE	SWRST
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit 10 – SWTRIG: Software Trigger Synchronization Busy
This bit is cleared when the synchronization of SWTRIG register between the clock domains is complete.

This bit is set when the synchronization of SWTRIG register between clock domains is started.

Bit 9 – OFFSETCORR: Offset Correction Synchronization Busy
This bit is cleared when the synchronization of OFFSETCORR register between the clock domains is complete.

This bit is set when the synchronization of OFFSETCORR register between clock domains is started.

Bit 8 – GAINCORR: Gain Correction Synchronization Busy
This bit is cleared when the synchronization of GAINCORR register between the clock domains is complete.

This bit is set when the synchronization of GAINCORR register between clock domains is started.

Bit 7 – WINUT: Window Monitor Lower Threshold Synchronization Busy
This bit is cleared when the synchronization of WINUT register between the clock domains is complete.

This bit is set when the synchronization of WINUT register between clock domains is started.

Bit 6 – WINLT: Window Monitor Upper Threshold Synchronization Busy
This bit is cleared when the synchronization of WINLT register between the clock domains is complete.

This bit is set when the synchronization of WINLT register between clock domains is started.

Bit 5 – SAMPCTRL: Sampling Time Control Synchronization Busy
This bit is cleared when the synchronization of SAMPCTRL register between the clock domains is complete.

This bit is set when the synchronization of SAMPCTRL register between clock domains is started.

Bit 4 – AVGCTRL: Average Control Synchronization Busy
This bit is cleared when the synchronization of AVGCTRL register between the clock domains is complete.

This bit is set when the synchronization of AVGCTRL register between clock domains is started.

Bit 3 – CTRLC: Control C Synchronization Busy
This bit is cleared when the synchronization of CTRLC register between the clock domains is complete.

This bit is set when the synchronization of CTRLC register between clock domains is started.