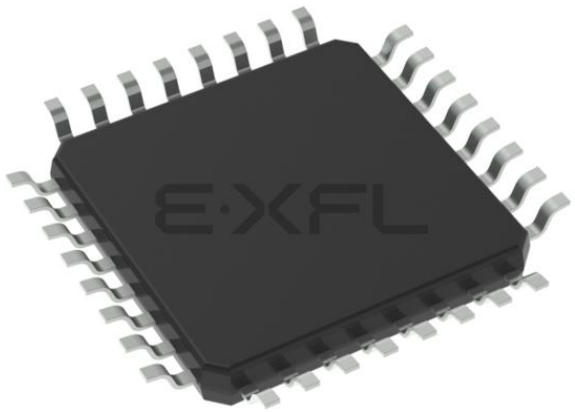

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, WDT
Number of I/O	26
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 10x12b, 1x16b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-TQFP
Supplier Device Package	32-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamc21e17a-aut

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6. I/O Multiplexing and Considerations

6.1 Multiplexed Signals

Each pin is by default controlled by the PORT as a general purpose I/O and alternatively it can be assigned to one of the peripheral functions A, B, C, D, E, F, G, H, or I. To enable a peripheral function on a pin, the Peripheral Multiplexer Enable bit in the Pin Configuration register corresponding to that pin (PINCFGn.PMUXEN, n = 0-31) in the PORT must be written to one. The selection of peripheral function A to H is done by writing to the Peripheral Multiplexing Odd and Even bits in the Peripheral Multiplexing register (PMUXn.PMUXE/O) in the PORT.

Table 6-1. PORT Function Multiplexing for SAM C21 N

Pin	I/O Pin	Supply	A		B			B[1][2]			C	D	E	F	G	H	I
			EIC	REF	ADC0	ADC1	SDADC	AC	PTC	DAC	SERCOM	SERCOM-ALT	TC	TCC	COM	AC/GCLK	CCL
1	PA00	VDDANA	EXTINT[0]									SERCOM1/PAD[0]	TC2/WO[0]			CMP[2]	
2	PA01	VDDANA	EXTINT[1]									SERCOM1/PAD[1]	TC2/WO[1]			CMP[3]	
3	PC00	VDDANA	EXTINT[8]		AIN[8]												
4	PC01	VDDANA	EXTINT[9]		AIN[9]												
5	PC02	VDDANA	EXTINT[10]		AIN[10]												
6	PC03	VDDIO	EXTINT[11]		AIN[11]						SERCOM7/PAD[0]			TCC2/WO[0]			
7	PA02	VDDANA	EXTINT[2]		AIN[0]			AIN[4]	Y[0]	VOUT							
8	PA03	VDDANA	EXTINT[3]	ADC/VREFA DAC/VREFB	AIN[1]				Y[1]								
9	PB04	VDDANA	EXTINT[4]			AIN[6]		AIN[5]	Y[10]								
10	PB05	VDDANA	EXTINT[5]			AIN[7]		AIN[6]	Y[11]								
13	PB06	VDDIO	EXTINT[6]			AIN[8]	INN[2]	AIN[7]	Y[12]		SERCOM7/PAD[1]						CCL2/IN[6]
14	PB07	VDDIO	EXTINT[7]			AIN[9]	INP[2]		Y[13]		SERCOM7/PAD[3]	SERCOM7/PAD[2]					CCL2/IN[7]
15	PB08	VDDIO	EXTINT[8]		AIN[2]	AIN[4]	INN[1]		Y[14]		SERCOM7/PAD[2]	SERCOM7/PAD[3]	TC4/WO[0]				CCL2/IN[8]
16	PB09	VDDANA	EXTINT[9]		AIN[3]	AIN[5]	INP[1]		Y[15]			SERCOM4/PAD[1]	TC4/WO[1]				CCL2/OUT[2]
17	PA04	VDDANA	EXTINT[4]	SDADC/VREFB	AIN[4]			AIN[0]	Y[2]			SERCOM0/PAD[0]	TC0/WO[0]				CCL0/IN[0]
18	PA05	VDDANA	EXTINT[5]		AIN[5]			AIN[1]	Y[3]			SERCOM0/PAD[1]	TC0/WO[1]				CCL0/IN[1]
19	PA06	VDDANA	EXTINT[6]		AIN[6]		INN[0]	AIN[2]	Y[4]			SERCOM0/PAD[2]	TC1/WO[0]				CCL0/IN[2]
20	PA07	VDDANA	EXTINT[7]		AIN[7]		INP[0]	AIN[3]	Y[5]			SERCOM0/PAD[3]	TC1/WO[1]				CCL0/OUT[0]
21	PC05	VDDANA	EXTINT[13]								SERCOM6/PAD[3]			TCC2/WO[1]			
22	PC06	VDDANA	EXTINT[14]								SERCOM6/PAD[0]						
23	PC07	VDDANA	EXTINT[15]								SERCOM6/PAD[1]						
26	PA08	VDDIO	NMI			AIN[10]			X[0]/Y[16]		SERCOM0/PAD[0]	SERCOM2/PAD[0]	TC0/WO[0]	TCC0/WO[0]			CCL1/IN[3]
27	PA09	VDDIO	EXTINT[9]			AIN[11]			X[1]/Y[17]		SERCOM0/PAD[1]	SERCOM2/PAD[1]	TC0/WO[1]	TCC0/WO[1]			CCL1/IN[4]
28	PA10	VDDIO	EXTINT[10]						X[2]/Y[18]		SERCOM0/PAD[2]	SERCOM2/PAD[2]	TC1/WO[0]	TCC0/WO[2]		GCLK_IO[4]	CCL1/IN[5]
29	PA11	VDDIO	EXTINT[11]						X[3]/Y[19]		SERCOM0/PAD[3]	SERCOM2/PAD[3]	TC1/WO[1]	TCC0/WO[3]		GCLK_IO[5]	CCL1/OUT[1]
30	PB10	VDDIO	EXTINT[10]									SERCOM4/PAD[2]	TC5/WO[0]	TCC0_WO4		GCLK_IO[4]	CCL1/IN[5]
31	PB11	VDDIO	EXTINT[11]									SERCOM4/PAD[3]	TC5/WO[1]	TCC0_WO5		GCLK_IO[5]	CCL1/OUT[1]
32	PB12	VDDIO	EXTINT[12]						X[12]/Y[28]		SERCOM4/PAD[0]		TC4/WO[0]	TCC0_WO6	CAN1/TX	GCLK_IO[6]	
33	PB13	VDDIO	EXTINT[13]						X[13]/Y[29]		SERCOM4/PAD[1]		TC4/WO[1]	TCC0_WO7	CAN1/RX	GCLK_IO[7]	
34	PB14	VDDIO	EXTINT[14]						X[14]/Y[30]		SERCOM4/PAD[2]		TC5/WO[0]		CAN1/TX	GCLK_IO[0]	CCL3/IN[9]
35	PB15	VDDIO	EXTINT[15]						X[15]/Y[31]		SERCOM4/PAD[3]		TC5/WO[1]		CAN1/RX	GCLK_IO[1]	CCL3/IN[10]
38	PC08	VDDIO	EXTINT[0]								SERCOM6/PAD[0]	SERCOM7/PAD[0]					
39	PC09	VDDIO	EXTINT[1]								SERCOM6/PAD[1]	SERCOM7/PAD[1]					
40	PC10	VDDIO	EXTINT[2]								SERCOM6/PAD[2]	SERCOM7/PAD[2]					
41	PC11	VDDIO	EXTINT[3]								SERCOM6/PAD[3]	SERCOM7/PAD[3]					
42	PC12	VDDIO	EXTINT[4]								SERCOM7/PAD[0]						
43	PC13	VDDIO	EXTINT[5]								SERCOM7/PAD[1]						
44	PC14	VDDIO	EXTINT[6]								SERCOM7/PAD[2]						
45	PC15	VDDIO	EXTINT[7]								SERCOM7/PAD[3]						
46	PA12	VDDIO	EXTINT[12]								SERCOM2/PAD[0]	SERCOM4/PAD[0]	TC2/WO[0]	TCC0_WO6		CMP[0]	
47	PA13	VDDIO	EXTINT[13]								SERCOM2/PAD[1]	SERCOM4/PAD[1]	TC2/WO[1]	TCC0_WO7		CMP[1]	
48	PA14	VDDIO	EXTINT[14]								SERCOM2/PAD[2]	SERCOM4/PAD[2]	TC3/WO[0]			GCLK_IO[0]	
49	PA15	VDDIO	EXTINT[15]								SERCOM2/PAD[3]	SERCOM4/PAD[3]	TC3/WO[1]			GCLK_IO[1]	
52	PA16	VDDIO	EXTINT[0]						X[4]/Y[20]		SERCOM1/PAD[0]	SERCOM3/PAD[0]	TC2/WO[0]	TCC1/WO[0]		GCLK_IO[2]	CCL0/IN[0]
53	PA17	VDDIO	EXTINT[1]						X[5]/Y[21]		SERCOM1/PAD[1]	SERCOM3/PAD[1]	TC2/WO[1]	TCC1/WO[1]		GCLK_IO[3]	CCL0/IN[1]
54	PA18	VDDIO	EXTINT[2]						X[6]/Y[22]		SERCOM1/PAD[2]	SERCOM3/PAD[2]	TC3/WO[0]	TCC1/WO[2]		CMP[0]	CCL0/IN[2]
55	PA19	VDDIO	EXTINT[3]						X[7]/Y[23]		SERCOM1/PAD[3]	SERCOM3/PAD[3]	TC3/WO[1]	TCC1/WO[3]		CMP[1]	CCL0/OUT[0]
56	PC16	VDDIO	EXTINT[8]								SERCOM6/PAD[0]						
57	PC17	VDDIO	EXTINT[9]								SERCOM6/PAD[1]						
58	PC18	VDDIO	EXTINT[10]								SERCOM6/PAD[2]						

Table 23-1. WDT Operating Modes

CTRLA.ENABLE	CTRLA.WEN	Interrupt Enable	Mode
0	x	x	Stopped
1	0	0	Normal mode
1	0	1	Normal mode with Early Warning interrupt
1	1	0	Window mode
1	1	1	Window mode with Early Warning interrupt

23.6.2 Basic Operation

23.6.2.1 Initialization

The following bits are enable-protected, meaning that they can only be written when the WDT is disabled (CTRLA.ENABLE=0):

- Control A register (CTRLA), except the Enable bit (CTRLA.ENABLE)
- Configuration register (CONFIG)
- Early Warning Interrupt Control register (EWCTRL)

Enable-protected bits in the CTRLA register can be written at the same time as CTRLA.ENABLE is written to '1', but not at the same time as CTRLA.ENABLE is written to '0'.

The WDT can be configured only while the WDT is disabled. The WDT is configured by defining the required Time-Out Period bits in the Configuration register (CONFIG.PER). If Window mode operation is desired, the Window Enable bit in the Control A register must be set (CTRLA.WEN=1) and the Window Period bits in the Configuration register (CONFIG.WINDOW) must be defined.

Enable-protection is denoted by the "Enable-Protected" property in the register description.

23.6.2.2 Configurable Reset Values

After a Power-on Reset, some registers will be loaded with initial values from the NVM User Row.

This includes the following bits and bit groups:

- Enable bit in the Control A register, CTRLA.ENABLE
- Always-On bit in the Control A register, CTRLA.ALWAYSON
- Watchdog Timer Windows Mode Enable bit in the Control A register, CTRLA.WEN
- Watchdog Timer Windows Mode Time-Out Period bits in the Configuration register, CONFIG.WINDOW
- Time-Out Period bits in the Configuration register, CONFIG.PER
- Early Warning Interrupt Time Offset bits in the Early Warning Interrupt Control register, EWCTRL.EWOFFSET

Related Links

NVM User Row Mapping

23.6.2.3 Enabling, Disabling, and Resetting

The WDT is enabled by writing a '1' to the Enable bit in the Control A register (CTRLA.ENABLE). The WDT is disabled by writing a '0' to CTRLA.ENABLE.

The WDT can be disabled only if the Always-On bit in the Control A register (CTRLA.ALWAYSON) is '0'.

PM – Power Manager

24.5.3 Clocks

The RTC bus clock (CLK_RTC_APB) can be enabled and disabled in the Main Clock module MCLK, and the default state of CLK_RTC_APB can be found in Peripheral Clock Masking section.

A 32KHz or 1KHz oscillator clock (CLK_RTC_OSC) is required to clock the RTC. This clock must be configured and enabled in the 32KHz oscillator controller (OSC32KCTRL) before using the RTC.

This oscillator clock is asynchronous to the bus clock (CLK_RTC_APB). Due to this asynchronicity, writing to certain registers will require synchronization between the clock domains. Refer to Synchronization for further details.

Related Links

OSC32KCTRL – 32KHz Oscillators Controller

Peripheral Clock Masking

24.5.4 DMA

Not applicable.

Related Links

DMAC – Direct Memory Access Controller

24.5.5 Interrupts

The interrupt request line is connected to the Interrupt Controller. Using the RTC interrupt requires the Interrupt Controller to be configured first.

Related Links

Nested Vector Interrupt Controller

24.5.6 Events

The events are connected to the *Event System*.

Related Links

EVSYS – Event System

24.5.7 Debug Operation

When the CPU is halted in debug mode the RTC will halt normal operation. The RTC can be forced to continue operation during debugging. Refer to DBGCTRL for details.

24.5.8 Register Access Protection

All registers with write-access are optionally write-protected by the peripheral access controller (PAC), except the following registers:

- Interrupt Flag Status and Clear (INTFLAG) register

Write-protection is denoted by the "PAC Write-Protection" property in the register description.

Write-protection does not apply to accesses through an external debugger. Refer to the PAC - Peripheral Access Controller for details.

Related Links

PAC - Peripheral Access Controller

Bit	15	14	13	12	11	10	9	8
	OVF						CMPn	CMPn
Access	R/W						R/W	R/W
Reset	0						0	0

Bit	7	6	5	4	3	2	1	0
	PERn	PERn	PERn	PERn	PERn	PERn	PERn	PERn
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – OVF: Overflow Interrupt Enable
Writing a '0' to this bit has no effect. Writing a '1' to this bit will set the Overflow Interrupt Enable bit, which enables the Overflow interrupt.

Value	Description
0	The Overflow interrupt is disabled.
1	The Overflow interrupt is enabled.

Bits 9:8 – CMPn: Compare n Interrupt Enable [n = 1..0]
Writing a '0' to this bit has no effect. Writing a '1' to this bit will set the Compare n Interrupt Enable bit, which and enables the Compare n interrupt.

Value	Description
0	The Compare n interrupt is disabled.
1	The Compare n interrupt is enabled.

Bits 7:0 – PERn: Periodic Interval n Interrupt Enable [n = 7..0]
Writing a '0' to this bit has no effect. Writing a '1' to this bit will set the Periodic Interval n Interrupt Enable bit, which enables the Periodic Interval n interrupt.

Value	Description
0	Periodic Interval n interrupt is disabled.
1	Periodic Interval n interrupt is enabled.

24.10.5 Interrupt Flag Status and Clear in COUNT16 mode (CTRLA.MODE=1)

Name: INTFLAG
Offset: 0x0C
Reset: 0x0000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
								TICKON
Access								RW
Reset								0

Bit	15	14	13	12	11	10	9	8
	STATESx	PRESCALERx[2:0]			STATESx	PRESCALERx[2:0]		
Access	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	STATESx	PRESCALERx[2:0]			STATESx	PRESCALERx[2:0]		
Access	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0

Bit 16 – TICKON: Pin Sampler frequency selection
This bit selects the clock used for the sampling of bounce during transition detection.

Value	Description
0	The bounce sampler is using GCLK_EIC.
1	The bounce sampler is using the low frequency clock.

Bits 3,7,11,15 – STATESx: Debouncer number of states x
This bit selects the number of samples by the debouncer low frequency clock needed to validate a transition from current pin state to next pin state in synchronous debouncing mode for pins EXTINT[7+(8x):8x].

Value	Description
0	The number of low frequency samples is 3.
1	The number of low frequency samples is 7.

Bits 2:0,6:4,10:8,14:12 – PRESCALERx: Debouncer Prescaler x
These bits select the debouncer low frequency clock for pins EXTINT[7+(8x):8x].

Value	Name	Description
0x0	F/2	EIC clock divided by 2
0x1	F/4	EIC clock divided by 4
0x2	F/8	EIC clock divided by 8
0x3	F/16	EIC clock divided by 16
0x4	F/32	EIC clock divided by 32
0x5	F/64	EIC clock divided by 64
0x6	F/128	EIC clock divided by 128
0x7	F/256	EIC clock divided by 256

26.8.13 Pin State

- Address register (ADDR)

Optional write-protection by the Peripheral Access Controller (PAC) is denoted by the "PAC Write-Protection" property in each individual register description.

PAC write-protection does not apply to accesses through an external debugger.

Related Links

PAC - Peripheral Access Controller

30.5.9 Analog Connections

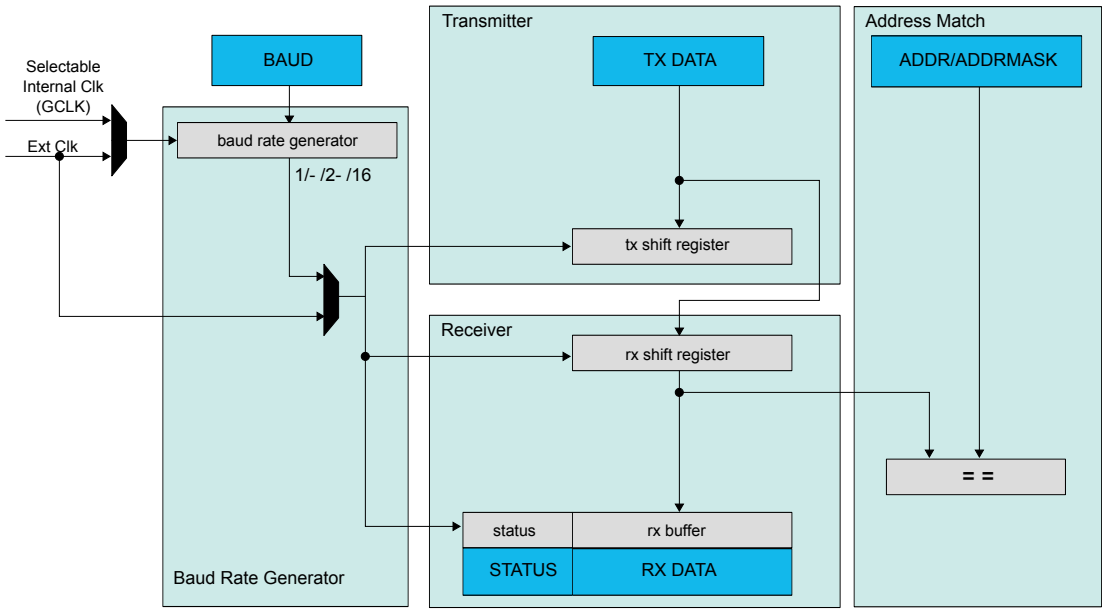
Not applicable.

30.6 Functional Description

30.6.1 Principle of Operation

The basic structure of the SERCOM serial engine is shown in Figure 30-2. Labels in capital letters are synchronous to the system clock and accessible by the CPU; labels in lowercase letters can be configured to run on the GCLK_SERCOMx_CORE clock or an external clock.

Figure 30-2. SERCOM Serial Engine



The transmitter consists of a single write buffer and a shift register.

The receiver consists of a two-level receive buffer and a shift register.

The baud-rate generator is capable of running on the GCLK_SERCOMx_CORE clock or an external clock.

Address matching logic is included for SPI and I^2C operation.

30.6.2 Basic Operation

30.6.2.1 Initialization

The SERCOM must be configured to the desired mode by writing the Operating Mode bits in the Control A register (CTRLA.MODE). Refer to table SERCOM Modes for details.

33.7 Register Summary - I2C Slave

Offset	Name	Bit Pos.								
0x00	CTRLA	7:0	RUNSTDBY			MODE[2:0]			ENABLE	SWRST
0x01		15:8								
0x02		23:16	SEXTTOEN		SDAHOLD[1:0]					PINOUT
0x03		31:24		LOWTOUT			SCLSM		SPEED[1:0]	
0x04	CTRLB	7:0								
0x05		15:8	AMODE[1:0]					AACKEN	GCMD	SMEN
0x06		23:16						ACKACT	CMD[1:0]	
0x07		31:24								
0x08 ... 0x13	Reserved									
0x14	INTENCLR	7:0	ERROR					DRDY	AMATCH	PREC
0x15	Reserved									
0x16	INTENSET	7:0	ERROR					DRDY	AMATCH	PREC
0x17	Reserved									
0x18	INTFLAG	7:0	ERROR					DRDY	AMATCH	PREC
0x19	Reserved									
0x1A	STATUS	7:0	CLKHOLD	LOWTOUT		SR	DIR	RXNACK	COLL	BUSERR
0x1B		15:8					LENERR	HS	SEXTTOUT	
0x1C	SYNCBUSY	7:0							ENABLE	SWRST
0x1D		15:8								
0x1E		23:16								
0x1F		31:24								
0x20 ... 0x23	Reserved									
0x24	ADDR	7:0	ADDR[6:0]							GENCEN
0x25		15:8	TENBITEN					ADDR[9:7]		
0x26		23:16	ADDRMASK[6:0]							
0x27		31:24						ADDRMASK[9:7]		
0x28	DATA	7:0	DATA[7:0]							
0x29		15:8								

33.8 Register Description - I2C Slave

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16- and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly.

Some registers are optionally write-protected by the Peripheral Access Controller (PAC). Optional PAC write-protection is denoted by the "PAC Write-Protection" property in each individual register description. For details, refer to Register Access Protection.

Some registers are synchronized when read and/or written. Synchronization is denoted by the "Write-Synchronized" or the "Read-Synchronized" property in each individual register description. For details, refer to Synchronization.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
			TFQF	TFQPI[4:0]				
Access			R	R	R	R	R	R
Reset			0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
				TFGI[4:0]				
Access				R	R	R	R	R
Reset				0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			TFFL[5:0]					
Access			R	R	R	R	R	R
Reset			0	0	0	0	0	0

Bit 21 – TFQF: Tx FIFO/Queue Full

Value	Description
0	Tx FIFO/Queue not full.
1	Tx FIFO/Queue full.

Bits 20:16 – TFQPI[4:0]: Tx FIFO/Queue Put Index
Tx FIFO/Queue write index pointer, range 0 to 31.

Bits 12:8 – TFGI[4:0]: Tx FIFO/Queue Get Index
Tx FIFO read index pointer, range 0 to 31. Read as zero when Tx Queue operation is configured (TXBC.TFQM = ‘1’).

Bits 5:0 – TFFL[5:0]: Tx FIFO Free Level
Number of consecutive free Tx FIFO elements starting from TFGI, range 0 to 32. Read as zero when Tx Queue operation is configured (TXBC.TFQM = ‘1’).

34.8.37 Tx Buffer Element Size Configuration

This register is write-restricted and only writable if bit fields CCCR.CCE = 1 and CCCR.INIT = 1.

Configures the number of data bytes belonging to a Tx Buffer element. Data field sizes >8 bytes are intended for CAN FD operation only.

Name: TXESC
Offset: 0xC8 [ID-0000a4bb]
Reset: 0x00000000
Property: Write-restricted

Bit	7	6	5	4	3	2	1	0
							WAVEGEN[1:0]	
Access							R/W	R/W
Reset							0	0

Bits 1:0 – WAVEGEN[1:0]: Waveform Generation Mode
These bits select the waveform generation operation. They affect the top value, as shown in Waveform Output Operations. They also control whether frequency or PWM waveform generation should be used. The waveform generation operations are explained in Waveform Output Operations.

These bits are not synchronized.

Value	Name	Operation	Top Value	Output Waveform on Match	Output Waveform on Wraparound
0x0	NFRQ	Normal frequency	PER[1] / Max	Toggle	No action
0x1	MFRQ	Match frequency	CC0	Toggle	No action
0x2	NPWM	Normal PWM	PER[1] / Max	Set	Clear
0x3	MPWM	Match PWM	CC0	Set	Clear

1) This depends on the TC mode: In 8-bit mode, the top value is the Period Value register (PER). In 16- and 32-bit mode it is the respective MAX value.

35.7.1.10 Driver Control

Name: DRVCTRL
Offset: 0x0D
Reset: 0x00
Property: PAC Write-Protection, Enable-Protected

Bit	7	6	5	4	3	2	1	0
								INVENx
Access								R/W
Reset								0

Bit 0 – INVENx: Output Waveform x Invert Enable
Bit x of INVEN[1:0] selects inversion of the output or capture trigger input of channel x.

Value	Description
0	Disable inversion of the WO[x] output and IO input pin.
1	Enable inversion of the WO[x] output and IO input pin.

35.7.1.11 Debug Control

This bit is set when the synchronization of ENABLE bit between clock domains is started.

Bit 0 – SWRST: SWRST Synchronization Busy
This bit is cleared when the synchronization of SWRST bit between the clock domains is complete.

This bit is set when the synchronization of SWRST bit between clock domains is started.

35.7.3.13 Counter Value, 32-bit Mode

Note: Prior to any read access, this register must be synchronized by user by writing the according TC Command value to the Control B Set register (CTRLBSET.CMD=READSYNC).

Name: COUNT
Offset: 0x14 [ID-00001cd8]
Reset: 0x00
Property: PAC Write-Protection, Write-Synchronized, Read-Synchronized

Bit	31	30	29	28	27	26	25	24
	COUNT[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	COUNT[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	COUNT[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	COUNT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – COUNT[31:0]: Counter Value
These bits contain the current counter value.

35.7.3.14 Period Value, 32-bit Mode

Name: PER
Offset: 0x1A [ID-00001cd8]
Reset: 0xFFFFFFFF
Property: Write-Synchronized

Pin Name	Type	Description
…	...	...
TCCx/WO[WO_NUM-1]	Digital output	Compare channel n waveform output

Refer to *I/O Multiplexing and Considerations* for details on the pin mapping for this peripheral. One signal can be mapped on several pins.

Related Links

I/O Multiplexing and Considerations

36.5 Product Dependencies

In order to use this peripheral, other parts of the system must be configured correctly, as described below.

36.5.1 I/O Lines

In order to use the I/O lines of this peripheral, the I/O pins must be configured using the I/O Pin Controller (PORT).

Related Links

PORT: IO Pin Controller

36.5.2 Power Management

This peripheral can continue to operate in any sleep mode where its source clock is running. The interrupts can wake up the device from sleep modes. Events connected to the event system can trigger other operations in the system without exiting sleep modes.

36.5.3 Clocks

The TCC bus clock (CLK_TCCx_APB, with x instance number of the TCCx) is enabled by default, and can be enabled and disabled in the Main Clock.

A generic clock (GCLK_TCCx) is required to clock the TCC. This clock must be configured and enabled in the generic clock controller before using the TCC. Note that TCC0 and TCC1 share a peripheral clock generator.

The generic clocks (GCLK_TCCx) are asynchronous to the bus clock (CLK_TCCx_APB). Due to this asynchronicity, writing certain registers will require synchronization between the clock domains. Refer to Synchronization for further details.

Related Links

Peripheral Clock Masking

GCLK - Generic Clock Controller

36.5.4 DMA

The DMA request lines are connected to the DMA Controller (DMAC). In order to use DMA requests with this peripheral the DMAC must be configured first. Refer to *DMAC – Direct Memory Access Controller* for details.

Related Links

DMAC – Direct Memory Access Controller

Bit 20 – INVEI: Inverted Event Input Enable

Value	Description
0	Incoming event is not inverted.
1	Incoming event is inverted.

Bit 7 – EDGESEL: Edge Selection

Value	Description
0	Edge detector is disabled.
1	Edge detector is enabled.

Bits 5:4 – FILTSEL[1:0]: Filter Selection
These bits select the LUT output filter options:

Filter Selection

Value	Name	Description
0x0	DISABLE	Filter disabled
0x1	SYNCH	Synchronizer enabled
0x2	FILTER	Filter enabled
0x3	-	Reserved

Bit 1 – ENABLE: LUT Enable

Value	Description
0	The LUT is disabled.
1	The LUT is enabled.

Bits 19:16,15:12,11:8 – INSELx: LUT Input x Source Selection
These bits select the LUT input x source:

Value	Name	Description
0x0	MASK	Masked input
0x1	FEEDBACK	Feedback input source
0x2	LINK	Linked LUT input source
0x3	EVENT	Event input source
0x4	IO	I/O pin input source
0x5	AC	AC input source
0x6	TC	TC input source
0x7	ALTTC	Alternative TC input source
0x8	TCC	TCC input source
0x9	SERCOM	SERCOM input source
0xA	ALT2TC	Alternative 2 TC input source

When executing an operation that requires synchronization, the corresponding synchronization bit is set in Synchronization Busy register (SYNCBUSY) and cleared when synchronization is complete.

If an operation that require synchronization is executed while its busy bit is on, the operation is discarded and a bus error is generated.

The following bits need synchronization when written:

- Software Reset bit in Control A register (CTRLA.SWRST)
- Enable bit in Control A register (CTRLA.ENABLE)

Write-synchronization is denoted by the Write-Synchronized property in the register description.

The following registers need synchronization when written:

- Input Control register (INPUTCTRL)
- Reference Control register (REFCTRL)
- Control C register (CTRLC)
- Window Monitor Lower Threshold register (WINLT)
- Window Monitor Upper Threshold register (WINUT)
- Offset correction register (OFFSETCORR)
- Gain correction register (GAINCORR)
- Shift correction register (SHIFTCORR)
- Software Trigger register (SWTRIG)
- Analog Control Register (ANACTRL)

Write-synchronization is denoted by the Write-Synchronized property in the register description.

41.8.10 Synchronization Busy

Name: SYNCBUSY
Offset: 0x10 [ID-00000bc7]
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
					DATABUF	DATA	ENABLE	SWRST
Access					R	R	R	R
Reset					0	0	0	0

Bit 3 – DATABUF: Data Buffer DAC0
This bit is set when DATABUF register is written.

This bit is cleared when DATABUF synchronization is completed.

Value	Description
0	No ongoing synchronized access.
1	Synchronized access is ongoing.

Bit 2 – DATA: Data
This bit is set when DATA register is written.

This bit is cleared when DATA synchronization is completed.

Value	Description
0	No ongoing synchronized access.
1	Synchronized access is ongoing.

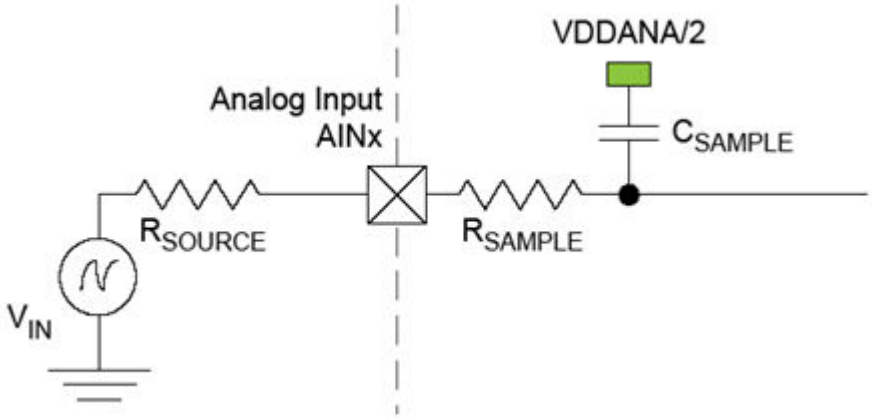
Bit 1 – ENABLE: DAC Enable Status
This bit is set when CTRLA.ENABLE bit is written.

This bit is cleared when CTRLA.ENABLE synchronization is completed.

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
Vcmin	Input common mode voltage	CTRLC.R2R=1	0.2	-	VREF-0.2	V
		CTRLC.R2R=0	VREF/2-0.2	-	VREF/2+0.2	V
CSAMPLE	Input sampling capacitance		-	1.6	4.5	pF
RSAMPLE	Input sampling on-resistance	For a sampling rate at 1 Msps	-	1000	1715	Ω
Rref	Reference input source resistance		0	-	1000	kΩ

1. These values are based on simulation. These values are not covered by test limits in production or characterization.

Figure 45-4. ADC Analog Input AINx



The minimum sampling time $t_{samplehold}$ for a given R_{source} can be found using this formula:

$$t_{samplehold} \geq \left(R_{sample} + R_{source}\right) \times C_{sample} \times \left(n + 2\right) \times \ln\left(2\right)$$

For 12-bit accuracy:

$$t_{samplehold} \geq \left(R_{sample} + R_{source}\right) \times C_{sample} \times 9.7$$

where $t_{samplehold} \geq \frac{1}{2 \times f_{ADC}}$.

Table 45-19. Differential Mode(1)

Symbol	Parameter	Conditions		Measurement			Unit
				Min	Typ	Max	
ENOB(2)	Effective Number of bits	Fadc = 500 ksps	Vddana=5.0V Vref=Vddana	10.0	10.7	11	bits
			Vddana=2.7V Vref=2.0V	10.3	10.5	10.9	
		Fadc = 1 Msps	Vddana=5.0V Vref=Vddana	10.5	10.8	11.1	
			Vddana=2.7V Vref=2.0V	9.9	10.0	10.6	
TUE	Total Unadjusted Error	Fadc = 500 ksps	Vddana=5.0V Vref=Vddana	-	7.8	17.0	LSB

Symbol	Parameter	Conditions		Measurement			Unit
				Min	Typ	Max	
			Vddana=2.7V Vref=2.0V	-	8.0	32.0	
		Fadc = 1 Msps	Vddana=5.0V Vref=Vddana	-	9.0	20.0	
			Vddana=2.7V Vref=2.0V	-	10.5	32.0	
INL	Integral Non Linearity	Fadc = 500 ksps	Vddana=5.0V Vref=Vddana	-	+/-1.6	+/-3	LSB
			Vddana=2.7V Vref=2.0V	-	+/-1.9	+/-3	
		Fadc = 1 Msps	Vddana=5.0V Vref=Vddana	-	+/-1.5	+/-3	
			Vddana=2.7V Vref=2.0V	-	+/-3.2	+/-5	
DNL	Differential Non Linearity	Fadc = 500 ksps	Vddana=5.0V Vref=Vddana	-	-0.8/+1	-1/+2	LSB
			Vddana=2.7V Vref=2.0V	-	-0.7/+1.3	-1/+2.1	
		Fadc = 1 Msps	Vddana=5.0V Vref=Vddana	-	-0.8/+1.1	-1/+3.3	
			Vddana=2.7V Vref=2.0V	-	-0.9/+1.3	-1/+3.2	
Gain	Gain Error (1)	Fadc = 1 Msps	Vddana=2.7V Vref=2.0V	-	+/-18	+/-57	mV
			Vddana=5.0V Vref=4.096V	-	+/-41	+/-100	
			Vddana=3.0V Vref=Vddana	-	+/-17	+/-66	
			Vddana=5.0V Vref=Vddana		+/-39	+/-81	
TCg	Gain Drift	Fadc = 1 Msps	Vddana=5.0V Vref=Vddana	-250	-210	-170	µV/°C
Offset	Offset Error (1)	Fadc = 1 Msps	Vddana=2.7V Vref=2.0V	-	+/-1.4	+/-11	mV
			Vddana=5.0V Vref=4.096V	-	+/-6	+/-18	
			Vddana=3.0V Vref=Vddana	-	+/-2	+/-9	

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
		XOSC.GAIN=2				
		F = 16MHz CL=20pF XOSC.GAIN=3	-	10.8	18.1	
		F = 32MHz CL=18pF XOSC.GAIN=4	-	8.7	15.4	

1. These are based on characterization.

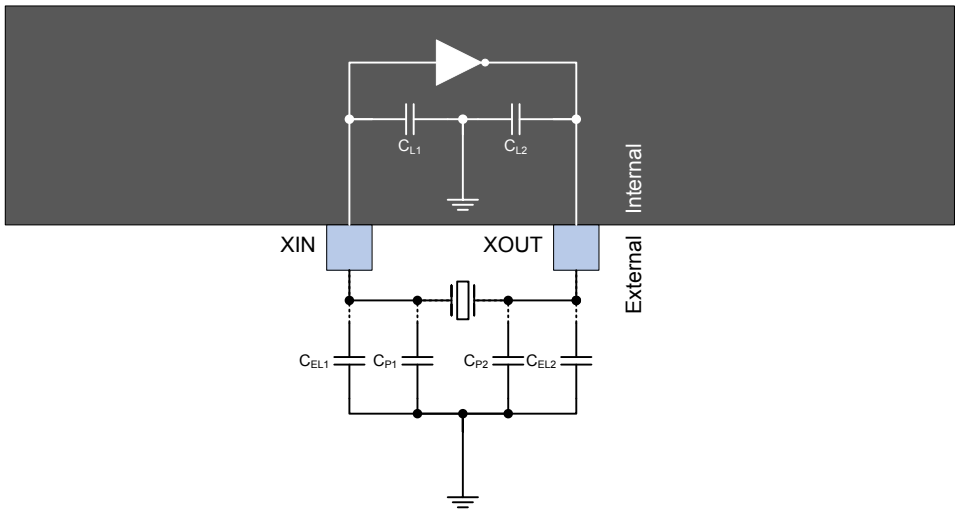
Table 45-41. Power Consumption (1)

Symbol	Parameters	Conditions	Ta	Typ.	Max	Units
IDD	Current consumption	F = 2MHz CL=20pF XOSC.GAIN=0 VDD = 5.0V AGC=OFF	Max 85°C Typ 25°C	150	202	µA
		AGC=ON		138	192	
		F = 4MHz CL=20pF XOSC.GAIN=1 VDD = 5.0V AGC=OFF		220	288	
		AGC=ON		175	260	
		F = 8MHz CL=20pF XOSC.GAIN=2 VDD = 5.0V AGC=OFF		350	416	
		AGC=ON		247	321	
		F = 16MHz CL=20pF XOSC.GAIN=3 VDD = 5.0V		663	843	

49.7.4 Calculating the Correct Crystal Decoupling Capacitor

The model shown in Figure 49-10 can be used to calculate correct load capacitor for a given crystal. This model includes internal capacitors C_{Ln}, external parasitic capacitance C_{ELn} and external load capacitance C_{Pn}.

Figure 49-10. Crystal Circuit With Internal, External and Parasitic Capacitance



Using this model the total capacitive load for the crystal can be calculated as shown in the equation below:

$$\sum C_{\text{tot}} = \frac{(C_{L1} + C_{P1} + C_{\text{EL1}})(C_{L2} + C_{P2} + C_{\text{EL2}})}{C_{L1} + C_{P1} + C_{\text{EL1}} + C_{L2} + C_{P2} + C_{\text{EL2}}}$$

where C_{tot} is the total load capacitance seen by the crystal. This value should be equal to the load capacitance value found in the crystal manufacturer datasheet.

The parasitic capacitance C_{ELn} can in most applications be disregarded as these are usually very small. If accounted for, these values are dependent on the PCB material and PCB layout.

For some crystal the internal capacitive load provided by the device itself can be enough. To calculate the total load capacitance in this case. C_{ELn} and C_{Pn} are both zero, $C_{L1} = C_{L2} = C_L$, and the equation reduces to the following:

$$\sum C_{\text{tot}} = \frac{C_L}{2}$$

See the related links for equivalent internal pin capacitance values.

Related Links

Crystal Oscillator Characteristics

49.8 Programming and Debug Ports

For programming and/or debugging the SAM C20/C21 the device should be connected using the Serial Wire Debug (SWD) interface. Currently the SWD interface is supported by several Microchip and third party programmers and debuggers, like the SAM-ICE, JTAGICE3 or SAM C21 Xplained Pro (SAM C21 evaluation kit) Embedded Debugger.