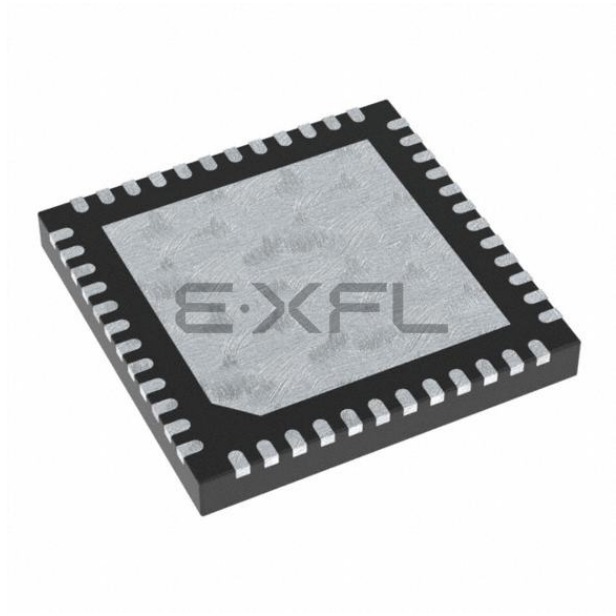

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, WDT
Number of I/O	38
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 14x12b, 2x16b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamc21g16a-mnt

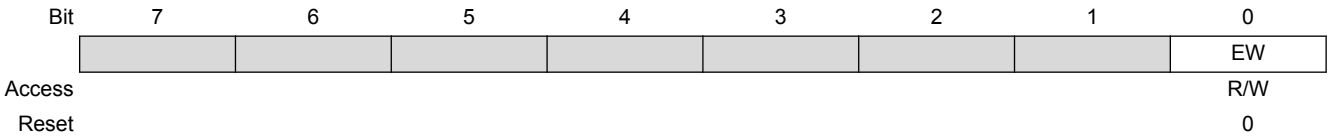
Offset	Name	Bit Pos.								
0xA9		15:8								
0xAA		23:16								
0xAB		31:24								
0xAC	PCHCTRL11	7:0	WRTLOCK	CHEN			GEN[3:0]			
0xAD		15:8								
0xAE		23:16								
0xAF		31:24								
0xB0	PCHCTRL12	7:0	WRTLOCK	CHEN			GEN[3:0]			
0xB1		15:8								
0xB2		23:16								
0xB3		31:24								
0xB4	PCHCTRL13	7:0	WRTLOCK	CHEN			GEN[3:0]			
0xB5		15:8								
0xB6		23:16								
0xB7		31:24								
0xB8	PCHCTRL14	7:0	WRTLOCK	CHEN			GEN[3:0]			
0xB9		15:8								
0xBA		23:16								
0xBB		31:24								
0xBC	PCHCTRL15	7:0	WRTLOCK	CHEN			GEN[3:0]			
0xBD		15:8								
0xBE		23:16								
0xBF		31:24								
0xC0	PCHCTRL16	7:0	WRTLOCK	CHEN			GEN[3:0]			
0xC1		15:8								
0xC2		23:16								
0xC3		31:24								
0xC4	PCHCTRL17	7:0	WRTLOCK	CHEN			GEN[3:0]			
0xC5		15:8								
0xC6		23:16								
0xC7		31:24								
0xC8	PCHCTRL18	7:0	WRTLOCK	CHEN			GEN[3:0]			
0xC9		15:8								
0xCA		23:16								
0xCB		31:24								
0xCC	PCHCTRL19	7:0	WRTLOCK	CHEN			GEN[3:0]			
0xCD		15:8								
0xCE		23:16								
0xCF		31:24								
0xD0	PCHCTRL20	7:0	WRTLOCK	CHEN			GEN[3:0]			
0xD1		15:8								
0xD2		23:16								
0xD3		31:24								
0xD4	PCHCTRL21	7:0	WRTLOCK	CHEN			GEN[3:0]			
0xD5		15:8								
0xD6		23:16								
0xD7		31:24								

Value	Description
0	The Early Warning interrupt is disabled.
1	The Early Warning interrupt is enabled.

23.8.5 Interrupt Enable Set

This register allows the user to enable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Clear (INTENCLR) register.

Name: INTENSET
Offset: 0x05 [ID-0000067a]
Reset: 0x00
Property: PAC Write-Protection

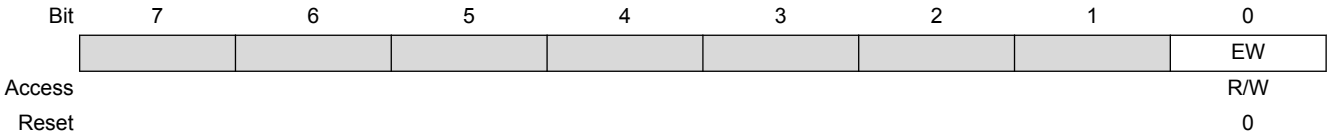


Bit 0 – EW: Early Warning Interrupt Enable
Writing a '0' to this bit has no effect.
Writing a '1' to this bit sets the Early Warning Interrupt Enable bit, which enables the Early Warning interrupt.

Value	Description
0	The Early Warning interrupt is disabled.
1	The Early Warning interrupt is enabled.

23.8.6 Interrupt Flag Status and Clear

Name: INTFLAG
Offset: 0x06 [ID-0000067a]
Reset: 0x00
Property: N/A



Bit 0 – EW: Early Warning
This flag is cleared by writing a '1' to it.

This flag is set when an Early Warning interrupt occurs, as defined by the EWOFFSET bit group in EWCTRL.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the Early Warning interrupt flag.

23.8.7 Synchronization Busy

27.7 Register Summary

Offset	Name	Bit Pos.									
0x00	CTRLA	7:0		CMD[6:0]							
0x01		15:8	CMDEX[7:0]								
0x02 ... 0x03	Reserved										
0x04	CTRLB	7:0	MANW			RWS[3:0]					
0x05		15:8							SLEEPPRM[1:0]		
0x06		23:16						CACHEDIS	READMODE[1:0]		
0x07		31:24									
0x08	PARAM	7:0	NVMP[7:0]								
0x09		15:8	NVMP[15:8]								
0x0A		23:16	RWWEEP[3:0]					PSZ[2:0]			
0x0B		31:24	RWWEEP[11:4]								
0x0C	INTENCLR	7:0							ERROR	READY	
0x0D ... 0x0F	Reserved										
0x10	INTENSET	7:0							ERROR	READY	
0x11 ... 0x13	Reserved										
0x14	INTFLAG	7:0							ERROR	READY	
0x15 ... 0x17	Reserved										
0x18	STATUS	7:0				NVME	LOCKE	PROGE	LOAD	PRM	
0x19		15:8								SB	
0x1A ... 0x1B	Reserved										
0x1C	ADDR	7:0	ADDR[7:0]								
0x1D		15:8	ADDR[15:8]								
0x1E		23:16				ADDR[20:16]					
0x1F		31:24									
0x20	LOCK	7:0	LOCK[7:0]								
0x21		15:8	LOCK[15:8]								
0x22 ... 0x27	Reserved										
0x28	PBLDATA0	7:0	PBLDATA[7:0]								
0x29		15:8	PBLDATA[15:8]								
0x2A		23:16	PBLDATA[23:16]								
0x2B		31:24	PBLDATA[31:24]								
0x2C	PBLDATA1	7:0	PBLDATA[7:0]								
0x2D		15:8	PBLDATA[15:8]								

Table 30-3. BAUD Register Value vs. Baud Frequency

BAUD Register Value	Serial Engine CPF	f_{BAUD} at 48MHz Serial Engine Frequency (f_{REF})
0 – 406	160	3MHz
407 – 808	161	2.981MHz
809 – 1205	162	2.963MHz
...	...	...
65206	31775	15.11kHz
65207	31871	15.06kHz
65208	31969	15.01kHz

30.6.3 Additional Features

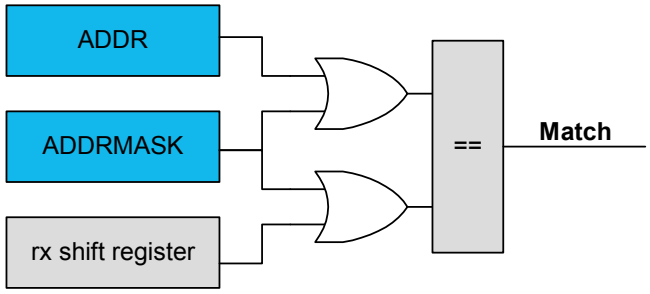
30.6.3.1 Address Match and Mask

The SERCOM address match and mask feature is capable of matching either one address, two unique addresses, or a range of addresses with a mask, based on the mode selected. The match uses seven or eight bits, depending on the mode.

Address With Mask

An address written to the Address bits in the Address register (ADDR.ADDR), and a mask written to the Address Mask bits in the Address register (ADDR.ADDRMASK) will yield an address match. All bits that are masked are not included in the match. Note that writing the ADDR.ADDRMASK to 'all zeros' will match a single unique address, while writing ADDR.ADDRMASK to 'all ones' will result in all addresses being accepted.

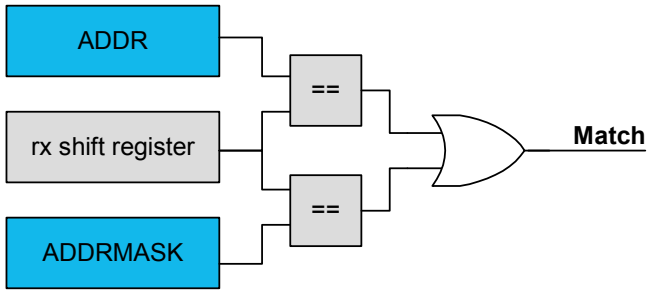
Figure 30-4. Address With Mask



Two Unique Addresses

The two addresses written to ADDR and ADDRMASK will cause a match.

Figure 30-5. Two Unique Addresses



Startup Timing The minimum time between SDA transition and SCL rising edge is 6 APB cycles when the DATA register is written in smart mode. If a greater startup time is required due to long rise times, the time between DATA write and IF clear must be controlled by software.

Note: When timing is controlled by user, the Smart Mode cannot be enabled.

Related Links

Electrical Characteristics 85°C (SAM C20/C21 E/G/J)

Master Clock Generation (High-Speed Mode)

For I²C *Hs* transfers, there is no SCL synchronization. Instead, the SCL frequency is determined by the GCLK_SERCOMx_CORE frequency (f_{GCLK}) and the High-Speed Baud setting in the Baud register (BAUD.HSBAUD). When BAUD.HSBAUDLOW=0, the HSBAUD value will determine both SCL high and SCL low. In this case the following formula determines the SCL frequency.

$$f_{SCL} = \frac{f_{GCLK}}{2 + 2 \cdot HS\,BAUD}$$

When HSBAUDLOW is non-zero, the following formula determines the SCL frequency.

$$f_{SCL} = \frac{f_{GCLK}}{2 + HS\,BAUD + HSBAUDLOW}$$

Note: The I²C standard *Hs* (High-speed) requires a nominal high to low SCL ratio of 1:2, and HSBAUD should be set accordingly. At a minimum, BAUD.HSBAUD and/or BAUD.HSBAUDLOW must be non-zero.

Transmitting Address Packets

The I²C master starts a bus transaction by writing the I²C slave address to ADDR.ADDR and the direction bit, as described in Principle of Operation. If the bus is busy, the I²C master will wait until the bus becomes idle before continuing the operation. When the bus is idle, the I²C master will issue a start condition on the bus. The I²C master will then transmit an address packet using the address written to ADDR.ADDR. After the address packet has been transmitted by the I²C master, one of four cases will arise according to arbitration and transfer direction.

Case 1: Arbitration lost or bus error during address packet transmission

If arbitration was lost during transmission of the address packet, the Master on Bus bit in the Interrupt Flag Status and Clear register (INTFLAG.MB) and the Arbitration Lost bit in the Status register (STATUS.ARBLOST) are both set. Serial data output to SDA is disabled, and the SCL is released, which disables clock stretching. In effect the I²C master is no longer allowed to execute any operation on the bus until the bus is idle again. A bus error will behave similarly to the arbitration lost condition. In this case, the MB interrupt flag and Master Bus Error bit in the Status register (STATUS.BUSERR) are both set in addition to STATUS.ARBLOST.

The Master Received Not Acknowledge bit in the Status register (STATUS.RXNACK) will always contain the last successfully received acknowledge or not acknowledge indication.

In this case, software will typically inform the application code of the condition and then clear the interrupt flag before exiting the interrupt routine. No other flags have to be cleared at this moment, because all flags will be cleared automatically the next time the ADDR.ADDR register is written.

Case 2: Address packet transmit complete – No ACK received

If there is no I²C slave device responding to the address packet, then the INTFLAG.MB interrupt flag and STATUS.RXNACK will be set. The clock hold is active at this point, preventing further activity on the bus.

Bit	31	30	29	28	27	26	25	24
	REL[3:0]				STEP[3:0]			
Access	R	R	R	R	R	R	R	R
Reset	0	0	1	1	0	0	1	0

Bit	23	22	21	20	19	18	17	16
	SUBSTEP[3:0]							
Access	R	R	R	R				
Reset	0	0	0	1				

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bits 31:28 – REL[3:0]: Core Release
One digit, BCD-coded.

Bits 27:24 – STEP[3:0]: Step of Core Release
One digit, BCD-coded.

Bits 23:20 – SUBSTEP[3:0]: Sub-step of Core Release
One digit, BCD-coded.

34.8.2 Endian

Name: ENDN
Offset: 0x04 [ID-0000a4bb]
Reset: 0x87654321
Property: Read-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	FLST	FIDX[6:0]						
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	MSI[1:0]		BIDX[5:0]					
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit 15 – FLST: Filter List
Indicates the filter list of the matching filter element.

Value	Description
0	Standard Filter List.
1	Extended Filter List.

Bits 14:8 – FIDX[6:0]: Filter Index
Index of matching filter element. Range is 0 to SIDFC.LSS - 1 (standard) or XIDFC.LSE - 1 (extended).

Bits 7:6 – MSI[1:0]: Message Storage Indicator
This field defines the message storage information to a FIFO.

Value	Name	Description
0x0	NONE	No FIFO selected.
0x1	LOST	FIFO message lost.
0x2	FIFO0	Message stored in FIFO 0.
0x3	FIFO1	Message stored in FIFO 1.

Bits 5:0 – BIDX[5:0]: Buffer Index
Index of Rx FIFO element to which the message was stored. Only valid when MSI[1] = 1.

34.8.25 New Data 1

Name: NDAT1
Offset: 0x98 [ID-0000a4bb]
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
	NDn	NDn	NDn	NDn	NDn	NDn	NDn	NDn
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	NDn	NDn	NDn	NDn	NDn	NDn	NDn	NDn
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NDn	NDn	NDn	NDn	NDn	NDn	NDn	NDn
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NDn	NDn	NDn	NDn	NDn	NDn	NDn	NDn
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – NDn: New Data [n = 32..64]
The register holds the New Data flags of Rx Buffers 32 to 63. The flags are set when the respective Rx Buffer has been updated from a received frame. The flags remain set until the Host clears them. A flag is cleared by writing 1 to the corresponding bit position. Writing a 0 has no effect. A hard reset will clear the register.

34.8.27 Rx FIFO 0 Configuration

Name: RXF0C
Offset: 0xA0 [ID-0000a4bb]
Reset: 0x00000000
Property: Write-restricted

Value	Description
0	Tx FIFO operation.
1	Tx Queue operation.

Bits 29:24 – TFQS[5:0]: Transmit FIFO/Queue Size

Value	Description
0	No Tx FIFO/Queue.
1 - 32	Number of Tx Buffers used for Tx FIFO/Queue.
>32	Values greater than 32 are interpreted as 32.

Bits 21:16 – NDTB[5:0]: Number of Dedicated Transmit Buffers

Value	Description
0	No Tx FIFO/Queue.
1 - 32	Number of Tx Buffers used for Tx FIFO/Queue.
>32	Values greater than 32 are interpreted as 32.

Bits 15:0 – TBSA[15:0]: Tx Buffers Start Address
Start address of Tx Buffers section in Message RAM. When the CAN module addresses the Message RAM it addresses 32-bit words, not single bytes. The configurable start addresses are 32-bit word addresses, i.e. only bits 15 to 2 are evaluated, the two least significant bits are ignored. Bits 1 to 0 will always be read back as “00”.

34.8.36 Tx FIFO/Queue Status

Note: In case of mixed configurations where dedicated Tx Buffers are combined with a Tx FIFO or a Tx Queue, the Put and Get Indexes indicate the number of the Tx Buffer starting with the first dedicated Tx Buffers. Example: For a configuration of 12 dedicated Tx Buffers and a Tx FIFO of 20 Buffers a Put Index of 15 points to the fourth buffer of the Tx FIFO.

Name: TXFQS
Offset: 0xC4 [ID-0000a4bb]
Reset: 0x00000000
Property: Read-only

Offset	Name	Bit Pos.								
0x2F		31:24	PERBUF[31:24]							
0x30	CCBUF0	7:0	CCBUF[7:0]							
0x31		15:8	CCBUF[15:8]							
0x32		23:16	CCBUF[23:16]							
0x33		31:24	CCBUF[31:24]							
0x34	CCBUF1	7:0	CCBUF[7:0]							
0x35		15:8	CCBUF[15:8]							
0x36		23:16	CCBUF[23:16]							
0x37		31:24	CCBUF[31:24]							

35.7.3.1 Control A

Name: CTRLA
Offset: 0x00
Reset: 0x00000000
Property: PAC Write-Protection, Write-Synchronized, Enable-Protected

Bit	31	30	29	28	27	26	25	24
				CAPTMODE1[1:0]			CAPTMODE0[1:0]	
Access				R/W	R/W		R/W	R/W
Reset				0	0		0	0

Bit	23	22	21	20	19	18	17	16
			COPEN1	COPEN0			CAPTEN1	CAPTEN0
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

Bit	15	14	13	12	11	10	9	8
					ALOCK	PRESCALER[2:0]		
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ONDEMAND	RUNSTDBY	PRESCSYNC[1:0]		MODE[1:0]		ENABLE	SWRST
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	W
Reset	0	0	0	0	0	0	0	0

Bits 28:27 – CAPTMODE1[1:0]: Capture mode Channel 1
These bits select the channel 1 capture mode.

Value	Name	Description
0x0	DEFAULT	Default capture
0x1	CAPTMIN	Minimum capture
0x2	CAPTMAX	Maximum capture
0x3		Reserved

Bits 25:24 – CAPTMODE0[1:0]: Capture mode Channel 0
These bits select the channel 0 capture mode.

Bit	31	30	29	28	27	26	25	24
	CC[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	CC[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CC[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

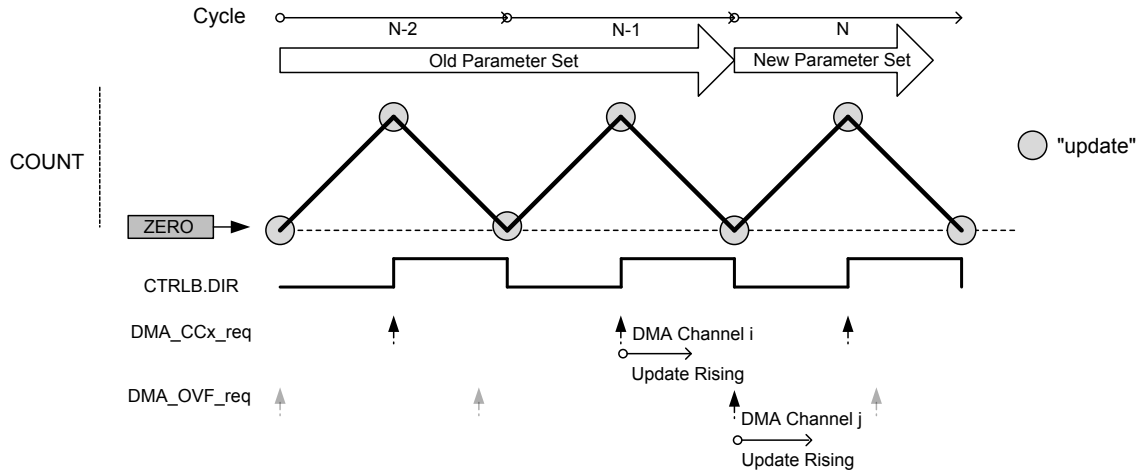
Bit	7	6	5	4	3	2	1	0
	CC[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – CC[31:0]: Channel x Compare/Capture Value
These bits contain the compare/capture value in 32-bit TC mode. In Match frequency (MFRQ) or Match PWM (MPWM) waveform operation (WAVE.WAVEGEN), the CC0 register is used as a period register.

35.7.3.16 Period Buffer Value, 32-bit Mode

Name: PERBUF
Offset: 0x2C [ID-00001cd8]
Reset: 0xFFFFFFFF
Property: Write-Synchronized

Figure 36-38. DMA Triggers in DSBOTH Operation Mode and Circular Buffer Enabled



36.6.5.2 Interrupts

The TCC has the following interrupt sources:

- Overflow/Underflow (OVF)
- Retrigger (TRG)
- Count (CNT) - refer also to description of EVCTRL.CNTSEL.
- Capture Overflow Error (ERR)
- Non-Recoverable Update Fault (UFS)
- Debug Fault State (DFS)
- Recoverable Faults (FAULTn)
- Non-recoverable Faults (FAULTx)
- Compare Match or Capture Channels (MCx)

These interrupts are asynchronous wake-up sources. See Sleep Mode Entry and Exit Table in PM/Sleep Mode Controller section for details.

Each interrupt source has an interrupt flag associated with it. The interrupt flag in the Interrupt Flag Status and Clear (INTFLAG) register is set when the interrupt condition occurs. Each interrupt can be individually enabled by writing a '1' to the corresponding bit in the Interrupt Enable Set (INTENSET) register, and disabled by writing a '1' to the corresponding bit in the Interrupt Enable Clear (INTENCLR) register. An interrupt request is generated when the interrupt flag is set and the corresponding interrupt is enabled. The interrupt request remains active until the interrupt flag is cleared, the interrupt is disabled, or the TCC is reset. See INTFLAG for details on how to clear interrupt flags. The TCC has one common interrupt request line for all the interrupt sources. The user must read the INTFLAG register to determine which interrupt condition is present.

Note: Interrupts must be globally enabled for interrupt requests to be generated. Refer to *Nested Vector Interrupt Controller* for details.

Related Links

Nested Vector Interrupt Controller

Sleep Mode Controller

36.6.5.3 Events

The TCC can generate the following output events:

Bit 0 – STOP: Stop
This bit is set when the TCC is disabled either on a STOP command or on an UPDATE condition when One-Shot operation mode is enabled (CTRLBSET.ONESHOT=1).

This bit is clear on the next incoming counter increment or decrement.

Value	Description
0	Counter is running.
1	Counter is stopped.

36.8.14 Counter Value

Note: Prior to any read access, this register must be synchronized by user by writing the according TCC Command value to the Control B Set register (CTRLBSET.CMD=READSYNC).

Name: COUNT
Offset: 0x34 [ID-00002e48]
Reset: 0x00000000
Property: PAC Write-Protection, Write-Synchronized, Read-Synchronized

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	COUNT[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	COUNT[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	COUNT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 23:0 – COUNT[23:0]: Counter Value
These bits hold the value of the counter register.

Note: When the TCC is configured as 16-bit timer/counter, the excess bits are read zero.

Note: This bit field occupies the MSB of the register, [23:m]. m is dependent on the Resolution bit in the Control A register (CTRLA.RESOLUTION):

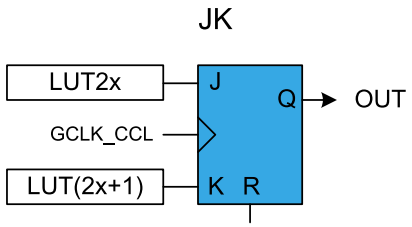
CTRLA.RESOLUTION	Bits [23:m]
0x0 - NONE	23:0 (depicted)
0x1 - DITH4	23:4

CTRLA.RESOLUTION	Bits [23:m]
0x2 - DITH5	23:5
0x3 - DITH6	23:6 (depicted)

Bits 5:0 – DITHERBUF[5:0]: Dithering Buffer Cycle Number
These bits represent the CCx.DITHER bits buffer. When the double buffering is enable, DITHERBUF bits value is copied to the CCx.DITHER bits on an UPDATE condition.
Note: This bit field consists of the n LSB of the register. n is dependent on the value of the Resolution bits in the Control A register (CTRLA.RESOLUTION):

CTRLA.RESOLUTION	Bits [n:0]
0x0 - NONE	-
0x1 - DITH4	3:0
0x2 - DITH5	4:0
0x3 - DITH6	5:0 (depicted)

Figure 37-15. JK Flip Flop



When the even LUT is disabled (LUTCTRL0.ENABLE=0 / LUTCTRL2.ENABLE=0), the flip-flop is asynchronously cleared. The reset command (R) is kept enabled for one APB clock cycle. In all other cases, the flip-flop output (OUT) is refreshed on rising edge of the GCLK_CCL, as shown in Table 37-3.

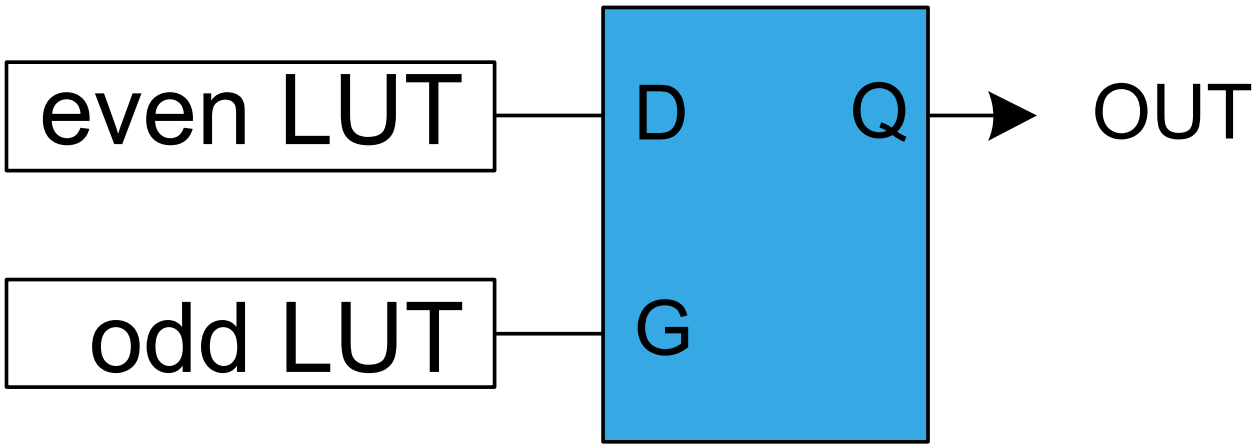
Table 37-3. JK Characteristics

R	J	K	OUT
1	X	X	Clear
0	0	0	Hold state (no change)
0	0	1	Clear
0	1	0	Set
0	1	1	Toggle

Gated D-Latch (DLATCH)

When the DLATCH is selected, the D-input is driven by the even LUT output (LUT0 and LUT2), and the G-input is driven by the odd LUT output (LUT1 and LUT3), as shown in Figure 37-14.

Figure 37-16. D-Latch



When the even LUT is disabled (LUTCTRL0.ENABLE=0 / LUTCTRL2.ENABLE=0), the latch output will be cleared. The G-input is forced enabled for one more APB clock cycle, and the D-input to zero. In all other cases, the latch output (OUT) is refreshed as shown in Table 37-4.

Bit 0 – SWRST: Synchronization Busy
This bit is cleared when the synchronization of CTRLA.SWRST is complete.

This bit is set when the synchronization of CTRLA.SWRST is started.

44.8.9 Value

Name: VALUE
Offset: 0x10 [ID-00000e03]
Reset: 0x00000000
Property: –

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	VALUE[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	VALUE[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	VALUE[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 23:0 – VALUE[23:0]: Measurement Value
Result from measurement.

45.10.4 Analog-to-Digital Converter (ADC) Characteristics

Table 45-18. Operating Conditions(1)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
Res	Resolution		-	-	12	bits
Rs	Sampling rate		10	-	1000	ksps
fs	Sampling clock		10	-	1000	kHz
	Differential mode Number of ADC clock cycles SAMPCTRL.OFFCOMP=1	resolution 12 bit (CTRLC.RESSEL=0)	-	16	-	cycles
		resolution 10 bit (CTRLC.RESSEL=2)		14		
		resolution 8 bit (CTRLC.RESSEL=3)		12		
	Differential mode Number of ADC clock cycles SAMPCTRL.OFFCOMP=0 SAMPLEN corresponds to the decimal value of SAMPCTRL.SAMPLEN[5:0] register	resolution 12 bit (CTRLC.RESSEL=0)	-	SAMPLEN +13	-	cycles
		resolution 10 bit (CTRLC.RESSEL=2)		SAMPLEN +11		
		resolution 8 bit (CTRLC.RESSEL=3)		SAMPLEN+9		
	Single-ended mode Number of ADC clock cycles SAMPCTRL.OFFCOMP=1	resolution 12 bit (CTRLC.RESSEL=0)	-	16	-	cycles
		resolution 10 bit (CTRLC.RESSEL=2)		15		
		resolution 8 bit (CTRLC.RESSEL=3)		13		
	Single-ended mode Number of ADC clock cycles SAMPCTRL.OFFCOMP=0 SAMPLEN corresponds to the decimal value of SAMPCTRL.SAMPLEN[5:0] register	resolution 12 bit (CTRLC.RESSEL=0)	-	SAMPLEN +13	-	cycles
		resolution 10 bit (CTRLC.RESSEL=2)		SAMPLEN +12		
		resolution 8 bit (CTRLC.RESSEL=3)		SAMPLEN +10		
fadc	ADC Clock frequency	SAMPCTRL.OFFCOMP=1 or CTRLC.R2R=1	-	fs*16	-	Hz
		SAMPCTRL.OFFCOMP=0	-	fs*13	-	
Ts	Sampling time	SAMPCTRL.OFFCOMP=1 or CTRLC.R2R=1	250	-	25000	ns
		SAMPCTRL.OFFCOMP=0	76	-	7692	
	Sampling time with DAC as input	SAMPCTRL.OFFCOMP=1 or CTRLC.R2R=1	3000	-	25000	
		SAMPCTRL.OFFCOMP=0	3000	-	7692	
	Conversion range	Differential mode	-VREF	-	+VREF	V
	Conversion range	Single-ended mode	0	-	VREF	
Vref	Reference input	REFCTRL.REFCOMP=1	2	-	VDDANA-0.6	V
		REFCTRL.REFCOMP=0	VDDANA	-	VDDANA	
Vin	Input channel range	-	0	-	VDDANA	V

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
		Single-Ended mode	1/(Cin x CLK_SDADC_FS x 2)			
	Input anti-alias filter recommendation (2)	R_{EXT}	-	1.0	-	kΩ
		C_{EXT}	3.3	-	10	nF

1. These are based on simulation. These values are not covered by test or characterization.
2. External Anti-alias filter must be placed in front of each SDADC input to ensure high-frequency signals to not alias into measurement bandwidth. Use capacitors of X5R type for DC measurement, or capacitors of COG or NPO type for AC measurement.

Table 45-23. SDADC DC Performance: Differential Input Mode (1)(2)

Symbol	Parameters	Conditions (2)	Min	Typ	Max	Unit
INL	Integral Non Linearity	CLK_SDADC = 6MHz; VREF = 1.2V	-	+/-1.3	+/-2	LSB
		CLK_SDADC = 6MHz; INT VREF = 5.5V	-	+/-5.3	+/-11	
DNL	Differential Non Linearity	CLK_SDADC = 6MHz; VREF = 1.2V	-	+1.4/-1	+1.3/-1	LSB
		CLK_SDADC = 6MHz; INT VREF = 5.5V	-	+2.1/-1	+1.7/-1	
Off	Offset Error	CLK_SDADC = 6MHz; VREF = 1.2V	-	+/-0.6	+/-3	mV
		CLK_SDADC = 6MHz; INT VREF = 5.5V	-	+/-3.9	+/-6	
Tco	Offset Error Drift	CLK_SDADC = 6MHz; VREF = 1.2V	2,3	3,6	5,0	uV/°C
Eg	Gain Errors	CLK_SDADC = 6MHz; VREF = 1.2V	-	+/-1.1	+/-3.7	%
		CLK_SDADC = 6MHz; INT VREF = 5.5V	-	+/-1.1	+/-3.4	
TCg	Gain Drift	CLK_SDADC = 6MHz; VREF = 1.2V	-10,9	1,2	7,6	ppm/°C
Input noise rms	AC Input noise rms	OSR = 256	-	0,08	0,12	mVrms

1. These are based on characterization.
2. OSR=256, Chopper ON, INL at -3dB.

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
		XOSC.GAIN=2				
		F = 16MHz CL=20pF XOSC.GAIN=3	-	10.8	18.1	
		F = 32MHz CL=18pF XOSC.GAIN=4	-	8.7	15.4	

1. These are based on characterization.

Table 45-41. Power Consumption (1)

Symbol	Parameters	Conditions	Ta	Typ.	Max	Units
IDD	Current consumption	F = 2MHz CL=20pF XOSC.GAIN=0 VDD = 5.0V AGC=OFF	Max 85°C Typ 25°C	150	202	µA
		AGC=ON		138	192	
		F = 4MHz CL=20pF XOSC.GAIN=1 VDD = 5.0V AGC=OFF		220	288	
		AGC=ON		175	260	
		F = 8MHz CL=20pF XOSC.GAIN=2 VDD = 5.0V AGC=OFF		350	416	
		AGC=ON		247	321	
		F = 16MHz CL=20pF XOSC.GAIN=3 VDD = 5.0V		663	843	

1. These values are only given as a typical example.

2. The capacitors should be placed close to the device for each supply pin pair in the signal group.

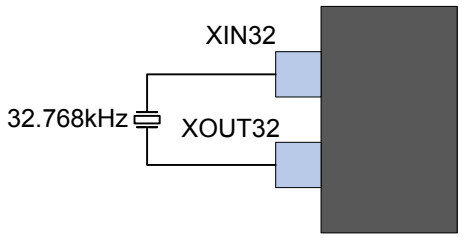
49.7.3 External Real Time Oscillator

The low frequency crystal oscillator is optimized for use with a 32.768kHz watch crystal. When selecting crystals, load capacitance and the crystal's Equivalent Series Resistance (ESR) must be taken into consideration. Both values are specified by the crystal vendor.

SAM C20/C21 oscillator is optimized for very low power consumption, hence close attention should be made when selecting crystals.

The typical parasitic load capacitance values are available in the Electrical Characteristics section. This capacitance and PCB capacitance can allow using a crystal inferior to 12.5pF load capacitance without external capacitors as shown in Figure 49-8.

Figure 49-8. External Real Time Oscillator without Load Capacitor



To improve accuracy and Safety Factor, the crystal datasheet can recommend adding external capacitors as shown in Figure 49-9.

To find suitable load capacitance for a 32.768kHz crystal, consult the crystal datasheet.

Figure 49-9. External Real Time Oscillator with Load Capacitor

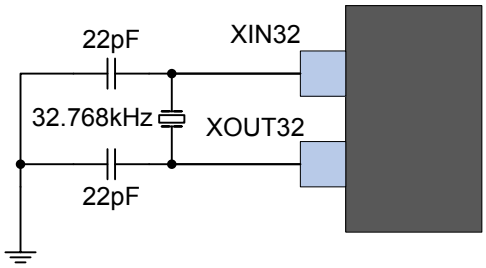


Table 49-6. External Real Time Oscillator Checklist

Signal Name	Recommended Pin Connection	Description
XIN32	Load capacitor 22pF(1)(2)	Timer oscillator input
XOUT32	Load capacitor 22pF(1)(2)	Timer oscillator output

1. These values are only given as typical examples.

2. The capacitors should be placed close to the device for each supply pin pair in the signal group.

Note: In order to minimize the cycle-to-cycle jitter of the external oscillator, keep the neighboring pins as steady as possible. For neighboring pin details, refer to the Oscillator Pinout section.