

#### Welcome to E-XFL.COM

#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

ĿХF

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I <sup>2</sup> C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, WDT
Number of I/O	38
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 14x12b, 2x16b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamc21g17a-ant

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

## Table 1-4. SAM C20 Family Features

	SAM C20N	SAM C20J	SAM C20G	SAM C20E
Pins	100	64 (56 for WLCSP)	48 (44 for WLCSP)	32
General Purpose I/O-pins (GPIOs)	84	52	38	26
Flash	256/128 KB	256/128/64/32 KB	256/128/64/32 KB	256/128/64/32 KB
Flash RWW section	8/4 KB	8/4/2/1 KB	8/4/2/1 KB	8/4/2/1 KB
System SRAM	32/16 KB	32/16/8/4 KB	32/16/8/4 KB	32/16/8/4 KB
Timer Counter (TC) instances	8	5	5	5
Waveform output channels per TC instance	2	2	2	2
TC Maximum and Minimum Capture	Yes	No	No	No
Timer Counter for Control (TCC) instances	3	3	3	3
Waveform output channels per TCC	8/4/2	8/4/2	8/4/2	6/4/2
DMA channels	12	12	12	12
Configurable Custom Logic (CCL) (LUTs)	4	4	4	4
Serial Communication Interface (SERCOM) instances	8	4	4	4
Divide and Square Root Accelerator (DIVAS)	Yes	Yes	Yes	Yes
Analog-to-Digital Converter (ADC) channels	12	12	12	10
Analog-to-Digital Converter (ADC) instances	1	1	1	1
Analog Comparators (AC)	2	2	2	2
Real-Time Counter (RTC)	Yes	Yes	Yes	Yes
RTC alarms	1	1	1	1
RTC compare values	One 32-bit value or	One 32-bit value or	One 32-bit value or	One 32-bit value or
	two 16-bit values	two 16-bit values	two 16-bit values	two 16-bit values
External Interrupt lines	16 with HW debouncing	16	16	16

## 4.2 SAM C21G / SAM C20G

#### 4.2.1 QFN48 / TQFP48



 Name:
 SYNCBUSY

 Offset:
 0x04

 Reset:
 0x0000000

 Property:
 –



#### Bits 2, 3, 4, 5, 6, 7, 8, 9 – GENCTRL: Generator Control n Synchronization Busy

This bit is cleared when the synchronization of the Generator Control n register (GENCTRLn) between clock domains is complete, or when clock switching operation is complete.

This bit is set when the synchronization of the Generator Control n register (GENCTRLn) between clock domains is started.

#### Bit 0 – SWRST: Software Reset Synchronization Busy

This bit is cleared when the synchronization of the CTRLA.SWRST register bit between clock domains is complete.

This bit is set when the synchronization of the CTRLA.SWRST register bit between clock domains is started.

#### 16.8.3 Generator Control

GENCTRLn controls the settings of Generic Generator n (n=0..8). The reset value is 0x00000106 for Generator n=0, else 0x00000000

Name: GENCTRL0, GENCTRL1, GENCTRL2, GENCTRL3, GENCTRL4, GENCTRL5, GENCTRL6, GENCTRL7, GENCTRL8
 Offset: 0x20 + n\*0x04 [n=0..8]
 Reset: 0x00000106

Property: PAC Write-Protection, Write-Synchronized

## 18. **RSTC – Reset Controller**

## 18.1 Overview

The Reset Controller (RSTC) manages the reset of the microcontroller. It issues a microcontroller reset, sets the device to its initial state and allows the reset source to be identified by software.

## 18.2 Features

- Reset the microcontroller and set it to an initial state according to the reset source
- Reset cause register for reading the reset source from the application code
- Multiple reset sources
  - Power supply reset sources: POR, BODCORE, BODVDD
  - User reset sources: External reset (RESET), Watchdog reset, and System Reset Request

## 18.3 Block Diagram

#### Figure 18-1. Reset System



## 18.4 Signal Description

Signal Name	Туре	Description
RESET	Digital input	External reset

One signal can be mapped on several pins.

#### **Related Links**

I/O Multiplexing and Considerations

## 18.5 Product Dependencies

In order to use this peripheral, other parts of the system must be configured correctly, as described below.

Some registers require synchronization when read and/or written. Synchronization is denoted by the "Read-Synchronized" and/or "Write-Synchronized" property in each individual register description.

Optional write-protection by the Peripheral Access Controller (PAC) is denoted by the "PAC Write-Protection" property in each individual register description.

Some registers are enable-protected, meaning they can only be written when the module is disabled. Enable-protection is denoted by the "Enable-Protected" property in each individual register description.

#### 24.12.1 Control A in Clock/Calendar mode (CTRLA.MODE=2)

 Name:
 CTRLA

 Offset:
 0x00

 Reset:
 0x0000

 Property:
 PAC Write-Protection, Enable-Protected, Write-Synchronized

Bit	15	14	13	12	11	10	9	8
	CLOCKSYNC				PRESCALER[3:0]			
Access	R/W				R/W	R/W	R/W	R/W
Reset	0				0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MATCHCLR	CLKREP			MOD	E[1:0]	ENABLE	SWRST
Access	R/W	R/W			R/W	R/W	R/W	R/W
Reset	0	0			0	0	0	0

#### Bit 15 – CLOCKSYNC: CLOCK Read Synchronization Enable

The CLOCK register requires synchronization when reading. Disabling the synchronization will prevent reading valid values from the CLOCK register.

This bit is not enable-protected.

Value	Description
0	CLOCK read synchronization is disabled
1	CLOCK read synchronization is enabled

#### Bits 11:8 – PRESCALER[3:0]: Prescaler

These bits define the prescaling factor for the RTC clock source (GCLK\_RTC) to generate the counter clock (CLK\_RTC\_CNT). Periodic events and interrupts are not available when the prescaler is off. These bits are not synchronized.

Value	Name	Description
0x0	OFF	CLK_RTC_CNT = GCLK_RTC/1
0x1	DIV1	CLK_RTC_CNT = GCLK_RTC/1
0x2	DIV2	CLK_RTC_CNT = GCLK_RTC/2
0x3	DIV4	CLK_RTC_CNT = GCLK_RTC/4
0x4	DIV8	CLK_RTC_CNT = GCLK_RTC/8
0x5	DIV16	CLK_RTC_CNT = GCLK_RTC/16
0x6	DIV32	CLK_RTC_CNT = GCLK_RTC/32
0x7	DIV64	CLK_RTC_CNT = GCLK_RTC/64
0x8	DIV128	CLK_RTC_CNT = GCLK_RTC/128
0x9	DIV256	CLK_RTC_CNT = GCLK_RTC/256

Each DMA channel supports a 4-level priority scheme. The priority level for a channel is configured by writing to the Channel Arbitration Level bit group in the Channel Control B register (CHCTRLB.LVL). As long as all priority levels are enabled, a channel with a higher priority level number will have priority over a channel with a lower priority level number. Each priority level x is enabled by setting the corresponding Priority Level x Enable bit in the Control register (CTRL.LVLENx=1).

Within each priority level the DMAC's arbiter can be configured to prioritize statically or dynamically:

*Static Arbitration* within a priority level is selected by writing a '0' to the Level x Round-Robin Scheduling Enable bit in the Priority Control 0 register (PRICTRL0.RRLVLENx).

When static arbitration is selected, the arbiter will prioritize a low channel number over a high channel number as shown in the figure below. When using the static arbitration there is a risk of high channel numbers never being granted access as the active channel. This can be avoided using a dynamic arbitration scheme.





*Dynamic Arbitration* within a priority level is selected by writing a '1' to **PRICTRL0.RRLVLENx**.

The dynamic arbitration scheme in the DMAC is round-robin. With the round-robin scheme, the channel number of the last channel being granted access will have the lowest priority the next time the arbiter has to grant access to a channel within the same priority level, as shown in Figure 25-6. The channel number of the last channel being granted access as the active channel is stored in the Level x Channel Priority Number bit group in the Priority Control 0 register (PRICTRL0.LVLPRIx) for the corresponding priority level.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access		•	•					
Reset								
Bit	15	14	13	12	11	10	9	8
					BUSYCHn	BUSYCHn	BUSYCHn	BUSYCHn
Access		•			R	R	R	R
Reset					0	0	0	0
Bit	7	6	5	4	3	2	1	0
	BUSYCHn							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

#### Bits 11:0 – BUSYCHn: Busy Channel n [x=11..0]

This bit is cleared when the channel trigger action for DMA channel n is complete, when a bus error for DMA channel n is detected, or when DMA channel n is disabled.

This bit is set when DMA channel n starts a DMA transfer.

#### 25.8.13 Pending Channels

 Name:
 PENDCH

 Offset:
 0x2C

 Reset:
 0x0000000

 Property:

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
								TICKON
Access			•		•	•		RW
Reset								0
Bit	15	14	13	12	11	10	9	8
	STATESx	F	RESCALERx[2:0	0]	STATESx	P	RESCALERx[2:0	0]
Access	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	STATESx	F	PRESCALERx[2:0	0]	STATESx	P	RESCALERx[2:0	0]
Access	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0

#### Bit 16 – TICKON: Pin Sampler frequency selection

This bit selects the clock used for the sampling of bounce during transition detection.

Value	Description
0	The bounce sampler is using GCLK_EIC.
1	The bounce sampler is using the low frequency clock.

#### Bits 3,7,11,15 – STATESx: Debouncer number of states x

This bit selects the number of samples by the debouncer low frequency clock needed to validate a transition from current pin state to next pin state in synchronous debouncing mode for pins EXTINT[7+(8x):8x].

Value	Description
0	The number of low frequency samples is 3.
1	The number of low frequency samples is 7.

#### Bits 2:0,6:4,10:8,14:12 – PRESCALERx: Debouncer Prescaler x

These bits select the debouncer low frequency clock for pins EXTINT[7+(8x):8x].

Value	Name	Description
0x0	F/2	EIC clock divided by 2
0x1	F/4	EIC clock divided by 4
0x2	F/8	EIC clock divided by 8
0x3	F/16	EIC clock divided by 16
0x4	F/32	EIC clock divided by 32
0x5	F/64	EIC clock divided by 64
0x6	F/128	EIC clock divided by 128
0x7	F/256	EIC clock divided by 256

#### 26.8.13 Pin State

- Output (OUT): I/O pin will be set when the incoming event has a high level ('1') and cleared when the incoming event has a low-level ('0').
- Set (SET): I/O pin will be set when an incoming event is detected.
- Clear (CLR): I/O pin will be cleared when an incoming event is detected.
- Toggle (TGL): I/O pin will toggle when an incoming event is detected.

The event is output to pin without any internal latency. For SET, CLEAR and TOGGLE event actions, the action will be executed up to three clock cycles after a rising edge.

The event actions can be configured with the Event Action m bit group in the Event Input Control register (EVCTRL.EVACTm). Writing a '1' to a PORT Event Enable Input m of the Event Control register (EVCTRL.PORTEIm) enables the corresponding action on input event. Writing '0' to this bit disables the corresponding action on input event. Note that several actions can be enabled for incoming events. If several events are connected to the peripheral, any enabled action will be taken for any of the incoming events. Refer to *EVSYS – Event System*. for details on configuring the Event System.

Each event input can address one and only one I/O pin at a time. The selection of the pin is indicated by the PORT Event Pin Identifier of the Event Input Control register (EVCTR.PIDn). On the other hand, one I/O pin can be addressed by up to four different input events. To avoid action conflict on the output value of the register (OUT) of this particular I/O pin, only one action is performed according to the table below.

Note that this truth table can be applied to any SET/CLR/TGL configuration from two to four active input events.

EVACT0	EVACT1	EVACT2	EVACT3	Executed Event Action
SET	SET	SET	SET	SET
CLR	CLR	CLR	CLR	CLR
All Other Comb	inations	TGL		

Table 28-3. Priority on Simultaneous SET/CLR/TGL Event Actions

Be careful when the event is output to pin. Due to the fact the events are received asynchronously, the I/O pin may have unpredictable levels, depending on the timing of when the events are received. When several events are output to the same pin, the lowest event line will get the access. All other events will be ignored.

#### **Related Links**

EVSYS – Event System

#### 28.6.5 PORT Access Priority

The PORT is accessed by different systems:

- The ARM<sup>®</sup> CPU through the high-speed matrix and the AHB/APB bridge (APB)
- EVSYS through four asynchronous input events

The following priority is adopted:

- 1. APB
- 2. EVSYS input events

For input events that require different actions on the same I/O pin, refer to Events.

Bit	31	30	29	28	27	26	25	24
				IN[3	1:24]			
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
				IN[2	3:16]			
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
				IN[1	5:8]			
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
				IN[	7:0]			
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

#### Bits 31:0 - IN[31:0]: PORT Data Input Value

These bits are cleared when the corresponding I/O pin input sampler detects a logical low level on the input pin.

These bits are set when the corresponding I/O pin input sampler detects a logical high level on the input pin.

#### 28.9.10 Control

**Tip:** The I/O pins are assembled in pin groups ("PORT groups") with up to 32 pins. Group 0 consists of the PA pins, group 1 is for the PB pins, etc. Each pin group has its own PORT registers. For example, the register address offset for the Data Direction (DIR) register for group 0 (PA00 to PA31) is 0x00, and the register address offset for the DIR register for group 1 (PB00 to PB31) is 0x80.

Name:CTRLOffset:0x24Reset:0x00000000Property:PAC Write-Protection

USERm	User Multiplexer	Description	Path Type
m = 9	TCC0 EV0	-	Asynchronous, synchronous, and resynchronized paths
m = 10	TCC0 EV1	-	Asynchronous, synchronous, and resynchronized paths
m = 11	TCC0 MC0	Match/Capture 0	Asynchronous, synchronous, and resynchronized paths
m = 12	TCC0 MC1	Match/Capture 1	Asynchronous, synchronous, and resynchronized paths
m = 13	TCC0 MC2	Match/Capture 2	Asynchronous, synchronous, and resynchronized paths
m = 14	TCC0 MC3	Match/Capture 3	Asynchronous, synchronous, and resynchronized paths
m = 15	TCC1 EV0	-	Asynchronous, synchronous, and resynchronized paths
m = 16	TCC1 EV1	-	Asynchronous, synchronous, and resynchronized paths
m = 17	TCC1 MC0	Match/Capture 0	Asynchronous, synchronous, and resynchronized paths
m = 18	TCC1 MC1	Match/Capture 1	Asynchronous, synchronous, and resynchronized paths
m = 19	TCC2 EV0	-	Asynchronous, synchronous, and resynchronized paths
m = 20	TCC2 EV1	-	Asynchronous, synchronous, and resynchronized paths
m = 21	TCC2 MC0	Match/Capture 0	Asynchronous, synchronous, and resynchronized paths
m = 22	TCC2 MC1	Match/Capture 1	Asynchronous, synchronous, and resynchronized paths

CPOL	TxD Change	RxD Sample
0x0	Rising XCK edge	Falling XCK edge
0x1	Falling XCK edge	Rising XCK edge

#### Bit 28 – CMODE: Communication Mode

This bit selects asynchronous or synchronous communication.

This bit is not synchronized.

Value	Description
0	Asynchronous communication.
1	Synchronous communication.

#### Bits 27:24 – FORM[3:0]: Frame Format

These bits define the frame format.

These bits are not synchronized.

FORM[3:0]	Description
0x0	USART frame
0x1	USART frame with parity
0x2	LIN Master - Break and sync generation. See LIN Command (CTRLB.LINCMD).
0x3	Reserved
0x4	Auto-baud - break detection and auto-baud.
0x5	Auto-baud - break detection and auto-baud with parity
0x6-0xF	Reserved

#### Bits 23:22 – SAMPA[1:0]: Sample Adjustment

These bits define the sample adjustment.

These bits are not synchronized.

SAMPA[1:0]	16x Over-sampling (CTRLA.SAMPR=0 or 1)	8x Over-sampling (CTRLA.SAMPR=2 or 3)
0x0	7-8-9	3-4-5
0x1	9-10-11	4-5-6
0x2	11-12-13	5-6-7
0x3	13-14-15	6-7-8

#### Bits 21:20 – RXPO[1:0]: Receive Data Pinout

These bits define the receive data (RxD) pin configuration.

These bits are not synchronized.

 Name:
 DATA

 Offset:
 0x28 [ID-00000fa7]

 Reset:
 0x0000

 Property:



### Bits 8:0 - DATA[8:0]: Data

Reading these bits will return the contents of the Receive Data register. The register should be read only when the Receive Complete Interrupt Flag bit in the Interrupt Flag Status and Clear register (INTFLAG.RXC) is set. The status bits in STATUS should be read before reading the DATA value in order to get any corresponding error.

Writing these bits will write the Transmit Data register. This register should be written only when the Data Register Empty Interrupt Flag bit in the Interrupt Flag Status and Clear register (INTFLAG.DRE) is set.

### 31.8.12 Debug Control

Name:DBGCTRLOffset:0x30 [ID-00000fa7]Reset:0x00Property:PAC Write-Protection



#### Bit 0 – DBGSTOP: Debug Stop Mode

This bit controls the baud-rate generator functionality when the CPU is halted by an external debugger.

Value	Description
0	The baud-rate generator continues normal operation when the CPU is halted by an external
	debugger.
1	The baud-rate generator is halted when the CPU is halted by an external debugger.

**Startup Timing** The minimum time between SDA transition and SCL rising edge is 6 APB cycles when the DATA register is written in smart mode. If a greater startup time is required due to long rise times, the time between DATA write and IF clear must be controlled by software.

**Note:** When timing is controlled by user, the Smart Mode cannot be enabled.

### **Related Links**

Electrical Characteristics 85°C (SAM C20/C21 E/G/J)

#### Master Clock Generation (High-Speed Mode)

For I<sup>2</sup>C *Hs* transfers, there is no SCL synchronization. Instead, the SCL frequency is determined by the GCLK\_SERCOMx\_CORE frequency ( $f_{GCLK}$ ) and the High-Speed Baud setting in the Baud register (BAUD.HSBAUD). When BAUD.HSBAUDLOW=0, the HSBAUD value will determine both SCL high and SCL low. In this case the following formula determines the SCL frequency.

$$f_{\rm SCL} = \frac{f_{\rm GCLK}}{2 + 2 \cdot HS \, BAUD}$$

When HSBAUDLOW is non-zero, the following formula determines the SCL frequency.

$$f_{\rm SCL} = \frac{f_{\rm GCLK}}{2 + HS \, BAUD + HSBAUDLOW}$$

**Note:** The I<sup>2</sup>C standard *Hs* (High-speed) requires a nominal high to low SCL ratio of 1:2, and HSBAUD should be set accordingly. At a minimum, BAUD.HSBAUD and/or BAUD.HSBAUDLOW must be non-zero.

### **Transmitting Address Packets**

The I<sup>2</sup>C master starts a bus transaction by writing the I<sup>2</sup>C slave address to ADDR.ADDR and the direction bit, as described in Principle of Operation. If the bus is busy, the I<sup>2</sup>C master will wait until the bus becomes idle before continuing the operation. When the bus is idle, the I<sup>2</sup>C master will issue a start condition on the bus. The I<sup>2</sup>C master will then transmit an address packet using the address written to ADDR.ADDR. After the address packet has been transmitted by the I<sup>2</sup>C master, one of four cases will arise according to arbitration and transfer direction.

## Case 1: Arbitration lost or bus error during address packet transmission

If arbitration was lost during transmission of the address packet, the Master on Bus bit in the Interrupt Flag Status and Clear register (INTFLAG.MB) and the Arbitration Lost bit in the Status register (STATUS.ARBLOST) are both set. Serial data output to SDA is disabled, and the SCL is released, which disables clock stretching. In effect the I<sup>2</sup>C master is no longer allowed to execute any operation on the bus until the bus is idle again. A bus error will behave similarly to the arbitration lost condition. In this case, the MB interrupt flag and Master Bus Error bit in the Status register (STATUS.BUSERR) are both set in addition to STATUS.ARBLOST.

The Master Received Not Acknowledge bit in the Status register (STATUS.RXNACK) will always contain the last successfully received acknowledge or not acknowledge indication.

In this case, software will typically inform the application code of the condition and then clear the interrupt flag before exiting the interrupt routine. No other flags have to be cleared at this moment, because all flags will be cleared automatically the next time the ADDR.ADDR register is written.

## Case 2: Address packet transmit complete – No ACK received

If there is no I<sup>2</sup>C slave device responding to the address packet, then the INTFLAG.MB interrupt flag and STATUS.RXNACK will be set. The clock hold is active at this point, preventing further activity on the bus.

Value	Description
0	Error_Warning status unchanged.
1	Error_Warning status changed.

#### Bit 23 – EP: Error Passive

Value	Description
0	Error_Passive status unchanged.
1	Error_Passive status changed.

#### Bit 22 – ELO: Error Logging Overflow

Value	Description
0	CAN Error Logging Counter did not overflow.
1	Overflow of CAN Error Logging Counter occurred.

#### Bit 21 – BEU: Bit Error Uncorrected

Message RAM bit error detected, uncorrected. Generated by an optional external parity / ECC logic attached to the Message RAM. An uncorrected Message RAM bit sets CCCR.INIT to 1. This is done to avoid transmission of corrupted data.

Value	Description
0	Not bit error detected when reading from Message RAM.
1	Bit error detected, uncorrected (e.g. parity logic).

#### Bit 20 – BEC: Bit Error Corrected

Message RAM bit error detected and corrected. Generated by an optional external parity / ECC logic attached to the Message RAM.

Value	Description
0	Not bit error detected when reading from Message RAM.
1	Bit error detected and corrected (e.g. ECC).

#### Bit 19 – DRX: Message stored to Dedicated Rx Buffer

The flag is set whenever a received message has been stored into a dedicated Rx Buffer.

Value	Description
0	No Rx Buffer updated.
1	At least one received message stored into a Rx Buffer.

### Bit 18 – TOO: Timeout Occurred

Value	Description
0	No timeout.
1	Timeout reached.

#### Bit 17 – MRAF: Message RAM Access Failure

The flag is set, when the Rx Handler

- has not completed acceptance filtering or storage of an accepted message until the arbitration field of the following message has been received. In this case acceptance filtering or message storage is aborted and the Rx Handler starts processing of the following message.
- was not able to write a message to the Message RAM. In this case message storage is aborted.

Bit	31	30	29	28	27	26	25	24
	NDn							
Access	R/W							
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	NDn							
Access	R/W							
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	NDn							
Access	R/W							
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	NDn							
Access	R/W							
Reset	0	0	0	0	0	0	0	0

#### Bits 31:0 – NDn: New Data n [n = 0..31]

The register holds the New Data flags of Rx Buffers 0 to 31. The flags are set when the respective Rx Buffer has been updated from a received frame. The flags remain set until the Host clears them. A flag is cleared by writing 1 to the corresponding bit position. Writing a 0 has no effect. A hard reset will clear the register.

### 34.8.26 New Data 2

 Name:
 NDAT2

 Offset:
 0x9C

 Reset:
 0x0000000

 Property:





#### Bit 0 – DBGRUN: Run in Debug Mode

This bit is not affected by a software Reset, and should not be changed by software while the TC is enabled.

Value	Description
0	The TC is halted when the device is halted in debug mode.
1	The TC continues normal operation when the device is halted in debug mode.

#### 35.7.2.12 Synchronization Busy

Name:	SYNCBUSY
Offset:	0x10
Reset:	0x00000000
<b>Property:</b>	-

Bit	31	30	29	28	27	26	25	24
Access							•	
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
		CCx	PER	COUNT	STATUS	CTRLB	ENABLE	SWRST
Access		R	R	R	R	R	R	R
Reset		0	0	0	0	0	0	0

## Bit 6 – CCx: Compare/Capture Channel x Synchronization Busy

For details on CC channels number, refer to each TC feature list.

Value	Name	Description	
0x3	RAMP2C	Critical RAMP2 operation	
0x4			

#### Bits 2:0 – WAVEGEN[2:0]: Waveform Generation Operation

These bits select the waveform generation operation. The settings impact the top value and control if frequency or PWM waveform generation should be used. These bits are not synchronized.

Value	Name	Description						
		Operation	Тор	Update	Waveform Output On Match	Waveform Output On Update	OVFIF/ Up Dov	Event wn
0x0	NFRQ	Normal Frequency	PER	TOP/Zero	Toggle	Stable	TOP	Zero
0x1	MFRQ	Match Frequency	CC0	TOP/Zero	Toggle	Stable	TOP	Zero
0x2	NPWM	Normal PWM	PER	TOP/Zero	Set	Clear	TOP	Zero
0x3								
0x4	DSCRITICAL	Dual-slope PWM	PER	Zero	~DIR	Stable	-	Zero
0x5	DSBOTTOM	Dual-slope PWM	PER	Zero	~DIR	Stable	-	Zero
0x6	DSBOTH	Dual-slope PWM	PER	TOP & Zero	~DIR	Stable	TOP	Zero
0x7	DSTOP	Dual-slope PWM	PER	Zero	~DIR	Stable	TOP	-

#### 36.8.17 Period Value

Name:PEROffset:0x40 [ID-00002e48]Reset:0xFFFFFFFProperty:Write-Synchronized

Name:CTRLAOffset:0x00 [ID-00000bc7]Reset:0x00Property:PAC Write-Protection, Write-Synchronized



### Bit 6 – RUNSTDBY: Run in Standby

This bit is not synchronized

Value	Description
0	The DAC output buffer is disabled in standby sleep mode.
1	The DAC output buffer can be enabled in standby sleep mode.

#### Bit 1 – ENABLE: Enable DAC Controller

Due to synchronization there is delay from writing CTRLA.ENABLE until the peripheral is enabled/ disabled. The value written to CTRLA.ENABLE will read back immediately and the corresponding bit in the Synchronization Busy register (SYNCBUSY.ENABLE) will be set. SYNCBUSY.ENABLE will be cleared when the operation is complete.

Value	Description
0	The peripheral is disabled or being disabled.
1	The peripheral is enabled or being enabled.

#### Bit 0 – SWRST: Software Reset

Writing '0' to this bit has no effect.

Writing '1' to this bit resets all registers in the DAC to their initial state, and the DAC will be disabled.

Writing a '1' to CTRLA.SWRST will always take precedence, meaning that all other writes in the same write-operation will be discarded.

Due to synchronization there is a delay from writing CTRLA.SWRST until the reset is complete. CTRLA.SWRST and SYNCBUSY.SWRST will both be cleared when the reset is complete.

Value	Description
0	There is no reset operation ongoing.
1	The reset operation is ongoing.

#### 41.8.2 Control B

Name:CTRLBOffset:0x01 [ID-00000bc7]Reset:0x00Property:PAC Write-Protection, Enable-Protected

Table 48-14. Device and Package Maximum Weight				
140	mg			
Table 48-15. Package Characteristics				
Moisture Sensitivity Level MSL3				
Table 48-16. Package Reference				
JEDEC Drawing Reference	MS-026			
JESD97 Classification	E3			