What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, WDT
Number of I/O	38
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 14x12b, 2x16b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamc21g18a-mnt

Signal Name	Function	Type	Active Level
Timer Counter - TCCx			
WO[1:0]	Waveform Outputs	Digital	
Peripheral Touch Controller - PTC			
X[15:0]	PTC Input	Analog	
Y[15:0]	PTC Input	Analog	
General Purpose I/O - PORT			
PA25 - PA00	Parallel I/O Controller I/O Port A	Digital	
PA28 - PA27	Parallel I/O Controller I/O Port A	Digital	
PA31 - PA30	Parallel I/O Controller I/O Port A	Digital	
PB17 - PB00	Parallel I/O Controller I/O Port B	Digital	
PB21 - PB19	Parallel I/O Controller I/O Port B	Digital	
PB25 - PB22	Parallel I/O Controller I/O Port B	Digital	
PB31 - PB30	Parallel I/O Controller I/O Port B	Digital	
PC03 - PC-00	Parallel I/O Controller I/O Port C	Digital	
PC21 - PC05	Parallel I/O Controller I/O Port C	Digital	
PC28 - PC24	Parallel I/O Controller I/O Port C	Digital	
Controller Area Network - CAN			
TX	CAN Transmit Line	Digital	
RX	CAN Receive Line	Digital	

Peripheral Name	Base Address	IRQ Line	AHB Clock		APB Clock		Generic Clock	PAC		Events		DMA	Sleep Walking
			Index	Enabled at Reset	Index	Enabled at Reset	Index	Index	Prot at Reset	User	Generator	Index	
SERCOM3	0x42001000	12			4	N	22: CORE 18: SLOW	4	N			8: RX 9: TX	Y
SERCOM4	0x42001400	13			5	N	23: CORE 18: SLOW	5	N			10: RX 11: TX	Y
SERCOM5	0x42001800	14			6	N	25: CORE 24: SLOW	6	N			12: RX 13: TX	Y
TCC0	0x42002400	17			9	N	28	9	N	9-10: EV0-1 11-14: MC0-3	34: OVF 35: TRG 36: CNT 37-40: MC0-3	16: OVF 17-20: MC0-3	Y
TCC1	0x42002800	18			10	N	28	10	N	15-16: EV0-1 17-18: MC0-1	41: OVF 42: TRG 43: CNT 44-45: MC0-1	21: OVF 22-23: MC0-1	Y
TCC2	0x42002C00	19			11	N	29	11	N	19-20: EV0-1 21-22: MC0-1	46: OVF 47: TRG 48: CNT 49-50: MC0-1	24: OVF 25-26: MC0-1	Y
TC0	0x42003000	20			12	N	30	12	N	23: EVU	51: OVF 52-53: MC0-1	27: OVF 28-29: MC0-1	Y
TC1	0x42003400	21			13	N	30	13	N	24: EVU	54: OVF 55-56: MC0-1	30: OVF 21-32: MC0-1	Y
TC2	0x42003800	22			14	N	31	14	N	25: EVU	57: OVF 58-59: MC0-1	33: OVF 23-35: MC0-1	Y
TC3	0x42003C00	23			15	N	31	15	N	26: EVU	60: OVF 61-62: MC0-1	36: OVF 37-38: MC0-1	Y
TC4	0x42004000	24			16	N	32	16	N	27: EVU	63: OVF 64-65: MC0-1	39: OVF 40-41: MC0-1	Y
ADC0	0x42004400	25			17	N	33	17	N	28: START 29: SYNC	66: RESRDY 67: WINMON	42: RESRDY	Y
AC	0x42005000	27			20	N	34	20	N	34-37: SOC0-3	72-75: COMP0-3 76-77: WIN0-1		Y
PTC	0x42005800	30			22	N	37	22	N	39: STCONV	79: EOC 80: WCOMP	EOC: 46 WCOMP: 47 SEQ: 48	
CCL	0x42005C00				23	N	38	23	N	40-43 : LUTIN0-3	781-84: LUTOUT0-3		Y
DIVAS	0x48000000		12	Y									N/A

14. DIVAS – Divide and Square Root Accelerator

14.1 Overview

The Divide and Square Root Accelerator (DIVAS) is a programmable 32-bit signed or unsigned hardware divider and a 32-bit unsigned square root hardware engine. The DIVAS is connected to the high-speed bus matrix and may also be accessed using the low-latency CPU local bus (IOBUS; ARM® single-cycle I/O port). The DIVAS takes dividend and divisor values and returns the quotient and remainder when it is used as divider. The DIVAS takes unsigned input value and returns its square root and remainder when it is used as square root function.

14.2 Features

- Division accelerator for Cortex-M0+ systems
- 32-bit signed or unsigned integer division
- 32-bit unsigned square root
- 32-bit division in 2-16 cycles
- Programmable leading zero optimization
- Result includes quotient and remainder
- Result includes square root and remainder
- Busy and Divide-by-zero status
- Automatic start of operation when divisor or square root input is loaded

14.3 Block Diagram

Figure 14-1. DIVAS Block Diagram
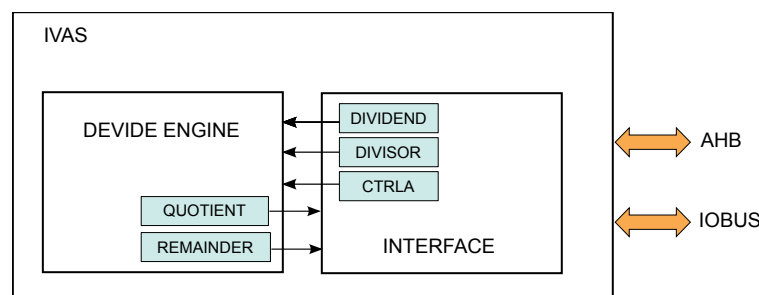
14.4 Signal Description

Not applicable

14.5 Product Dependencies

In order to use this peripherial, other parts of the system must be configured correctly, as described below.

15.6   Power Consumption vs. Speed

Due to the nature of the asynchronous clocking of the peripherals there are some considerations that needs to be taken if either targeting a low-power or a fast-acting system. If clocking a peripheral with a very low clock, the active power consumption of the peripheral will be lower. At the same time the synchronization to the synchronous (CPU) clock domain is dependent on the peripheral clock speed, and will be longer with a slower peripheral clock; giving lower response time and more time waiting for the synchronization to complete.

15.7   Clocks after Reset

On any reset the synchronous clocks start to their initial state:

- OSC48M is enabled and divided by 12
- GCLK_MAIN uses OSC48M as source
- CPU and BUS clocks are undivided

On a power reset the GCLK starts to their initial state:

- All generic clock generators disabled except:
    - The generator 0 (GCLK_MAIN) using OSC48M as source, with no division
- All generic clocks disabled

On a user reset the GCLK starts to their initial state, except for:

- Generic clocks that are write-locked (WRTLOCK is written to one prior to reset)

On any reset the clock sources are reset to their initial state except the 32KHz clock sources which are reset only by a power reset.

Value	Name	Description
0x06	OSC48M	OSC48M oscillator output
0x07	DPLL96M	DPLL96M output
0x08-0x1F	Reserved	Reserved for future use

A Power Reset will reset all GENCTRLn registers. the Reset values of the GENCTRLn registers are shown in table below.

Table 16-5. GENCTRLn Reset Value after a Power Reset

GCLK Generator	Reset Value after a Power Reset
0	0x00000106
others	0x00000000

A User Reset will reset the associated GENCTRL register unless the Generator is the source of a locked Peripheral Channel (PCHCTRLm.WRTLOCK=1). The reset values of the GENCTRL register are as shown in the table below.

Table 16-6. GENCTRLn Reset Value after a User Reset

GCLK Generator	Reset Value after a User Reset
0	0x00000106
others	No change if the generator is used by a Peripheral Channel m with PCHCTRLm.WRTLOCK=1 else 0x00000000

Related Links

PCHCTRL0, PCHCTRL1, PCHCTRL2, PCHCTRL3, PCHCTRL4, PCHCTRL5, PCHCTRL6, PCHCTRL7, PCHCTRL8, PCHCTRL9, PCHCTRL10, PCHCTRL11, PCHCTRL12, PCHCTRL13, PCHCTRL14, PCHCTRL15, PCHCTRL16, PCHCTRL17, PCHCTRL18, PCHCTRL19, PCHCTRL20, PCHCTRL21, PCHCTRL22, PCHCTRL23, PCHCTRL24, PCHCTRL25, PCHCTRL26, PCHCTRL27, PCHCTRL28, PCHCTRL29, PCHCTRL30, PCHCTRL31, PCHCTRL32, PCHCTRL33, PCHCTRL34, PCHCTRL35, PCHCTRL36, PCHCTRL37, PCHCTRL38, PCHCTRL39, PCHCTRL40, PCHCTRL41, PCHCTRL42, PCHCTRL43, PCHCTRL44, PCHCTRL45

16.8.4 Peripheral Channel Control

PCHTRLm controls the settings of Peripheral Channel number m (m=0..45).

Name: PCHCTRL0, PCHCTRL1, PCHCTRL2, PCHCTRL3, PCHCTRL4, PCHCTRL5, PCHCTRL6, PCHCTRL7, PCHCTRL8, PCHCTRL9, PCHCTRL10, PCHCTRL11, PCHCTRL12, PCHCTRL13, PCHCTRL14, PCHCTRL15, PCHCTRL16, PCHCTRL17, PCHCTRL18, PCHCTRL19, PCHCTRL20, PCHCTRL21, PCHCTRL22, PCHCTRL23, PCHCTRL24, PCHCTRL25, PCHCTRL26, PCHCTRL27, PCHCTRL28, PCHCTRL29, PCHCTRL30, PCHCTRL31, PCHCTRL32, PCHCTRL33, PCHCTRL34, PCHCTRL35, PCHCTRL36,

Bit 2 – TC5: TC5 APBd Mask Clock Enable

Value	Description
0	The APBD clock for the TC5 is stopped.
1	The APBD clock for the TC5 is enabled.

Bit 1 – SERCOM7: SERCOM7 APBD Mask Clock Enable

Value	Description
0	The APBD clock for the SERCOM7 is stopped.
1	The APBD clock for the SERCOM7 is enabled.

Bit 0 – SERCOM6: SERCOM6 APBD Mask Clock Enable

Value	Description
0	The APBD clock for the SERCOM6 is stopped.
1	The APBD clock for the SERCOM6 is enabled.

21.5.3 Clocks

The OSC32KCTRL gathers controls for all 32KHz oscillators and provides clock sources to the Generic Clock Controller (GCLK), Real-Time Counter (RTC), and Watchdog Timer (WDT).

The available clock sources are: XOSC32K, OSC32K, and OSCULP32K.

The OSC32KCTRL bus clock (CLK_OSC32KCTRL_APB) can be enabled and disabled in the Main Clock module (MCLK).

Related Links

Peripheral Clock Masking

21.5.4 Interrupts

The interrupt request lines are connected to the interrupt controller. Using the OSC32KCTRL interrupts requires the interrupt controller to be configured first.

Related Links

Nested Vector Interrupt Controller

21.5.5 Events

The events of this peripheral are connected to the Event System.

Related Links

EVSYS – Event System

21.5.6 Debug Operation

When the CPU is halted in debug mode, OSC32KCTRL will continue normal operation. If OSC32KCTRL is configured in a way that requires it to be periodically serviced by the CPU through interrupts or similar, improper operation or data loss may result during debugging.

21.5.7 Register Access Protection

All registers with write-access can be write-protected optionally by the Peripheral Access Controller (PAC), except for the following registers:

•   Interrupt Flag Status and Clear (INTFLAG) register

Optional write-protection by the Peripheral Access Controller (PAC) is denoted by the "PAC Write-Protection" property in each individual register description.

PAC write-protection does not apply to accesses through an external debugger.

Related Links

PAC - Peripheral Access Controller

21.5.8 Analog Connections

The external 32.768kHz crystal must be connected between the XIN32 and XOUT32 pins, along with any required load capacitors. For details on recommended oscillator characteristics and capacitor load, refer to the related links.

Related Links

Electrical Characteristics 85°C (SAM C20/C21 E/G/J)

21.5.9 Calibration

The OSC32K calibration value from the production test must be loaded from the NVM Software Calibration Area into the OSC32K register (OSC32K.CALIB) by software to achieve specified accuracy.

Protection" property in the register description. Write-protection does not apply to accesses through an external debugger.

Related Links

PAC - Peripheral Access Controller

21.8.1 Interrupt Enable Clear

This register allows the user to disable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Set register (INTENSET).

Name: INTENCLR
Offset: 0x00 [ID-00001010]
Reset: 0x00000000
Property: PAC Write-Protection

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
						CLKFAIL	OSC32KRDY	XOSC32KRDY
Access						R/W	R/W	R/W
Reset						0	0	0

Bit 2 – CLKFAIL: XOSC32K Clock Failure Detection Interrupt Enable
Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the XOSC32K Clock Failure Interrupt Enable bit, which disables the XOSC32K Clock Failure interrupt.

Value	Description
0	The XOSC32K Clock Failure Detection is disabled.
1	The XOSC32K Clock Failure Detection is enabled. An interrupt request will be generated when the XOSC32K Clock Failure Detection interrupt flag is set.

Bit 1 – OSC32KRDY: OSC32K Ready Interrupt Enable
Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the OSC32K Ready Interrupt Enable bit, which disables the OSC32K Ready interrupt.

Figure 25-2. DMA Transfer Sizes
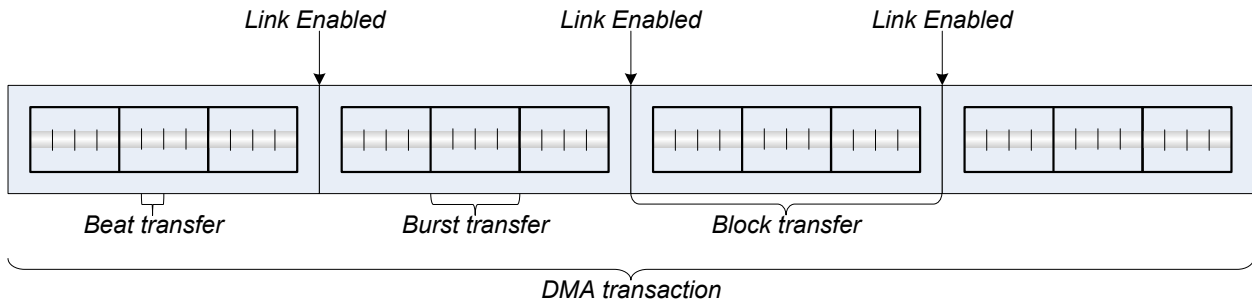
- Beat transfer: The size of one data transfer bus access, and the size is selected by writing the Beat Size bit group in the Block Transfer Control register (BTCTRL.BEATSIZE)
- Burst transfer: Defined as n beat transfers, where n will differ from one device family to another. A burst transfer is atomic, cannot be interrupted and the length of the burst is selected by writing the Burst Length bit group in each Channel n Control A register (CHCTRLA.BURSTLEN).
- Block transfer: The amount of data one transfer descriptor can transfer, and the amount can range from 1 to 64k beats. A block transfer can be interrupted, in contrast to the burst transfer.
- Transaction: The DMAC can link several transfer descriptors by having the first descriptor pointing to the second and so forth, as shown in the figure above. A DMA transaction is the complete transfer of all blocks within a linked list.

A transfer descriptor describes how a block transfer should be carried out by the DMAC, and it must remain in SRAM. For further details on the transfer descriptor refer to Transfer Descriptors.

The figure above shows several block transfers linked together, which are called linked descriptors. For further information about linked descriptors, refer to Linked Descriptors.

A DMA transfer is initiated by an incoming transfer trigger on one of the DMA channels. This trigger can be configured to be either a software trigger, an event trigger, or one of the dedicated peripheral triggers. The transfer trigger will result in a DMA transfer request from the specific channel to the arbiter. If there are several DMA channels with pending transfer requests, the arbiter chooses which channel is granted access to become the active channel. The DMA channel granted access as the active channel will carry out the transaction as configured in the transfer descriptor. A current transaction can be interrupted by a higher prioritized channel after each burst transfer, but will resume the block transfer when the according DMA channel is granted access as the active channel again.

For each beat transfer, an optional output event can be generated. For each block transfer, optional interrupts and an optional output event can be generated. When a transaction is completed, dependent of the configuration, the DMA channel will either be suspended or disabled.

25.6.1.2 CRC

The internal CRC engine supports two commonly used CRC polynomials: CRC-16 (CRC-CCITT) and CRC-32 (IEEE 802.3). It can be used on a selectable DMA channel, or on the I/O interface. Refer to CRC Operation for details.
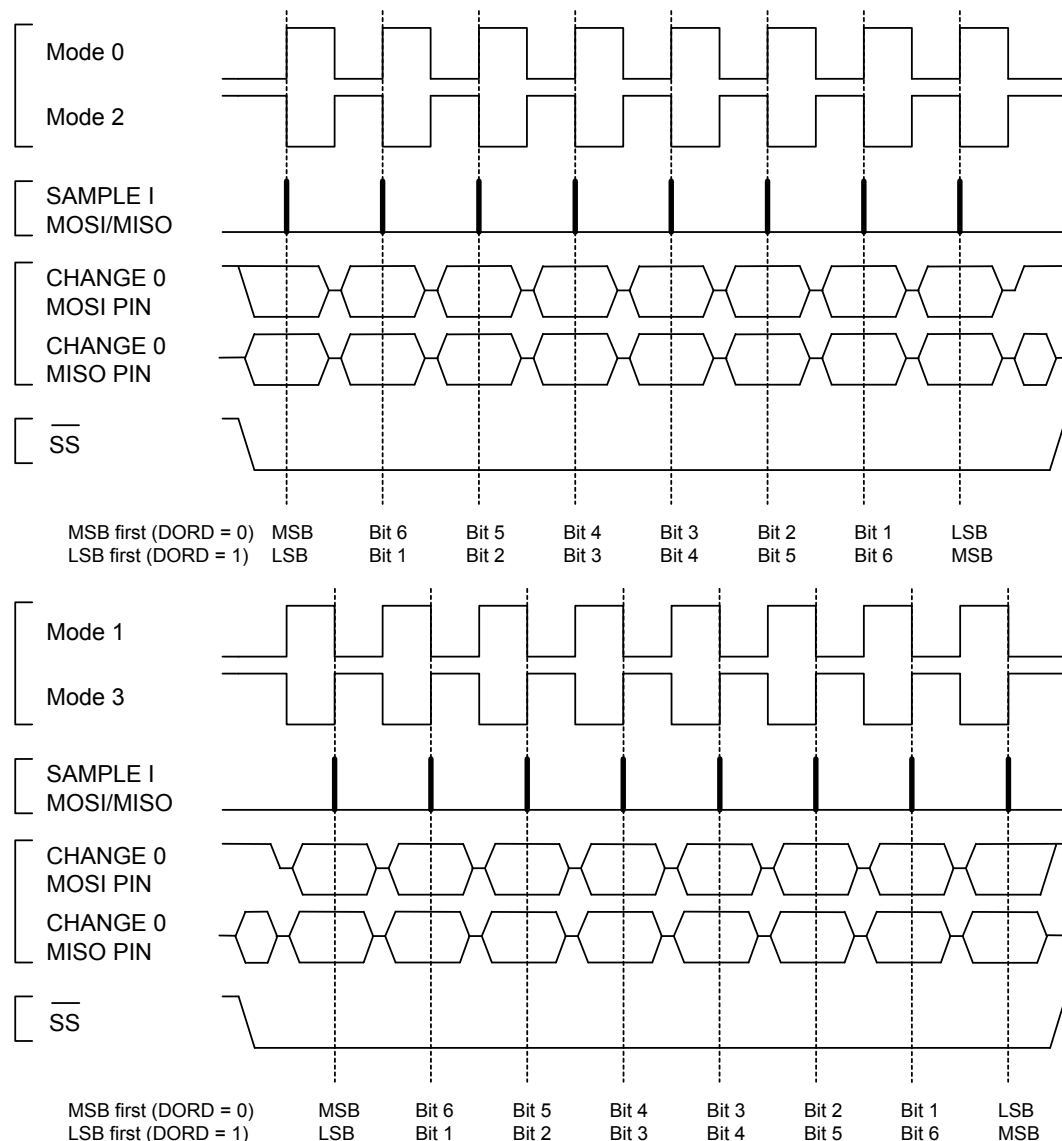
25.6.2 Basic Operation

25.6.2.1 Initialization

The following DMAC registers are enable-protected, meaning that they can only be written when the DMAC is disabled (CTRL.DMAENABLE=0):

- Descriptor Base Memory Address register (BASEADDR)
- Write-Back Memory Base Address register (WRBADDR)

opefort

Bit 0 – RF0N: Rx FIFO 0 New Message

Value	Description
0	No new message written to Rx FIFO 0.
1	New message written to Rx FIFO 0.

34.8.17 Interrupt Enable

The settings in the Interrupt Enable register determine which status changes in the Interrupt Register will be signalled on an interrupt line.

Name: IE
Offset: 0x54 [ID-0000a4bb]
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
			ARAE	PEDE	PEAE	WDIE	BOE	EWE
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	EPE	ELOE	BEUE	BECE	DRXE	TOOE	MRAFE	TSWE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TEFLE	TEFFE	TEFWE	TEFNE	TFEE	TCFE	TCE	HPME
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RF1LE	RF1FE	RF1WE	RF1NE	RF0LE	RF0FE	RF0WE	RF0NE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 29 – ARAE: Access to Reserved Address Interrupt Enable

Value	Description
0	Interrupt disabled.
1	Interrupt enabled.

Bit 28 – PEDE: Protocol Error in Data Phase Interrupt Enable

Value	Description
0	Interrupt disabled.
1	Interrupt enabled.

Bit 27 – PEAE: Protocol Error in Arbitration Phase Interrupt Enable

Value	Description
0	Interrupt disabled.
1	Interrupt enabled.

Bit 17 – MRAFE: Message RAM Access Failure Interrupt Enable

Value	Description
0	Interrupt disabled.
1	Interrupt enabled.

Bit 16 – TSWE: Timestamp Wraparound Interrupt Enable

Value	Description
0	Interrupt disabled.
1	Interrupt enabled.

Bit 15 – TEFLE: Tx Event FIFO Event Lost Interrupt Enable

Value	Description
0	Interrupt disabled.
1	Interrupt enabled.

Bit 14 – TEFFE: Tx Event FIFO Full Interrupt Enable

Value	Description
0	Interrupt disabled.
1	Interrupt enabled.

Bit 13 – TEFWE: Tx Event FIFO Watermark Reached Interrupt Enable

Value	Description
0	Interrupt disabled.
1	Interrupt enabled.

Bit 12 – TEFNE: Tx Event FIFO New Entry Interrupt Enable

Value	Description
0	Interrupt disabled.
1	Interrupt enabled.

Bit 11 – TFEE: Tx FIFO Empty Interrupt Enable

Value	Description
0	Interrupt disabled.
1	Interrupt enabled.

Bit 10 – TCFE: Transmission Cancellation Finished Interrupt Enable

Value	Description
0	Interrupt disabled.
1	Interrupt enabled.

Bit 9 – TCE: Transmission Completed Interrupt Enable

Bit	31	30	29	28	27	26	25	24
	TIEn	TIEn	TIEn	TIEn	TIEn	TIEn	TIEn	TIEn
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	TIEn	TIEn	TIEn	TIEn	TIEn	TIEn	TIEn	TIEn
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TIEn	TIEn	TIEn	TIEn	TIEn	TIEn	TIEn	TIEn
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TIEn	TIEn	TIEn	TIEn	TIEn	TIEn	TIEn	TIEn
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – TIEn: Transmission Interrupt Enable
Each Tx Buffer has its own Transmission Interrupt Enable bit.

Value	Description
0	Transmission interrupt disabled.
1	Transmission interrupt enabled.

34.8.44 Tx Buffer Cancellation Finished Interrupt Enable

Name: TXBCIE
Offset: 0xE4 [ID-0000a4bb]
Reset: 0x00000000
Property: -

Bit	7	6	5	4	3	2	1	0
				MCx			ERR	OVF
Access				R/W			R/W	R/W
Reset				0			0	0

Bit 4 – MCx: Match or Capture Channel x

This flag is set on a comparison match, or when the corresponding CCx register contains a valid capture value. This flag is set on the next CLK_TC_CNT cycle, and will generate an interrupt request if the corresponding Match or Capture Channel x Interrupt Enable bit in the Interrupt Enable Set register (INTENSET.MCx) is '1'.

Writing a '0' to one of these bits has no effect.

Writing a '1' to one of these bits will clear the corresponding Match or Capture Channel x interrupt flag

In capture operation, this flag is automatically cleared when CCx register is read.

Bit 1 – ERR: Error Interrupt Flag

This flag is set when a new capture occurs on a channel while the corresponding Match or Capture Channel x interrupt flag is set, in which case there is nowhere to store the new capture.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the Error interrupt flag.

Bit 0 – OVF: Overflow Interrupt Flag

This flag is set on the next CLK_TC_CNT cycle after an overflow condition occurs, and will generate an interrupt request if INTENCLR.OVF or INTENSET.OVF is '1'.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the Overflow interrupt flag.

35.7.3.8 Status

Name: STATUS
Offset: 0x0B
Reset: 0x01
Property: Read-Synchronized

Bit	7	6	5	4	3	2	1	0
				CCBUFVx	PERBUFV		SLAVE	STOP
Access				R/W	R/W		R	R
Reset				0	0		0	1

Bit 4 – CCBUFVx: Channel x Compare or Capture Buffer Valid

For a compare channel x, the bit x is set when a new value is written to the corresponding CCBUFx register.

The bit x is cleared by writing a '1' to it when CTRLB.LUPD is set, or it is cleared automatically by hardware on UPDATE condition.

For a capture channel x, the bit x is set when a valid capture value is stored in the CCBUFx register. The bit x is cleared automatically when the CCx register is read.

36. TCC – Timer/Counter for Control Applications

36.1 Overview

The device provides three instances of the Timer/Counter for Control applications (TCC) peripheral, TCC[2:0].

Each TCC instance consists of a counter, a prescaler, compare/capture channels and control logic. The counter can be set to count events or clock pulses. The counter together with the compare/capture channels can be configured to time stamp input events, allowing capture of frequency and pulse-width. It can also perform waveform generation such as frequency generation and pulse-width modulation.

Waveform extensions are featured for motor control, ballast, LED, H-bridge, power converters, and other types of power control applications. They allow for low- and high-side output with optional dead-time insertion. Waveform extensions can also generate a synchronized bit pattern across the waveform output pins. The fault options enable fault protection for safe and deterministic handling, disabling and/or shut down of external drivers.

Figure 36-1 shows all features in TCC.

Note: The TCC configurations, such as channel numbers and features, may be reduced for some of the TCC instances.

Related Links

TCC Configurations

36.2 Features

- Up to four compare/capture channels (CC) with:
  - Double buffered period setting
  - Double buffered compare or capture channel
  - Circular buffer on period and compare channel registers
- Waveform generation:
  - Frequency generation
  - Single-slope pulse-width modulation (PWM)
  - Dual-slope pulse-width modulation with half-cycle reload capability
- Input capture:
  - Event capture
  - Frequency capture
  - Pulse-width capture
- Waveform extensions:
  - Configurable distribution of compare channels outputs across port pins
  - Low- and high-side output with programmable dead-time insertion
  - Waveform swap option with double buffer support
  - Pattern generation with double buffer support
  - Dithering support
- Fault protection for safe disabling of drivers:
  - Two recoverable fault sources

Fault Inputs

The first two channel input events (TCCxMC0 and TCCxMC1) can be used as Fault A and Fault B inputs, respectively. Event system channels connected to these fault inputs must be configured as asynchronous. The TCC must work in a PWM mode.

Fault Filtering

There are three filters available for each input Fault A and Fault B. They are configured by the corresponding Recoverable Fault n Configuration registers (FCTRLA and FCTRLB). The three filters can either be used independently or in any combination.

Input Filtering By default, the event detection is asynchronous. When the event occurs, the fault system will immediately and asynchronously perform the selected fault action on the compare channel output, also in device power modes where the clock is not available. To avoid false fault detection on external events (e.g. due to a glitch on an I/O port) a digital filter can be enabled and configured by the Fault B Filter Value bits in the Fault n Configuration registers (FCTRLn.FILTERVAL). If the event width is less than FILTERVAL (in clock cycles), the event will be discarded. A valid event will be delayed by FILTERVAL clock cycles.

Fault Blanking This ignores any fault input for a certain time just after a selected waveform output edge. This can be used to prevent false fault triggering due to signal bouncing, as shown in the figure below. Blanking can be enabled by writing an edge triggering configuration to the Fault n Blanking Mode bits in the Recoverable Fault n Configuration register (FCTRLn.BLANK). The desired duration of the blanking must be written to the Fault n Blanking Time bits (FCTRLn.BLANKVAL).
The blanking time t_b is calculated by

$$t_b = \frac{1 + \text{BLANKVAL}}{f_{\text{GCLK\_TCCx\_PRESC}}}$$

Here, $f_{\text{GCLK\_TCCx\_PRESC}}$ is the frequency of the prescaled peripheral clock frequency $f_{\text{GCLK\_TCCx}}$.

The maximum blanking time (FCTRLn.BLANKVAL= 255) at $f_{\text{GCLK\_TCCx}}$=96MHz is 2.67µs (no prescaler) or 170µs (prescaling). For $f_{\text{GCLK\_TCCx}}$=1MHz, the maximum blanking time is either 170µs (no prescaling) or 10.9ms (prescaling enabled).

Figure 37-13. Edge Detector
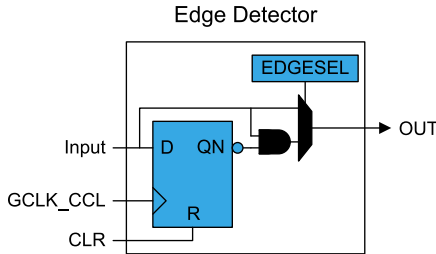

37.6.2.7 Sequential Logic

Each LUT pair can be connected to the internal sequential logic which can be configured to work as D flip flop, JK flip flop, gated D-latch or RS-latch by writing the Sequential Selection bits on the corresponding Sequential Control x register (SEQCTRLx.SEQSEL). Before using sequential logic, the GCLK_CCL clock and optionally each LUT filter or edge detector must be enabled.

Note: While configuring the sequential logic, the even LUT must be disabled. When configured the even LUT must be enabled.

Gated D Flip-Flop (DFF)
When the DFF is selected, the D-input is driven by the even LUT output (LUT0 and LUT2), and the G-input is driven by the odd LUT output (LUT1 and LUT3), as shown in Figure 37-14.

Figure 37-14. D Flip Flop
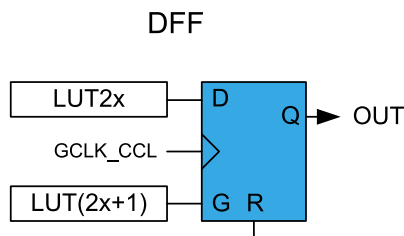
When the even LUT is disabled (LUTCTRL0.ENABLE=0 / LUTCTRL2.ENABLE=0), the flip-flop is asynchronously cleared. The reset command (R) is kept enabled for one APB clock cycle. In all other cases, the flip-flop output (OUT) is refreshed on rising edge of the GCLK_CCL, as shown in Table 37-2.

Table 37-2. DFF Characteristics

R	G	D	OUT
1	X	X	Clear
0	1	1	Set
		0	Clear
	0	X	Hold state (no change)

JK Flip-Flop (JK)
When this configuration is selected, the J-input is driven by the even LUT output (LUT0 and LUT2), and the K-input is driven by the odd LUT output (LUT1 and LUT3), as shown in Figure 37-15.

43.5.8 Register Access Protection

All registers with write-access are optionally write-protected by the Peripheral Access Controller (PAC), except the following registers:

- Control B (CTRLB) register
- Interrupt Flag Status and Clear (INTFLAG) register

Write-protection is denoted by the PAC Write-Protection property in the register description.

Write-protection does not apply to accesses through an external debugger. Refer to the Peripheral Access Controller chapter for details.

43.5.9 Calibration

The GAIN, OFFSET, FCAL, and TCAL calibration values from the production test must be loaded from the NVM Temperature Calibration Area into the TSENS Gain register (GAIN), Offset register (OFFSET) and Calibration register (CAL) by software to achieve specified accuracy.

Related Links

NVM Software Calibration Area Mapping
Temperature Sensor Characteristics

43.6 Functional Description

43.6.1 Principle of Operation

The TSENS accurately measures the operating temperature of the device by comparing the difference in two temperature dependent frequencies to a known frequency. The frequency of the temperature dependent oscillator (TOSC) is measured twice: first with the min configuration and next with the max configuration. The number of periods of GCLK_TSENS used for the measurement is defined by the GAIN register. The width of the resulting pulse is measured using a counter clocked by GCLK_TSENS in the up direction for the 1st phase and in the down 2nd phase.

The resulting signed value is proportional to the temperature and is corrected for offset by the contents of the OFFSET register.

$$\text{VALUE} = \text{OFFSET} + \text{GAIN} \times \left(\frac{f_{\text{TOSCMIN}}}{f_{\text{GCLK}}} + - \frac{f_{\text{TOSCMAX}}}{f_{\text{GCLK}}} \right)$$

Note:

- The values of GAIN and OFFSET are factory programmed to give a specific temperature slope when using the undivided internal 48MHz oscillator (OSC48M) as the GCLK_TSENS source. Other frequencies/sources may be used, but the GAIN setting and/or expected slope will need to be scaled accordingly.
- The calibration value should be copied and written into the GAIN and OFFSET registers to get the specified accuracy.

Related Links

VALUE

43.6.2 Basic Operation

43.6.2.1 Initialization

The generic clocks (GCLK_TSENS) should be configured and enabled. Refer to the Generic Clock Controller chapter for details.

Optional write-protection by the Peripheral Access Controller (PAC) is denoted by the "PAC Write-Protection" property in each individual register description.

Some registers require synchronization when read and/or written. Synchronization is denoted by the "Read-Synchronized" and/or "Write-Synchronized" property in each individual register description.

Some registers are enable-protected, meaning they can only be written when the module is disabled. Enable-protection is denoted by the "Enable-Protected" property in each individual register description.

43.8.1 Control A

Name: CTRLA
Offset: 0x00 [ID-00001f13]
Reset: 0x00
Property: PAC Write-Protection, Write-Synchronized (ENABLE, SWRST)

Bit	7	6	5	4	3	2	1	0
		RUNSTDBY					ENABLE	SWRST
Access		R/W					R/W	R/W
Reset		0					0	0

Bit 6 – RUNSTDBY: Run in Standby
This bit controls how the TSENS behaves during standby sleep mode:

This bit is not synchronized.

Value	Description
0	The TSENS is halted during standby sleep mode.
1	The TSENS is not stopped in standby sleep mode. If CTRLC.FREERUN is zero, the TSENS will be running when a peripheral is requesting it. If CTRLC.FREERUN is one, the TSENS will always be running in standby sleep mode.

Bit 1 – ENABLE: Enable
Due to synchronization there is delay from writing CTRLA.ENABLE until the peripheral is enabled/disabled. The value written to CTRLA.ENABLE will read back immediately and the ENABLE bit in the Synchronization Busy register (SYNCBUSY.ENABLE) will be set. SYNCBUSY.ENABLE will be cleared when the operation is complete.

This bit is not enable-protected.

Value	Description
0	The peripheral is disabled.
1	The peripheral is enabled.

Bit 0 – SWRST: Software Reset
Writing a zero to this bit has no effect.

Writing a one to this bit resets all registers in the TSENS, except GAIN, OFFSET, CAL and DBGCTRL, to their initial state, and the TSENS will be disabled.

Writing a one to CTRLA.SWRST will always take precedence, meaning that all other writes in the same write-operation will be discarded.

49.5 External Reset Circuit

The external Reset circuit is connected to the $\overline{RESET}$ pin when the external Reset function is used. The circuit is not necessary when the $\overline{RESET}$ pin is not driven LOW externally by the application circuitry.

The reset switch can also be removed, if a manual reset is not desired. The $\overline{RESET}$ pin itself has an internal pull-up resistor, hence it is optional to add any external pull-up resistor.

Figure 49-5. External Reset Circuit Schematic
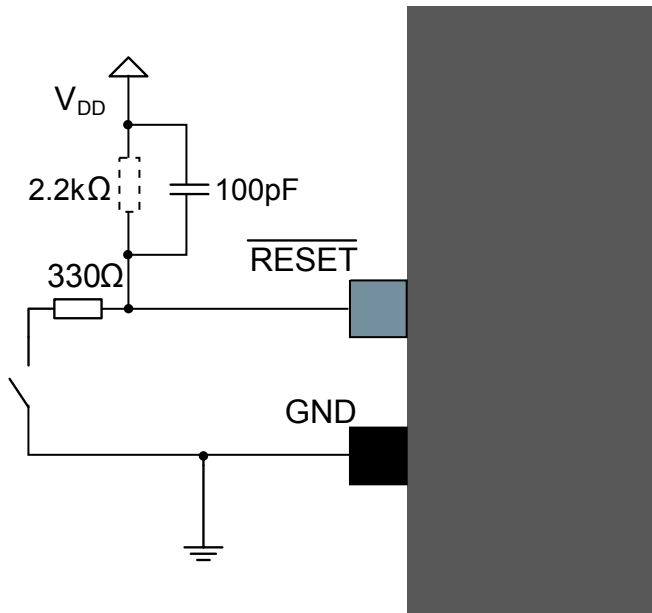
A pull-up resistor makes sure that the reset does not go low and unintentionally causing a device reset. An additional resistor has been added in series with the switch to safely discharge the filtering capacitor, i.e. preventing a current surge when shorting the filtering capacitor which again can cause a noise spike that can have a negative effect on the system.

Table 49-3. Reset Circuit Connections

Signal Name	Recommended Pin Connection	Description
$\overline{RESET}$	Reset low level threshold voltage V_{DDIO} = 2.7V - 5.5V: Below 0.3 * V_{DDIO} Decoupling/filter capacitor 100 pF[1] Pull-up resistor 2.2 kΩ[1][2] Resistor in series with the switch 330Ω[1]	Reset pin

1. These values are only given as a typical example.
2. The SAM C20/C21 features an internal pull-up resistor on the $\overline{RESET}$ pin; therefore, an external pull-up is optional.

49.6 Unused or Unconnected Pins

Unused or unconnected pins (unless marked as NC where applicable) should not be left unconnected and floating. Floating pins will add to the overall power consumption of the device. To prevent this one should always draw the pin voltage towards a given level, either VDD or GND, through a pull up/down