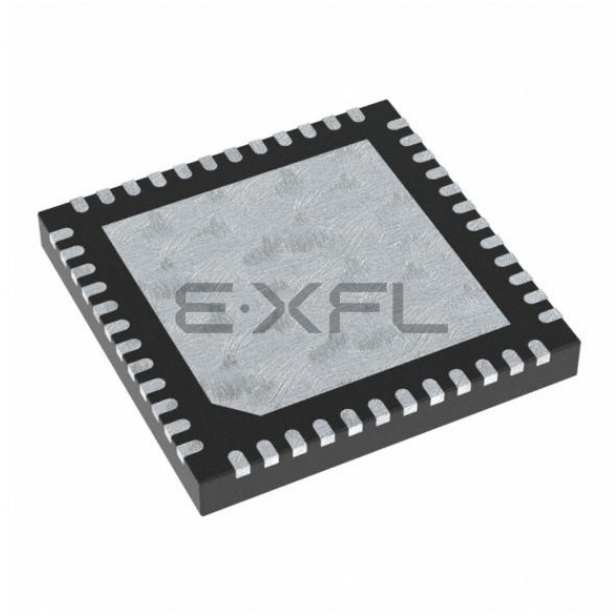

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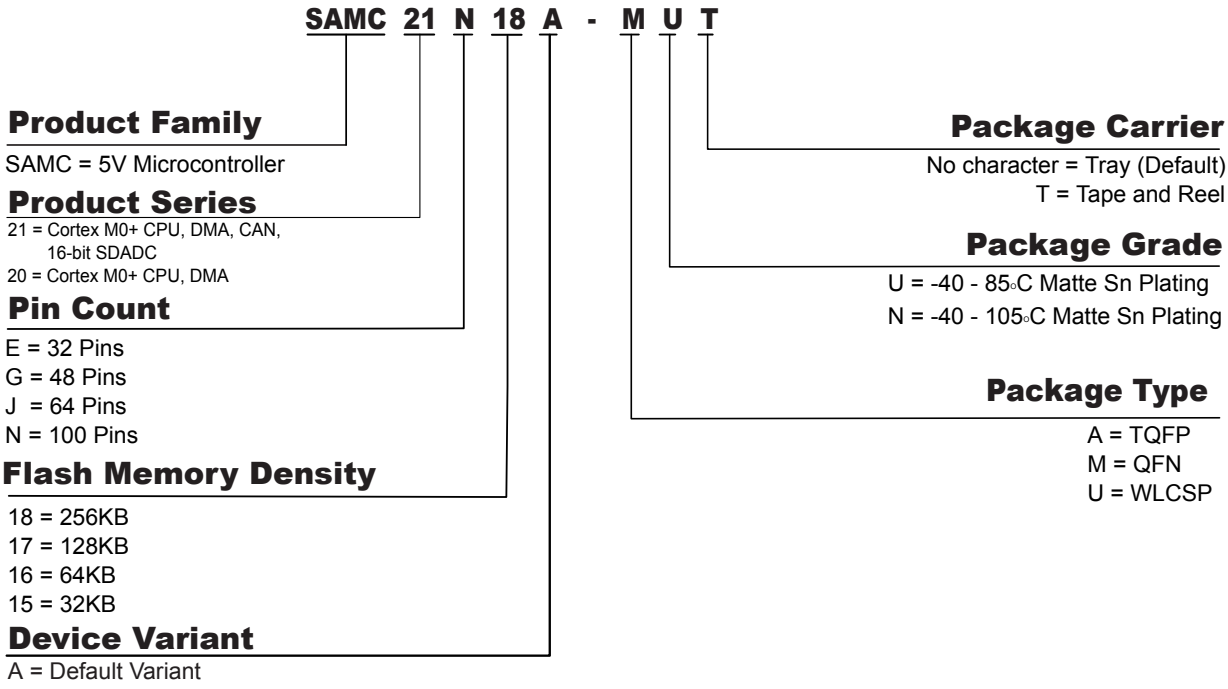
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, WDT
Number of I/O	38
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 14x12b, 2x16b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamc21g18a-mut

2. Ordering Information



Note: Not all combinations are valid. The available ordering numbers are listed in the Configuration Summary.

Table 10-4. Interrupt Line Mapping, SAM C20

Peripheral Source	NVIC Line
EIC NMI – External Interrupt Controller	NMI
PM – Power Manager MCLK - Main Clock OSCCTRL - Oscillators Controller OSC32KCTRL - 32kHz Oscillators Controller SUPC - Supply Controller PAC - Protection Access Controller	0
WDT – Watchdog Timer	1
RTC – Real Time Clock	2
EIC – External Interrupt Controller	3
FREQM – Frequency Meter	4
Reserved	5
NVMCTRL – Non-Volatile Memory Controller	6
DMAC - Direct Memory Access Controller	7
EVSYS – Event System	8
SERCOM0 – Serial Communication Controller 0 SERCOM6 – Serial Communication Controller 6	9
SERCOM1 – Serial Communication Controller 1 SERCOM7 – Serial Communication Controller 7	10
SERCOM2 – Serial Communication Controller 2	11
SERCOM3 – Serial Communication Controller 3	12
SERCOM4 – Serial Communication Controller 4	13
SERCOM5 – Serial Communication Controller 5	14
Reserved	15
Reserved	16
TCC0 – Timer Counter for Control 0	17
TCC1 – Timer Counter for Control 1	18
TCC2 – Timer Counter for Control 2	19
TC0 – Timer Counter 0 TC5 – Timer Counter 5	20
TC1 – Timer Counter 1	21

11.7.7 Peripheral Interrupt Flag Status and Clear B

This flag is cleared by writing a '1' to the flag.

This flag is set when a Peripheral Access Error occurs while accessing the peripheral associated with the respective INTFLAGB bit, and will generate an interrupt request if INTENCLR/SET.ERR is '1'.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the corresponding INTFLAGB interrupt flag.

Name: INTFLAGB
Offset: 0x18 [ID-00000a18]
Reset: 0x000000
Property: –

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				MTB	DMAC	NVMCTRL	DSU	PORT
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit 4 – MTB: Interrupt Flag for MTB

Bit 3 – DMAC: Interrupt Flag for DMAC

Bit 2 – NVMCTRL: Interrupt Flag for NVMCTRL

Bit 1 – DSU: Interrupt Flag for DSU

Bit 0 – PORT: Interrupt Flag for PORT

11.7.8 Peripheral Interrupt Flag Status and Clear C

This flag is cleared by writing a one to the flag.

This flag is set when a Peripheral Access Error occurs while accessing the peripheral associated with the respective INTFLAGC bit, and will generate an interrupt request if INTENCLR/SET.ERR is one.

Writing a zero to this bit has no effect.

Name: STATUSA
Offset: 0x34 [ID-00000a18]
Reset: 0x000000
Property: –

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
				TSENS	FREQM	EIC	RTC	WDT
Access				R	R	R	R	R
Reset				0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	GCLK	SUPC	OSC32KCTRL	OSCCTRL	RSTC	MCLK	PM	PAC
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit 12 – TSENS: Peripheral TSENS Write Protection Status

Bit 11 – FREQM: Peripheral FREQM Write Protection Status

Bit 10 – EIC: Peripheral EIC Write Protection Status

Bit 9 – RTC: Peripheral RTC Write Protection Status

Bit 8 – WDT: Peripheral WDT Write Protection Status

Bit 7 – GCLK: Peripheral GCLK Write Protection Status

Bit 6 – SUPC: Peripheral SUPC Write Protection Status

Bit 5 – OSC32KCTRL: Peripheral OSC32KCTRL Write Protection Status

Bit 4 – OSCCTRL: Peripheral OSCCTRL Write Protection Status

Bit 3 – RSTC: Peripheral RSTC Write Protection Status

Bit 2 – MCLK: Peripheral MCLK Write Protection Status

Bit 1 – PM: Peripheral PM Write Protection Status

Bit 0 – PAC: Peripheral PAC Write Protection Status

18. RSTC – Reset Controller

18.1 Overview

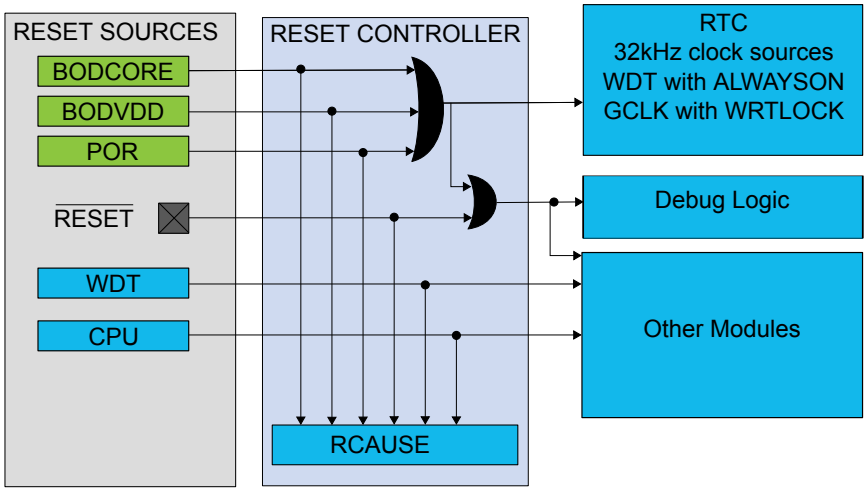
The Reset Controller (RSTC) manages the reset of the microcontroller. It issues a microcontroller reset, sets the device to its initial state and allows the reset source to be identified by software.

18.2 Features

- Reset the microcontroller and set it to an initial state according to the reset source
- Reset cause register for reading the reset source from the application code
- Multiple reset sources
  - Power supply reset sources: POR, BODCORE, BODVDD
  - User reset sources: External reset ($\overline{\text{RESET}}$), Watchdog reset, and System Reset Request

18.3 Block Diagram

Figure 18-1. Reset System



18.4 Signal Description

Signal Name	Type	Description
$\overline{\text{RESET}}$	Digital input	External reset

One signal can be mapped on several pins.

Related Links

I/O Multiplexing and Considerations

18.5 Product Dependencies

In order to use this peripheral, other parts of the system must be configured correctly, as described below.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					DPLLLDRTO	DPLLLTO	DPLLLCKF	DPLLLCKR
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
				OSC48MRDY			CLKFAIL	XOSCRDY
Access				R/W			R/W	R/W
Reset				0			0	0

Bit 11 – DPLLLDRTO: DPLL Loop Divider Ratio Update Complete
This flag is cleared by writing '1' to it.

This flag is set on 0-to-1 transition of the DPLL Loop Divider Ratio Update Complete bit in the Status register (STATUS.DPLLLDRTO) and will generate an interrupt request if INTENSET.DPLLLDRTO is '1'.

Writing '0' to this bit has no effect.

Writing '1' to this bit clears the DPLL Loop Divider Ratio Update Complete interrupt flag.

Bit 10 – DPLLLTO: DPLL Lock Timeout
This flag is cleared by writing '1' to it.

This flag is set on 0-to-1 transition of the DPLL Lock Timeout bit in the Status register (STATUS.DPLLLTO) and will generate an interrupt request if INTENSET.DPLLLTO is '1'.

Writing '0' to this bit has no effect.

Writing '1' to this bit clears the DPLL Lock Timeout interrupt flag.

Bit 9 – DPLLLCKF: DPLL Lock Fall
This flag is cleared by writing '1' to it.

This flag is set on 0-to-1 transition of the DPLL Lock Fall bit in the Status register (STATUS.DPLLLCKF) and will generate an interrupt request if INTENSET.DPLLLCKF is '1'.

Writing '0' to this bit has no effect.

Writing '1' to this bit clears the DPLL Lock Fall interrupt flag.

Bit 8 – DPLLLCKR: DPLL Lock Rise
This flag is cleared by writing '1' to it.

This flag is set on 0-to-1 transition of the DPLL Lock Rise bit in the Status register (STATUS.DPLLLCKR) and will generate an interrupt request if INTENSET.DPLLLCKR is '1'.

Writing '0' to this bit has no effect.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
						CLKFAIL	OSC32KRDY	XOSC32KRDY
Access						R/W	R/W	R/W
Reset						0	0	0

Bit 2 – CLKFAIL: XOSC32K Clock Failure Detection
This flag is cleared by writing a '1' to it.

This flag is set on a zero-to-one transition of the XOSC32K Clock Failure Detection bit in the Status register (STATUS.CLKFAIL) and will generate an interrupt request if INTENSET.CLKFAIL is '1'.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the XOSC32K Clock Failure Detection flag.

Bit 1 – OSC32KRDY: OSC32K Ready
This flag is cleared by writing a '1' to it.

This flag is set by a zero-to-one transition of the OSC32K Ready bit in the Status register (STATUS.OSC32KRDY), and will generate an interrupt request if INTENSET.OSC32KRDY=1.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the OSC32K Ready interrupt flag.

Bit 0 – XOSC32KRDY: XOSC32K Ready
This flag is cleared by writing a '1' to it.

This flag is set by a zero-to-one transition of the XOSC32K Ready bit in the Status register (STATUS.XOSC32KRDY), and will generate an interrupt request if INTENSET.XOSC32KRDY=1.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the XOSC32K Ready interrupt flag.

21.8.4 Status

Name: SYNCBUSY
Offset: 0x04
Reset: 0x00000000
Property: –

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
							ENABLE	SWRST
Access							R	R
Reset							0	0

Bit 1 – ENABLE: Enable Synchronization Busy Status

Value	Description
0	Write synchronization for CTRLA.ENABLE bit is complete.
1	Write synchronization for CTRLA.ENABLE bit is ongoing.

Bit 0 – SWRST: Software Reset Synchronization Busy Status

Value	Description
0	Write synchronization for CTRLA.SWRST bit is complete.
1	Write synchronization for CTRLA.SWRST bit is ongoing.

26.8.5 Event Control

Name: EVCTRL
Offset: 0x08
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected

Value	Description
0	The PMUXn registers of the selected pins will not be updated.
1	The PMUXn registers of the selected pins will be updated.

Bits 27:24 – PMUX[3:0]: Peripheral Multiplexing
These bits determine the new value written to the Peripheral Multiplexing register (PMUXn) for all pins selected by the WRCONFIG.PINMASK and WRCONFIG.HWSEL bits, when the WRCONFIG.WRPMUX bit is set.

These bits will always read as zero.

Bit 22 – DRVSTR: Output Driver Strength Selection
This bit determines the new value written to PINCFGy.DRVSTR for all pins selected by the WRCONFIG.PINMASK and WRCONFIG.HWSEL bits, when the WRCONFIG.WRPINCFG bit is set.

This bit will always read as zero.

Bit 18 – PULLEN: Pull Enable
This bit determines the new value written to PINCFGy.PULLEN for all pins selected by the WRCONFIG.PINMASK and WRCONFIG.HWSEL bits, when the WRCONFIG.WRPINCFG bit is set.

This bit will always read as zero.

Bit 17 – INEN: Input Enable
This bit determines the new value written to PINCFGy.INEN for all pins selected by the WRCONFIG.PINMASK and WRCONFIG.HWSEL bits, when the WRCONFIG.WRPINCFG bit is set.

This bit will always read as zero.

Bit 16 – PMUXEN: Peripheral Multiplexer Enable
This bit determines the new value written to PINCFGy.PMUXEN for all pins selected by the WRCONFIG.PINMASK and WRCONFIG.HWSEL bits, when the WRCONFIG.WRPINCFG bit is set.

This bit will always read as zero.

Bits 15:0 – PINMASK[15:0]: Pin Mask for Multiple Pin Configuration
These bits select the pins to be configured within the half-word group selected by the WRCONFIG.HWSEL bit.

These bits will always read as zero.

Value	Description
0	The configuration of the corresponding I/O pin in the half-word group will be left unchanged.
1	The configuration of the corresponding I/O pin in the half-word PORT group will be updated.

28.9.12 Event Input Control

Tip: The I/O pins are assembled in pin groups (”PORT groups”) with up to 32 pins. Group 0 consists of the PA pins, group 1 is for the PB pins, etc. Each pin group has its own PORT registers. For example, the register address offset for the Data Direction (DIR) register for group 0 (PA00 to PA31) is 0x00, and the register address offset for the DIR register for group 1 (PB00 to PB31) is 0x80.

29.6.2.9 The Overrun Channel n Interrupt

The Overrun Channel n interrupt flag in the Interrupt Flag Status and Clear register (INTFLAG.OVRn) will be set, and the optional interrupt will be generated in the following cases:

- One or more event users on channel n is not ready when there is a new event.
- An event occurs when the previous event on channel m has not been handled by all event users connected to that channel.

The flag will only be set when using resynchronized paths. In the case of asynchronous path, the INTFLAG.OVRn is always read as zero.

29.6.2.10 The Event Detected Channel n Interrupt

The Event Detected Channel n interrupt flag in the Interrupt Flag Status and Clear register (INTFLAG.EVDn) is set when an event coming from the event generator configured on channel n is detected.

The flag will only be set when using a resynchronized path. In the case of asynchronous path, the INTFLAG.EVDn is always zero.

29.6.2.11 Channel Status

The Channel Status register (CHSTATUS) shows the status of the channels when using a synchronous or resynchronized path. There are two different status bits in CHSTATUS for each of the available channels:

- The CHSTATUS.CHBUSYn bit will be set when an event on the corresponding channel n has not been handled by all event users connected to that channel.
- The CHSTATUS.USRRDYn bit will be set when all event users connected to the corresponding channel are ready to handle incoming events on that channel.

29.6.2.12 Software Event

A software event can be initiated on a channel by setting the Channel n bit in the Software Event register (SWEVT.CHANNELn) to ‘1’. Then the software event can be serviced as any event generator; i.e., when the bit is set to ‘1’, an event will be generated on the respective channel.

29.6.3 Interrupts

The EVSYS has the following interrupt sources:

- Overrun Channel n interrupt (OVRn): for details, refer to The Overrun Channel n Interrupt.
- Event Detected Channel n interrupt (EVDn): for details, refer to The Event Detected Channel n Interrupt.

These interrupts events are asynchronous wake-up sources. See *Sleep Mode Controller*. Each interrupt source has an interrupt flag which is in the Interrupt Flag Status and Clear (INTFLAG) register. The flag is set when the interrupt is issued. Each interrupt event can be individually enabled by setting a ‘1’ to the corresponding bit in the Interrupt Enable Set (INTENSET) register, and disabled by setting a ‘1’ to the corresponding bit in the Interrupt Enable Clear (INTENCLR) register. An interrupt event is generated when the interrupt flag is set and the corresponding interrupt is enabled. The interrupt event works until the interrupt flag is cleared, the interrupt is disabled, or the Event System is reset. See INTFLAG for details on how to clear interrupt flags.

All interrupt events from the peripheral are ORed together on system level to generate one combined interrupt request to the NVIC. Refer to the *Nested Vector Interrupt Controller* for details. The event user must read the INTFLAG register to determine what the interrupt condition is.

Note that interrupts must be globally enabled for interrupt requests to be generated. Refer to *Nested Vector Interrupt Controller* for details.

Related Links

SFDE	INTENSET.RXS	INTENSET.RXC	Description
1	1	0	Start-of-frame detection enabled. RXS wakes up the device from all sleep modes.
1	1	1	Start-of-frame detection enabled. Both RXC and RXS wake up the device from all sleep modes.

Bit 8 – COLDEN: Collision Detection Enable
This bit enables collision detection.

This bit is not synchronized.

Value	Description
0	Collision detection is not enabled.
1	Collision detection is enabled.

Bit 6 – SBMODE: Stop Bit Mode
This bit selects the number of stop bits transmitted.

This bit is not synchronized.

Value	Description
0	One stop bit.
1	Two stop bits.

Bits 2:0 – CHSIZE[2:0]: Character Size
These bits select the number of bits in a character.

These bits are not synchronized.

CHSIZE[2:0]	Description
0x0	8 bits
0x1	9 bits
0x2-0x4	Reserved
0x5	5 bits
0x6	6 bits
0x7	7 bits

31.8.3 Control C

Name: CTRLC
Offset: 0x08
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected

33.6.2.4 I²C Master Operation

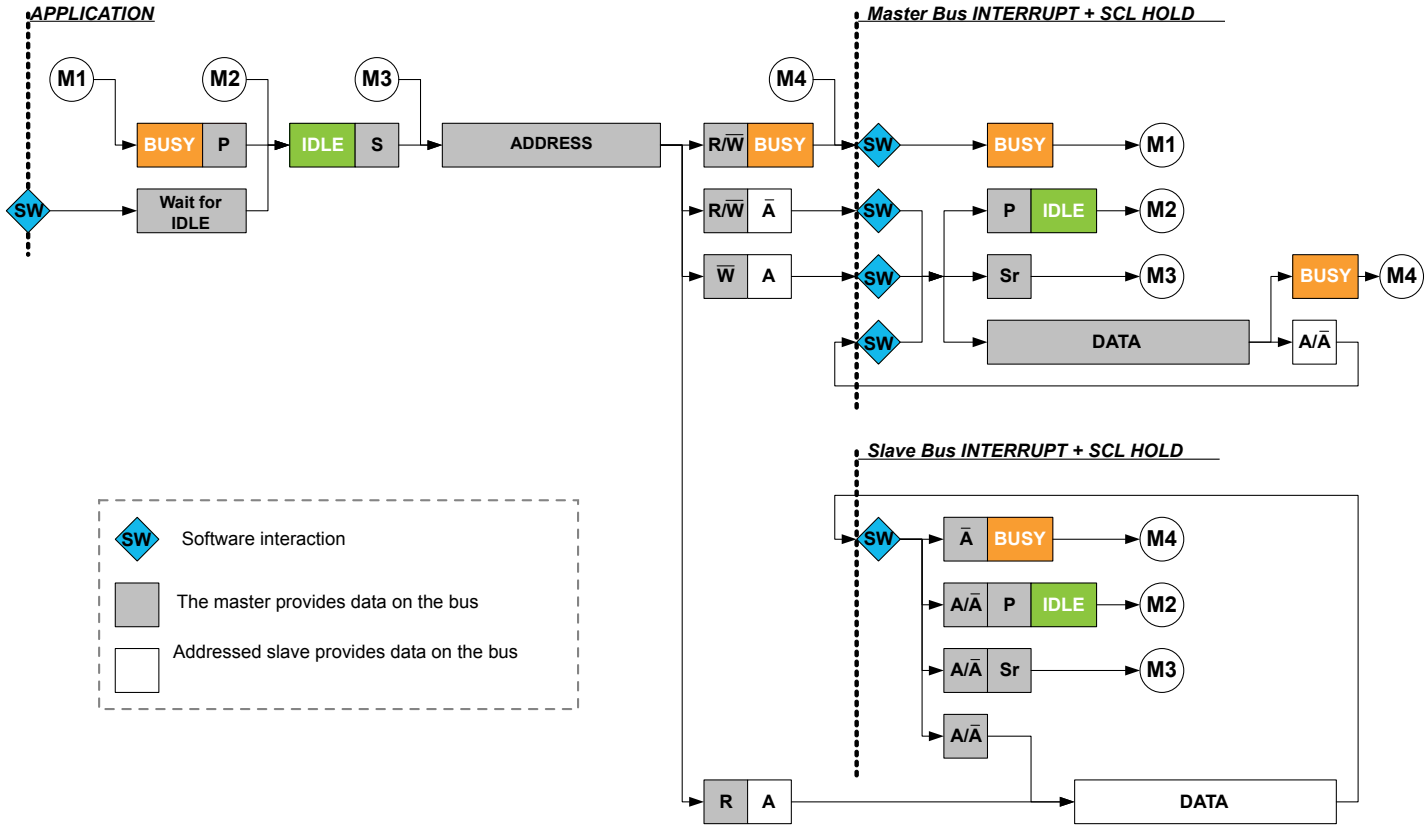
The I²C master is byte-oriented and interrupt based. The number of interrupts generated is kept at a minimum by automatic handling of most incidents. The software driver complexity and code size are reduced by auto-triggering of operations, and a special smart mode, which can be enabled by the Smart Mode Enable bit in the Control A register (CTRLA.SMEN).

The I²C master has two interrupt strategies.

When SCL Stretch Mode (CTRLA.SCLSM) is '0', SCL is stretched before or after the acknowledge bit . In this mode the I²C master operates according to Master Behavioral Diagram (SCLSM=0). The circles labelled "M*n*" (M1, M2..) indicate the nodes the bus logic can jump to, based on software or hardware interaction.

This diagram is used as reference for the description of the I²C master operation throughout the document.

Figure 33-5. I²C Master Behavioral Diagram (SCLSM=0)



In the second strategy (CTRLA.SCLSM=1), interrupts only occur after the ACK bit, as in Master Behavioral Diagram (SCLSM=1). This strategy can be used when it is not necessary to check DATA before acknowledging.

Note: I²C High-speed (*Hs*) mode requires CTRLA.SCLSM=1.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	FLST	FIDX[6:0]						
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	MSI[1:0]		BIDX[5:0]					
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit 15 – FLST: Filter List
Indicates the filter list of the matching filter element.

Value	Description
0	Standard Filter List.
1	Extended Filter List.

Bits 14:8 – FIDX[6:0]: Filter Index
Index of matching filter element. Range is 0 to SIDFC.LSS - 1 (standard) or XIDFC.LSE - 1 (extended).

Bits 7:6 – MSI[1:0]: Message Storage Indicator
This field defines the message storage information to a FIFO.

Value	Name	Description
0x0	NONE	No FIFO selected.
0x1	LOST	FIFO message lost.
0x2	FIFO0	Message stored in FIFO 0.
0x3	FIFO1	Message stored in FIFO 1.

Bits 5:0 – BIDX[5:0]: Buffer Index
Index of Rx FIFO element to which the message was stored. Only valid when MSI[1] = 1.

34.8.25 New Data 1

Name: NDAT1
Offset: 0x98 [ID-0000a4bb]
Reset: 0x00000000
Property: -

The table below shows the update counter and overflow event/interrupt generation conditions in different operation modes.

Table 35-3. Counter Update and Overflow Event/interrupt Conditions in TC

Name	Operation	TOP	Update	Output Waveform		OVFIF/Event	
				On Match	On Update	Up	Down
NFRQ	Normal Frequency	PER	TOP/ ZERO	Toggle	Stable	TOP	ZERO
MFRQ	Match Frequency	CC0	TOP/ ZERO	Toggle	Stable	TOP	ZERO
NPWM	Single-slope PWM	PER	TOP/ ZERO	See description above.		TOP	ZERO
MPWM	Single-slope PWM	CC0	TOP/ ZERO	Toggle	Toggle	TOP	ZERO

Related Links

PORT: IO Pin Controller

35.6.2.7 Double Buffering

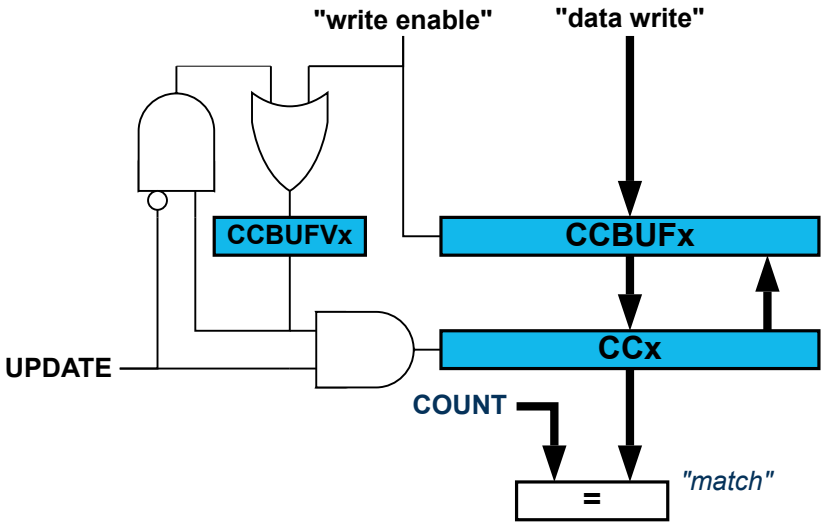
The Compare Channels (CCx) registers, and the Period (PER) register in 8-bit mode are double buffered. Each buffer register has a buffer valid bit (CCBUFVx or PERBUFV) in the STATUS register, which indicates that the buffer register contains a new valid value that can be copied into the corresponding register. As long as the respective buffer valid status flag (PERBUFV or CCBUFVx) are set to '1', related syncbusy bits are set (SYNCBUSY.PER or SYNCBUSY.CCx), a write to the respective PER/PERBUF or CCx/CCBUFx registers will generate a PAC error, and access to the respective PER or CCx register is invalid.

When the buffer valid flag bit in the STATUS register is '1' and the Lock Update bit in the CTRLB register is set to '0', (writing CTRLBCLR.LUPD to '1'), double buffering is enabled: the data from buffer registers will be copied into the corresponding register under hardware UPDATE conditions, then the buffer valid flags bit in the STATUS register are automatically cleared by hardware.

Note: The software update command (CTRLBSET.CMD=0x3) is acting independently of the LUPD value.

A compare register is double buffered as in the following figure.

Figure 35-7. Compare Channel Double Buffering



Name: CTRLA
Offset: 0x00
Reset: 0x00000000
Property: PAC Write-Protection, Write-Synchronized, Enable-Protected

Bit	31	30	29	28	27	26	25	24
				CAPTMODE1[1:0]			CAPTMODE0[1:0]	
Access				R/W	R/W		R/W	R/W
Reset				0	0		0	0

Bit	23	22	21	20	19	18	17	16
			COPEN1	COPEN0			CAPTEN1	CAPTEN0
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

Bit	15	14	13	12	11	10	9	8
					ALOCK	PRESCALER[2:0]		
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ONDEMAND	RUNSTDBY	PRESCSYNC[1:0]		MODE[1:0]		ENABLE	SWRST
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	W
Reset	0	0	0	0	0	0	0	0

Bits 28:27 – CAPTMODE1[1:0]: Capture mode Channel 1
These bits select the channel 1 capture mode.

Value	Name	Description
0x0	DEFAULT	Default capture
0x1	CAPTMIN	Minimum capture
0x2	CAPTMAX	Maximum capture
0x3		Reserved

Bits 25:24 – CAPTMODE0[1:0]: Capture mode Channel 0
These bits select the channel 0 capture mode.

Value	Name	Description
0x0	DEFAULT	Default capture
0x1	CAPTMIN	Minimum capture
0x2	CAPTMAX	Maximum capture
0x3		Reserved

Bits 20, 21 – COPENx: Capture On Pin x Enable
Bit x of COPEN[1:0] selects the trigger source for capture operation, either events or I/O pin input.

Value	Description
0	Event from Event System is selected as trigger source for capture operation on channel x.
1	I/O pin is selected as trigger source for capture operation on channel x.

Bit	31	30	29	28	27	26	25	24
	PERBUF[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PERBUF[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PERBUF[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PERBUF[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	1

Bits 31:0 – PERBUF[31:0]: Period Buffer Value
These bits hold the value of the period buffer register. The value is copied to PER register on UPDATE condition.

35.7.3.17 Channel x Compare Buffer Value, 32-bit Mode

Name: CCBUFx
Offset: 0x30 + x*0x04 [x=0..1]
Reset: 0x00000000
Property: Write-Synchronized

Name: DBGCTRL
Offset: 0x1E [ID-00002e48]
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
						FDDBD		DBGRUN
Access						R/W		R/W
Reset						0		0

Bit 2 – FDDBD: Fault Detection on Debug Break Detection
This bit is not affected by software reset and should not be changed by software while the TCC is enabled.

By default this bit is zero, and the on-chip debug (OCD) fault protection is disabled. When this bit is written to '1', OCD break request from the OCD system will trigger non-recoverable fault. When this bit is set, OCD fault protection is enabled and OCD break request from the OCD system will trigger a non-recoverable fault.

Value	Description
0	No faults are generated when TCC is halted in debug mode.
1	A non recoverable fault is generated and FAULTD flag is set when TCC is halted in debug mode.

Bit 0 – DBGRUN: Debug Running State
This bit is not affected by software reset and should not be changed by software while the TCC is enabled.

Value	Description
0	The TCC is halted when the device is halted in debug mode.
1	The TCC continues normal operation when the device is halted in debug mode.

36.8.9 Event Control

Name: EVCTRL
Offset: 0x20 [ID-00002e48]
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected

Bit	7	6	5	4	3	2	1	0
							START	FLUSH
Access							W	W
Reset							0	0

Bit 1 – START: ADC Start Conversion
Writing a '1' to this bit will start a conversion or sequence. The bit is cleared by hardware when the conversion has started. Writing a '1' to this bit when it is already set has no effect.

Writing a '0' to this bit will have no effect.

Bit 0 – FLUSH: ADC Conversion Flush
Writing a '1' to this bit will flush the ADC pipeline. A flush will restart the ADC clock on the next peripheral clock edge, and all conversions in progress will be aborted and lost. This bit is cleared until the ADC has been flushed.

After the flush, the ADC will resume where it left off; i.e., if a conversion was pending, the ADC will start a new conversion.

Writing this bit to '0' will have no effect.

38.8.18 Debug Control

Name: DBGCTRL
Offset: 0x1C [ID-0000120e]
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
								DBGRUN
Access								R/W
Reset								0

Bit 0 – DBGRUN: Debug Run
This bit is not reset by a software reset.

This bit controls the functionality when the CPU is halted by an external debugger.

This bit should be written only while a conversion is not ongoing.

Value	Description
0	The ADC is halted when the CPU is halted by an external debugger.
1	The ADC continues normal operation when the CPU is halted by an external debugger.

38.8.19 Synchronization Busy

Name: SYNCBUSY
Offset: 0x20 [ID-0000120e]
Reset: 0x0000
Property: -

2. External Anti-alias filter must be placed in front of each SDADC input to ensure high-frequency signals to not alias into measurement bandwidth. Use capacitors of X5R type for DC measurement. or capacitors of COG or NPO type for AC measurement.

Table 47-9. SDADC DC Performance: Differential Input Mode. Chopper ON(1)

Symbol	Parameters	Conditions (2)	Min	Typ	Max	Unit
INL	Integral Non Linearity	CLK_SDADC = 3MHz VREF = 1.2V	-	+/-2.9	+/-3.9	LSB
		CLK_SDADC = 3MHz INT VREF = 5.5V	-	+/-8.4	+/-9.3	
DNL	Differential Non Linearity	CLK_SDADC = 3MHz VREF = 1.2V	-	+/-1.5	+/-2.1	LSB
		CLK_SDADC = 3MHz INT VREF = 5.5V	-	+/-1.7	+/-2.3	
Eg	Gain Errors	CLK_SDADC = 3MHz VREF = 1.2V	-	+/-0.3	+/-1.9	%
		CLK_SDADC = 3MHz INT VREF = 5.5V	-	+/-0.3	+/-1.7	
TCg	Gain Drift	CLK_SDADC = 3MHz VREF = 1.2V	-0.9	3.9	17.5	ppm/°C
Off	Offset Error	CLK_SDADC = 3MHz VREF = 1.2V	-	+/-2.3	+/-3.7	mV
		CLK_SDADC = 3MHz INT VREF = 5.5V	-	+/-0.3	+/-2.4	
Tco	Offset Error Drift	CLK_SDADC = 3MHz VREF = 1.2V	-1.4	0.01	0.6	uV/°C

1. OSR=256

Table 47-10. SDADC DC Performance: Differential Input Mode. Chopper OFF(1)

Symbol	Parameters	Conditions (2)	Min	Typ	Max	Unit
INL	Integral Non Linearity	CLK_SDADC = 6MHz VREF = 1.2V	-	+/-5.5	+/-9.3	LSB
		CLK_SDADC = 6MHz INT VREF = 5.5V	-	+/-8.9	+/-10.1	
DNL	Differential Non Linearity	CLK_SDADC = 6MHz VREF = 1.2V	-	+/-2.8	+/-4.1	LSB
		CLK_SDADC = 6MHz INT VREF = 5.5V	-	+/-1.8	+/-3	
Eg	Gain Errors	CLK_SDADC = 6MHz VREF = 1.2V	-	+/-0.6	+/-2.1	%
		CLK_SDADC = 6MHz INT VREF = 5.5V	-	+/-0.3	+/-1.7	
TCg	Gain Drift	CLK_SDADC = 6MHz VREF = 1.2V	-19.7	2.2	20.9	ppm/°C
Off	Offset Error	CLK_SDADC = 6MHz VREF = 1.2V	-	+/-1.7	+/-14.3	mV
		CLK_SDADC = 6MHz INT VREF = 5.5V	-	+/-4.9	+/-13.2	
Tco	Offset Error Drift	CLK_SDADC = 6MHz VREF = 1.2V	-14	12.4	60	µV/°C
Input noise rms	AC Input noise rms	OSR = 256 VREF = 1.2V	-	19	20	
		OSR = 256 VREF = 5.5V	-	59	76	mVrms

1. OSR=256

Table 47-11. SDADC AC Performance: : Differential Input Mode(1)

Symbol	Parameters	Conditions (2)	Min	Typ	Max	Unit
ENOB	Effective Number Of Bits	Ext ref = 1.2V	12	15.3	15.4	dB
		Int Ref = 5.5V	12.9	13.1	14	
DR	Dynamic Range	Ext ref = 1.2V	90.5	92.4	93.2	dB
		Int Ref = 5.5V	83.0	95.6	97.0	
SNR	Signal to Noise Ratio	Ext ref = 1.2V	68.7	88.7	89	dB