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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, WDT
Number of I/O	52
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 20x12b, 3x16b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamc21j16a-aut

Pin	I/O Pin	Supply	A		B			B[1][2]			C	D	E	F	G	H	I
			EIC	REF	ADC0	ADC1	SDADC	AC	PTC	DAC	SERCOM	SERCOM-ALT	TC	TCC	COM	AC/GCLK	CCL
59	PC19	VDDIO	EXTINT[11]								SERCOM6/PAD[3]						
60	PC20	VDDIO	EXTINT[12]														CCL3/IN[9]
61	PC21	VDDIO	EXTINT[13]														CCL3/IN[10]
64	PB16	VDDIO	EXTINT[0]								SERCOM5/PAD[0]		TC6/WO[0]			GCLK_IO[2]	CCL3/IN[11]
65	PB17	VDDIO	EXTINT[1]								SERCOM5/PAD[1]		TC6/WO[1]			GCLK_IO[3]	CCL3/OUT[3]
66	PB18	VDDIO	EXTINT[2]								SERCOM5/PAD[2]	SERCOM3/PAD[2]				GCLK_IO[4]	
67	PB19	VDDIO	EXTINT[3]								SERCOM5/PAD[3]	SERCOM3/PAD[3]				GCLK_IO[5]	
68	PB20	VDDIO	EXTINT[4]								SERCOM3/PAD[0]	SERCOM2/PAD[0]				GCLK_IO[6]	
69	PB21	VDDIO	EXTINT[5]								SERCOM3/PAD[1]	SERCOM2/PAD[1]				GCLK_IO[7]	
70	PA20	VDDIO	EXTINT[4]						X[8]/Y[24]		SERCOM5/PAD[2]	SERCOM3/PAD[2]	TC7/WO[0]	TCC2/WO[0]		GCLK_IO[4]	
71	PA21	VDDIO	EXTINT[5]						X[9]/Y[25]		SERCOM5/PAD[3]	SERCOM3/PAD[3]	TC7/WO[1]	TCC2/WO[1]		GCLK_IO[5]	
72	PA22	VDDIO	EXTINT[6]						X[10]/Y[26]		SERCOM3/PAD[0]	SERCOM5/PAD[0]	TC4/WO[0]	TCC1/WO[0]	CAN0/TX	GCLK_IO[6]	CCL2/IN[6]
73	PA23	VDDIO	EXTINT[7]						X[11]/Y[27]		SERCOM3/PAD[1]	SERCOM5/PAD[1]	TC4/WO[1]	TCC1/WO[1]	CAN0/RX	GCLK_IO[7]	CCL2/IN[7]
74	PA24	VDDIO	EXTINT[12]								SERCOM3/PAD[2]	SERCOM5/PAD[2]	TC5/WO[0]	TCC2/WO[0]	CAN0/TX	CMP[2]	CCL2/IN[8]
75	PA25	VDDIO	EXTINT[13]								SERCOM3/PAD[3]	SERCOM5/PAD[3]	TC5/WO[1]	TCC2/WO[1]	CAN0/RX	CMP[3]	CCL2/OUT[2]
78	PB22	VDDIO	EXTINT[6]								SERCOM0/PAD[2]	SERCOM5/PAD[2]	TC7/WO[0]	TCC1/WO[2]		GCLK_IO[0]	CCL0/IN[0]
79	PB23	VDDIO	EXTINT[7]								SERCOM0/PAD[3]	SERCOM5/PAD[3]	TC7/WO[1]	TCC1/WO[3]		GCLK_IO[1]	CCL0/OUT[0]
80	PB24	VDDIO	EXTINT[8]								SERCOM0/PAD[0]	SERCOM4/PAD[0]				CMP[0]	
81	PB25	VDDIO	EXTINT[9]								SERCOM0/PAD[1]	SERCOM4/PAD[1]				CMP[1]	
82	PC24	VDDIO	EXTINT[0]								SERCOM0/PAD[2]	SERCOM4/PAD[2]					
83	PC25	VDDIO	EXTINT[1]								SERCOM0/PAD[3]	SERCOM4/PAD[3]					
84	PC26	VDDIO	EXTINT[2]														
85	PC27	VDDIO	EXTINT[3]									SERCOM1/PAD[0]					CCL1/IN[4]
86	PC28	VDDIO	EXTINT[4]									SERCOM1/PAD[1]					CCL1/IN[5]
87	PA27	VDDIN	EXTINT[15]													GCLK_IO[0]	
89	PA28	VDDIN	EXTINT[8]													GCLK_IO[0]	
93	PA30	VDDIN	EXTINT[10]									SERCOM1/PAD[2]	TC1/WO[0]		CORTEX_M0P/SWCLK	GCLK_IO[0]	CCL1/IN[3]
94	PA31	VDDIN	EXTINT[11]									SERCOM1/PAD[3]	TC1/WO[1]		CORTEX_M0P/SWDIO		CCL1/OUT[1]
95	PB30	VDDIN	EXTINT[14]								SERCOM1/PAD[0]	SERCOM5/PAD[0]	TC0/WO[0]			CMP[2]	
96	PB31	VDDIN	EXTINT[15]								SERCOM1/PAD[1]	SERCOM5/PAD[1]	TC0/WO[1]			CMP[3]	
97	PB00	VDDANA	EXTINT[0]			AIN[0]			Y[6]			SERCOM5/PAD[2]	TC7/WO[0]				CCL0/IN[1]
98	PB01	VDDANA	EXTINT[1]			AIN[1]			Y[7]			SERCOM5/PAD[3]	TC7/WO[1]				CCL0/IN[2]
99	PB02	VDDANA	EXTINT[2]			AIN[2]			Y[8]			SERCOM5/PAD[0]	TC6/WO[0]				CCL0/OUT[0]
100	PB03	VDDANA	EXTINT[3]			AIN[3]			Y[9]			SERCOM5/PAD[1]	TC6/WO[1]				

1. All analog pin functions are on peripheral function B. Peripheral function B must be selected to disable the digital control of the pin.
2. Only some pins can be used in SERCOM I2C mode. Refer to SERCOM I2C Pins.

Table 6-2. PORT Function Multiplexing for SAM C21 E/G/J

	Pin[1]		I/O Pin	Supply	A				B[2][3]				C	D	E	F	G	H	I
SAM C21E	SAM C21G	SAM C21J			EIC	REF	ADC0	ADC1	AC	PTC	DAC	SDADC	SERCOM[2][3][4]	SERCOM-ALT[4]	TC TCC	TCC	COM	AC/GCLK	CCL
1	1	1	PA00	VDDANA	EXTINT[0]									SERCOM1/PAD[0]	TCC2/WO[0]			CMP[2]	
2	2	2	PA01	VDDANA	EXTINT[1]									SERCOM1/PAD[1]	TCC2/WO[1]			CMP[3]	
3	3	3	PA02	VDDANA	EXTINT[2]		AIN[0]		AIN[4]	Y[0]	VOUT								
4	4	4	PA03	VDDANA	EXTINT[3]	ADC/ VREFA	AIN[1]		AIN[5]	Y[1]									
		5	PB04	VDDANA	EXTINT[4]			AIN[6]		Y[10]									
		6	PB05	VDDANA	EXTINT[5]			AIN[7]	AIN[6]	Y[11]									
		9	PB06	VDDANA	EXTINT[6]			AIN[8]	AIN[7]	Y[12]		INN[2]							CCL2/ IN[6]
		10	PB07	VDDANA	EXTINT[7]			AIN[9]		Y[13]		INP[2]							CCL2/ IN[7]
	7	11	PB08	VDDANA	EXTINT[8]		AIN[2]	AIN[4]		Y[14]		INN[1]		SERCOM4/ PAD[0]	TC0/WO[0]				CCL2/ IN[8]
	8	12	PB09	VDDANA	EXTINT[9]		AIN[3]	AIN[5]		Y[15]		INP[1]		SERCOM4/ PAD[1]	TC0WO[1]				CCL2/ OUT[2]
5	9	13	PA04	VDDANA	EXTINT[4]		AIN[4]		AIN[0]	Y[2]				SERCOM0/ PAD[0]	TCC0/WO[0]				CCL0/ IN[0]
6	10	14	PA05	VDDANA	EXTINT[5]		AIN[5]		AIN[1]	Y[3]				SERCOM0/ PAD[1]	TCC0/WO[1]				CCL0/ IN[1]
7	11	15	PA06	VDDANA	EXTINT[6]		AIN[6]		AIN[2]	Y[4]		INN[0]		SERCOM0/ PAD[2]	TCC1/WO[0]				CCL0/ IN[2]
8	12	16	PA07	VDDANA	EXTINT[7]		AIN[7]		AIN[3]	Y[5]		INP[0]		SERCOM0/ PAD[3]	TCC1/WO[1]				CCL0/ OUT[0]
11	13	17	PA08	VDDIO	NMI		AIN[8]	AIN[10]		X[0]/Y[16]			SERCOM0/ PAD[0]	SERCOM2/ PAD[0]	TCC0/WO[0]	TCC1/ WO[2]			CCL1/

	Pin[1]		I/O Pin	Supply	A			B[2][3]		C	D	E	F	G	H	I
SAM C20E	SAM C20G	SAM C20J			EIC	REF	ADC0	AC	PTC	SERCOM[2][3][4]	SERCOM-ALT[4]	TC TCC	TCC	COM	AC/GCLK	CCL
		25	PB12	VDDIO	EXTINT[12]				X[12]/Y[28]	SERCOM4/ PAD[0]		TC0/WO[0]	TCC0/ WO[6]		GCLK_IO[6]	
		26	PB13	VDDIO	EXTINT[13]				X[13]/Y[29]	SERCOM4/ PAD[1]		TC0/WO[1]	TCC0/ WO[7]		GCLK_IO[7]	
		27	PB14	VDDIO	EXTINT[14]				X[14]/Y[30]	SERCOM4/ PAD[2]		TC1/WO[0]			GCLK_IO[0]	CCL3/ IN[9]
		28	PB15	VDDIO	EXTINT[15]				X[15]/Y[31]	SERCOM4/ PAD[3]		TC1/WO[1]			GCLK_IO[1]	CCL3/ IN[10]
	21	29	PA12	VDDIO	EXTINT[12]					SERCOM2/ PAD[0]	SERCOM4/ PAD[0]	TCC2/WO[0]	TCC0/ WO[6]		AC/CMP[0]	
	22	30	PA13	VDDIO	EXTINT[13]					SERCOM2/ PAD[1]	SERCOM4/ PAD[1]	TCC2/WO[1]	TCC0/ WO[7]		AC/CMP[1]	
15	23	31	PA14	VDDIO	EXTINT[14]					SERCOM2/ PAD[2]	SERCOM4/ PAD[2]	TC4/WO[0]	TCC0/ WO[4]		GCLK_IO[0]	
16	24	32	PA15	VDDIO	EXTINT[15]					SERCOM2/ PAD[3]	SERCOM4/ PAD[3]	TC4/WO[1]	TCC0/ WO[5]		GCLK_IO[1]	
17	25	35	PA16	VDDIO	EXTINT[0]				X[4]/Y[20]	SERCOM1/ PAD[0]	SERCOM3/ PAD[0]	TCC2/WO[0]	TCC0/ WO[6]		GCLK_IO[2]	CCL0/ IN[0]
18	26	36	PA17	VDDIO	EXTINT[1]				X[5]/Y[21]	SERCOM1/ PAD[1]	SERCOM3/ PAD[1]	TCC2/WO[1]	TCC0/ WO[7]		GCLK_IO[3]	CCL0/ IN[1]
19	27	37	PA18	VDDIO	EXTINT[2]				X[6]/Y[22]	SERCOM1/ PAD[2]	SERCOM3/ PAD[2]	TC4/WO[0]	TCC0/ WO[2]		AC/CMP[0]	CCL0/ IN[2]
20	28	38	PA19	VDDIO	EXTINT[3]				X[7]/Y[23]	SERCOM1/ PAD[3]	SERCOM3/ PAD[3]	TC4/WO[1]	TCC0/ WO[3]		AC/CMP[1]	CCL0/ OUT[0]
		39	PB16	VDDIO	EXTINT[0]					SERCOM5/ PAD[0]		TC2/WO[0]	TCC0/ WO[4]		GCLK_IO[2]	CCL3/ IN[11]
		40	PB17	VDDIO	EXTINT[1]					SERCOM5/ PAD[1]		TC2/WO[1]	TCC0/ WO[5]		GCLK_IO[3]	CCL3/ OUT[3]
	29	41	PA20	VDDIO	EXTINT[4]				X[8]/Y[24]	SERCOM5/ PAD[2]	SERCOM3/ PAD[2]	TC3/WO[0]	TCC0/ WO[6]		GCLK_IO[4]	
	30	42	PA21	VDDIO	EXTINT[5]				X[9]/Y[25]	SERCOM5/ PAD[3]	SERCOM3/ PAD[3]	TC3/WO[1]	TCC0/ WO[7]		GCLK_IO[5]	
21	31	43	PA22	VDDIO	EXTINT[6]				X[10]/Y[26]	SERCOM3/ PAD[0]	SERCOM5/ PAD[0]	TC0/WO[0]	TCC0/ WO[4]		GCLK_IO[6]	CCL2/ IN[6]
22	32	44	PA23	VDDIO	EXTINT[7]				X[11]/Y[27]	SERCOM3/ PAD[1]	SERCOM5/ PAD[1]	TC0/WO[1]	TCC0/ WO[5]		GCLK_IO[7]	CCL2/ IN[7]
23	33	45	PA24	VDDIO	EXTINT[12]					SERCOM3/ PAD[2]	SERCOM5/ PAD[2]	TC1/WO[0]	TCC1/ WO[2]		AC/CMP[2]	CCL2/ IN[8]
24	34	46	PA25	VDDIO	EXTINT[13]					SERCOM3/ PAD[3]	SERCOM5/ PAD[3]	TC1/WO[1]	TCC1/ WO[3]		AC/CMP[3]	CCL2/ OUT[2]
	37	49	PB22	VDDIN	EXTINT[6]						SERCOM5/ PAD[2]	TC3/WO[0]			GCLK_IO[0]	CCL0/ IN[0]
	38	50	PB23	VDDIN	EXTINT[7]						SERCOM5/ PAD[3]	TC3/WO[1]			GCLK_IO[1]	CCL0/ OUT[0]
25	39	51	PA27	VDDIN	EXTINT[15]										GCLK_IO[0]	
27	41	53	PA28	VDDIN	EXTINT[8]										GCLK_IO[0]	
31	45	57	PA30	VDDIN	EXTINT[10]						SERCOM1/ PAD[2]	TCC1/WO[0]		CORTEX_M0P/ SWCLK	GCLK_IO[0]	CCL1/ IN[3]
32	46	58	PA31	VDDIN	EXTINT[11]						SERCOM1/ PAD[3]	TCC1/WO[1]		CORTEX_M0P/ SWDIO		CCL1/ OUT[1]
		59	PB30	VDDIN	EXTINT[14]						SERCOM5/ PAD[0]	TCC0/WO[0]	TCC1/ WO[2]		AC/CMP[2]	
		60	PB31	VDDIN	EXTINT[15]						SERCOM5/ PAD[1]	TCC0/WO[1]	TCC1/ WO[3]		AC/CMP[3]	
		61	PB00	VDDANA	EXTINT[0]				Y[6]		SERCOM5/ PAD[2]	TC3/WO[0]				CCL0/ IN[1]
		62	PB01	VDDANA	EXTINT[1]				Y[7]		SERCOM5/ PAD[3]	TC3/WO[1]				CCL0/ IN[2]
	47	63	PB02	VDDANA	EXTINT[2]				Y[8]		SERCOM5/ PAD[0]	TC2/WO[0]				CCL0/ OUT[0]
	48	64	PB03	VDDANA	EXTINT[3]				Y[9]		SERCOM5/ PAD[1]	TC2/WO[1]				

1. Use the SAM C21J pinout muxing for the WLCSP56 package.
2. All analog pin functions are on peripheral function B. Peripheral function B must be selected to disable the digital control of the pin.
3. Only some pins can be used in SERCOM I2C mode. Refer to SERCOM I2C Pins.
4. SERCOM4 and SERCOM5 are not supported on SAM C20E

Related Links

13.12 Register Summary

Offset	Name	Bit Pos.									
0x00	CTRL	7:0				CE	MBIST		CRC	SWRST
0x01	STATUSA	7:0				PERR	FAIL	BERR	CRSTEXT	DONE
0x02	STATUSB	7:0				HPE	DCCDx	DCCDx	DBGPRES	PROT
0x03	Reserved									
0x04	ADDR	7:0	ADDR[5:0]						AMOD[1:0]	
0x05		15:8	ADDR[13:6]							
0x06		23:16	ADDR[21:14]							
0x07		31:24	ADDR[29:22]							
0x08	LENGTH	7:0	LENGTH[5:0]							
0x09		15:8	LENGTH[13:6]							
0x0A		23:16	LENGTH[21:14]							
0x0B		31:24	LENGTH[29:22]							
0x0C	DATA	7:0	DATA[7:0]							
0x0D		15:8	DATA[15:8]							
0x0E		23:16	DATA[23:16]							
0x0F		31:24	DATA[31:24]							
0x10	DCC0	7:0	DATA[7:0]							
0x11		15:8	DATA[15:8]							
0x12		23:16	DATA[23:16]							
0x13		31:24	DATA[31:24]							
0x14	DCC1	7:0	DATA[7:0]							
0x15		15:8	DATA[15:8]							
0x16		23:16	DATA[23:16]							
0x17		31:24	DATA[31:24]							
0x18	DID	7:0	DEVSEL[7:0]							
0x19		15:8	DIE[3:0]				REVISION[3:0]			
0x1A		23:16	FAMILY[0:0]		SERIES[5:0]					
0x1B		31:24	PROCESSOR[3:0]				FAMILY[4:1]			
0x1C ... 0x0FFF	Reserved									
0x1000	ENTRY0	7:0							FMT	EPRES
0x1001		15:8	ADDOFF[3:0]							
0x1002		23:16	ADDOFF[11:4]							
0x1003		31:24	ADDOFF[19:12]							
0x1004	ENTRY1	7:0							FMT	EPRES
0x1005		15:8	ADDOFF[3:0]							
0x1006		23:16	ADDOFF[11:4]							
0x1007		31:24	ADDOFF[19:12]							
0x1008	END	7:0	END[7:0]							
0x1009		15:8	END[15:8]							
0x100A		23:16	END[23:16]							
0x100B		31:24	END[31:24]							
0x100C	Reserved									

Offset	Name	Bit Pos.								
0x0136		23:16								
0x0137		31:24								

16.8 Register Description

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16- and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly.

Some registers are optionally write-protected by the Peripheral Access Controller (PAC). Optional PAC write-protection is denoted by the "PAC Write-Protection" property in each individual register description. For details, refer to Register Access Protection.

Some registers are synchronized when read and/or written. Synchronization is denoted by the "Write-Synchronized" or the "Read-Synchronized" property in each individual register description. For details, refer to Synchronization.

16.8.1 Control A

Name: CTRLA
Offset: 0x00 [ID-000008c2]
Reset: 0x00
Property: PAC Write-Protection, Write-Synchronized

Bit	7	6	5	4	3	2	1	0
								SWRST
Access								R/W
Reset								0

Bit 0 – SWRST: Software Reset
Writing a zero to this bit has no effect.

Setting this bit to 1 will reset all registers in the GCLK to their initial state after a Power Reset, except for generic clocks and associated Generators that have their WRTLOCK bit in PCHCTRLm set to 1.

Refer to GENCTRL Reset Value for details on GENCTRL register reset.

Refer to PCHCTRL Reset Value for details on PCHCTRL register reset.

Due to synchronization, there is a waiting period between setting CTRLA.SWRST and a completed Reset. CTRLA.SWRST and SYNCBUSY.SWRST will both be cleared when the reset is complete.

Value	Description
0	There is no Reset operation ongoing.
1	A Reset operation is ongoing.

16.8.2 Synchronization Busy

(BODVDD.STBYCFG=1). The frequency of the clock ticks ($F_{clksampling}$) is controlled by the Prescaler Select bit groups in the BODVDD register (BODVDD.PSEL).

$$F_{clksampling} = \frac{F_{clkprescaler}}{2^{(\mathrm{PSEL}+1)}}$$

The prescaler signal ($F_{clkprescaler}$) is a 1KHz clock, output by the 32KHz Ultra Low Power Oscillator OSCULP32K.

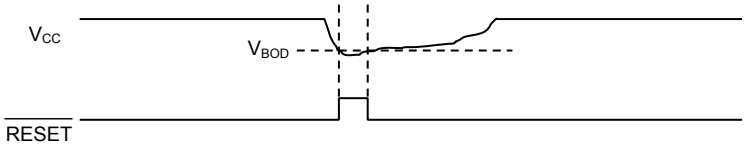
As the sampling clock is different from the APB clock domain, synchronization among the clocks is necessary. See also Synchronization.

22.6.3.7 Hysteresis

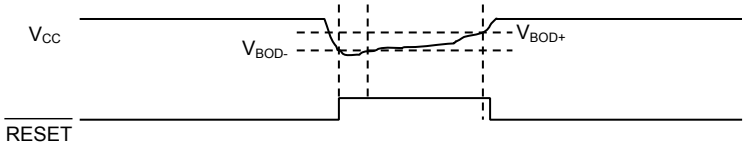
A hysteresis on the trigger threshold of a BOD will reduce the sensitivity to ripples on the monitored voltage: instead of switching $\overline{\text{RESET}}$ at each crossing of V_{BOD}, the thresholds for switching $\overline{\text{RESET}}$ on and off are separated (V_{BOD-} and V_{BOD+}, respectively).

Figure 22-2. BOD Hysteresis Principle

Hysteresis OFF:



Hysteresis ON:



Enabling the BODVDD hysteresis by writing the Hysteresis bit in the BODVDD register (BODVDD.HYST) to '1' will add hysteresis to the BODVDD threshold level.

The hysteresis functionality can be used in both Continuous and Sampling Mode.

22.6.3.8 Sleep Mode Operation

Standby Mode

The BODVDD can be used in standby mode if the BOD is enabled and the corresponding Run in Standby bit is written to '1' (BODVDD.RUNSTDBY).

The BODVDD can be configured to work in either Continuous or Sampling Mode by writing a '1' to the Configuration in Standby Sleep Mode bit (BODVDD.STDBYCFG).

22.6.4 Interrupts

The SUPC has the following interrupt sources, which are either synchronous or asynchronous wake-up sources:

- BODVDD Ready (BODVDDRDY), synchronous
- BODVDD Detection (BODVDDDET), asynchronous
- BODVDD Synchronization Ready (BVDDSRDY), synchronous

Each interrupt source has an interrupt flag associated with it. The interrupt flag in the Interrupt Flag Status and Clear register (INTFLAG) is set when the interrupt condition occurs.

This bus clock (CLK_DMAC_APB) is always synchronous to the module clock (CLK_DMAC_AHB), but can be divided by a prescaler and may run even when the module clock is turned off.

Related Links

Peripheral Clock Masking

25.5.4 DMA

Not applicable.

25.5.5 Interrupts

The interrupt request line is connected to the interrupt controller. Using the DMAC interrupt requires the interrupt controller to be configured first.

Related Links

Nested Vector Interrupt Controller

25.5.6 Events

The events are connected to the event system.

Related Links

EVSYS – Event System

25.5.7 Debug Operation

When the CPU is halted in debug mode the DMAC will halt normal operation. The DMAC can be forced to continue operation during debugging. Refer to DBGCTRL for details.

25.5.8 Register Access Protection

All registers with write-access can be write-protected optionally by the Peripheral Access Controller (PAC), except for the following registers:

- Interrupt Pending register (INTPEND)
- Channel ID register (CHID)
- Channel Interrupt Flag Status and Clear register (CHINTFLAG)

Optional write-protection by the Peripheral Access Controller (PAC) is denoted by the "PAC Write-Protection" property in each individual register description.

PAC write-protection does not apply to accesses through an external debugger.

Related Links

PAC - Peripheral Access Controller

25.5.9 Analog Connections

Not applicable.

25.6 Functional Description

25.6.1 Principle of Operation

The DMAC consists of a DMA module and a CRC module.

25.6.1.1 DMA

The DMAC can transfer data between memories and peripherals without interaction from the CPU. The data transferred by the DMAC are called transactions, and these transactions can be split into smaller data transfers. Figure 'DMA Transfer Sizes' shows the relationship between the different transfer sizes:

The corresponding DMAC Enable bit in the Control register is cleared (CTRL.DMAENABLE=0) when the entire DMAC module is disabled.

25.6.3.7 CRC Operation

A cyclic redundancy check (CRC) is an error detection technique used to find errors in data. It is commonly used to determine whether the data during a transmission, or data present in data and program memories has been corrupted or not. A CRC takes a data stream or a block of data as input and generates a 16- or 32-bit output that can be appended to the data and used as a checksum.

When the data is received, the device or application repeats the calculation: If the new CRC result does not match the one calculated earlier, the block contains a data error. The application will then detect this and may take a corrective action, such as requesting the data to be sent again or simply not using the incorrect data.

The CRC engine in DMAC supports two commonly used CRC polynomials: CRC-16 (CRC-CCITT) and CRC-32 (IEEE 802.3). Typically, applying CRC-n (CRC-16 or CRC-32) to a data block of arbitrary length will detect any single alteration that is ≤n bits in length, and will detect the fraction 1-2-n of all longer error bursts.

- CRC-16:
  - Polynomial: $x^{16}+ x^{12}+ x^5+ 1$
  - Hex value: 0x1021
- CRC-32:
  - Polynomial: $x^{32}+x^{26}+ x^{23}+ x^{22}+x^{16}+ x^{12}+ x^{11}+ x^{10}+ x^8+ x^7+ x^5+ x^4+ x^2+ x + 1$
  - Hex value: 0x04C11DB7

The data source for the CRC engine can either be one of the DMA channels or the APB bus interface, and must be selected by writing to the CRC Input Source bits in the CRC Control register (CRCCTRL.CRCSRC). The CRC engine then takes data input from the selected source and generates a checksum based on these data. The checksum is available in the CRC Checksum register (CRCCHKSUM). When CRC-32 polynomial is used, the final checksum read is bit reversed and complemented, as shown in Figure 25-16.

The CRC polynomial is selected by writing to the CRC Polynomial Type bit in the CRC Control register (CRCCTRL.CRCPOLY), the default is CRC-16. The CRC engine operates on byte only. When the DMA is used as data source for the CRC engine, the DMA channel beat size setting will be used. When used with APB bus interface, the application must select the CRC Beat Size bit field of CRC Control register (CRCCTRL.CRCBEATSIZE). 8-, 16-, or 32-bit bus transfer access type is supported. The corresponding number of bytes will be written in the CRCDATAIN register and the CRC engine will operate on the input data in a byte by byte manner.

Bits 3:2 – FQOS[1:0]: Fetch Quality of Service
These bits define the memory priority access during the fetch operation.

FQOS[1:0]	Name	Description
0x0	DISABLE	Background (no sensitive operation)
0x1	LOW	Sensitive Bandwidth
0x2	MEDIUM	Sensitive Latency
0x3	HIGH	Critical Latency

Bits 1:0 – WRBQOS[1:0]: Write-Back Quality of Service
These bits define the memory priority access during the write-back operation.

WRBQOS[1:0]	Name	Description
0x0	DISABLE	Background (no sensitive operation)
0x1	LOW	Sensitive Bandwidth
0x2	MEDIUM	Sensitive Latency
0x3	HIGH	Critical Latency

Related Links
SRAM Quality of Service

25.8.8 Software Trigger Control

Name: SWTRIGCTRL
Offset: 0x10
Reset: 0x00000000
Property: PAC Write-Protection

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the flag.

Bit 1 – SB: Slave on Bus
The Slave on Bus flag (SB) is set when a byte is successfully received in master read mode, i.e., no arbitration lost or bus error occurred during the operation. When this flag is set, the master forces the SCL line low, stretching the I^2C clock period. The SCL line will be released and SB will be cleared on one of the following actions:

- Writing to ADDR.ADDR
- Writing to DATA.DATA
- Reading DATA.DATA when smart mode is enabled (CTRLB.SMEN)
- Writing a valid command to CTRLB.CMD

Writing '1' to this bit location will clear the SB flag. The transaction will not continue or be terminated until one of the above actions is performed.

Writing '0' to this bit has no effect.

Bit 0 – MB: Master on Bus
This flag is set when a byte is transmitted in master write mode. The flag is set regardless of the occurrence of a bus error or an arbitration lost condition. MB is also set when arbitration is lost during sending of NACK in master read mode, or when issuing a start condition if the bus state is unknown. When this flag is set and arbitration is not lost, the master forces the SCL line low, stretching the I^2C clock period. The SCL line will be released and MB will be cleared on one of the following actions:

- Writing to ADDR.ADDR
- Writing to DATA.DATA
- Reading DATA.DATA when smart mode is enabled (CTRLB.SMEN)
- Writing a valid command to CTRLB.CMD

Writing '1' to this bit location will clear the MB flag. The transaction will not continue or be terminated until one of the above actions is performed.

Writing '0' to this bit has no effect.

33.10.7 Status

Name: STATUS
Offset: 0x1A [ID-00001bb3]
Reset: 0x0000
Property: Write-Synchronized

- Drive Control register (DRVCTRL)
- Wave register (WAVE)
- Event Control register (EVCTRL)

Enable-protected bits in the CTRLA register can be written at the same time as CTRLA.ENABLE is written to '1', but not at the same time as CTRLA.ENABLE is written to '0'. Enable-protection is denoted by the "Enable-Protected" property in the register description.

Before enabling the TC, the peripheral must be configured by the following steps:

1. Enable the TC bus clock (CLK_TCx_APB).
2. Select 8-, 16- or 32-bit counter mode via the TC Mode bit group in the Control A register (CTRLA.MODE). The default mode is 16-bit.
3. Select one wave generation operation in the Waveform Generation Operation bit group in the WAVE register (WAVE.WAVEGEN).
4. If desired, the GCLK_TCx clock can be prescaled via the Prescaler bit group in the Control A register (CTRLA.PRESCALER).
   – If the prescaler is used, select a prescaler synchronization operation via the Prescaler and Counter Synchronization bit group in the Control A register (CTRLA.PRESYNC).
5. If desired, select one-shot operation by writing a '1' to the One-Shot bit in the Control B Set register (CTRLBSET.ONESHOT).
6. If desired, configure the counting direction 'down' (starting from the TOP value) by writing a '1' to the Counter Direction bit in the Control B register (CTRLBSET.DIR).
7. For capture operation, enable the individual channels to capture in the Capture Channel x Enable bit group in the Control A register (CTRLA.CAPTEN).
8. If desired, enable inversion of the waveform output or IO pin input signal for individual channels via the Invert Enable bit group in the Drive Control register (DRVCTRL.INVEN).

35.6.2.2 Enabling, Disabling, and Resetting

The TC is enabled by writing a '1' to the Enable bit in the Control A register (CTRLA.ENABLE). The TC is disbled by writing a zero to CTRLA.ENABLE.

The TC is reset by writing a '1' to the Software Reset bit in the Control A register (CTRLA.SWRST). All registers in the TC, except DBGCTRL, will be reset to their initial state. Refer to the CTRLA register for details.

The TC should be disabled before the TC is reset in order to avoid undefined behavior.

35.6.2.3 Prescaler Selection

The GCLK_TCx is fed into the internal prescaler.

The prescaler consists of a counter that counts up to the selected prescaler value, whereupon the output of the prescaler toggles.

If the prescaler value is higher than one, the counter update condition can be optionally executed on the next GCLK_TCx clock pulse or the next prescaled clock pulse. For further details, refer to Prescaler (CTRLA.PRESCALER) and Counter Synchronization (CTRLA.PRESYNC) description.

Prescaler outputs from 1 to 1/1024 are available. For a complete list of available prescaler outputs, see the register description for the Prescaler bit group in the Control A register (CTRLA.PRESCALER).

Note: When counting events, the prescaler is bypassed.

The joint stream of prescaler ticks and event action ticks is called CLK_TC_CNT.

35.7.1 Register Summary - 8-bit Mode

Offset	Name	Bit Pos.								
0x00	CTRLA	7:0	ONDEMAND	RUNSTDBY	PRESCSYNC[1:0]		MODE[1:0]		ENABLE	SWRST
0x01		15:8					ALOCK	PRESCALER[2:0]		
0x02		23:16			COPEN1	COPEN0			CAPTEN1	CAPTEN0
0x03		31:24				CAPTMODE1[1:0]			CAPTMODE0[1:0]	
0x04	CTRLBCLR	7:0	CMD[2:0]					ONESHOT	LUPD	DIR
0x05	CTRLBSET	7:0	CMD[2:0]					ONESHOT	LUPD	DIR
0x06	EVCTRL	7:0			TCEI	TCINV		EVACT[2:0]		
0x07		15:8			MCEOx	MCEOx				OVFEO
0x08	INTENCLR	7:0				MCx			ERR	OVF
0x09	INTENSET	7:0				MCx			ERR	OVF
0x0A	INTFLAG	7:0				MCx			ERR	OVF
0x0B	STATUS	7:0				CCBUFVx	PERBUFV		SLAVE	STOP
0x0C	WAVE	7:0							WAVEGEN[1:0]	
0x0D	DRVCTRL	7:0								INVENx
0x0E	Reserved									
0x0F	DBGCTRL	7:0								DBGRUN
0x10	SYNCBUSY	7:0		CCx	PER	COUNT	STATUS	CTRLB	ENABLE	SWRST
0x11		15:8								
0x12		23:16								
0x13		31:24								
0x14	COUNT	7:0	COUNT[7:0]							
0x15 ... 0x1A	Reserved									
0x1B	PER	7:0	PER[7:0]							
0x1C	CC0	7:0	CC[7:0]							
0x1D	CC1	7:0	CC[7:0]							
0x1E ... 0x2E	Reserved									
0x2F	PERBUF	7:0	PERBUF[7:0]							
0x30	CCBUF0	7:0	CCBUF[7:0]							
0x31	CCBUF1	7:0	CCBUF[7:0]							

35.7.1.1 Control A

Name: CTRLA
Offset: 0x00
Reset: 0x00000000
Property: PAC Write-Protection, Write-Synchronized, Enable-Protected

Value	Description
0	The Error interrupt is disabled.
1	The Error interrupt is enabled.

Bit 0 – OVF: Overflow Interrupt Enable
Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the Overflow Interrupt Enable bit, which enables the Overflow interrupt request.

Value	Description
0	The Overflow interrupt is disabled.
1	The Overflow interrupt is enabled.

35.7.1.7 Interrupt Flag Status and Clear

Name: INTFLAG
Offset: 0x0A
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
				MCx			ERR	OVF
Access				R/W			R/W	R/W
Reset				0			0	0

Bit 4 – MCx: Match or Capture Channel x
This flag is set on a comparison match, or when the corresponding CCx register contains a valid capture value. This flag is set on the next CLK_TC_CNT cycle, and will generate an interrupt request if the corresponding Match or Capture Channel x Interrupt Enable bit in the Interrupt Enable Set register (INTENSET.MCx) is '1'.

Writing a '0' to one of these bits has no effect.

Writing a '1' to one of these bits will clear the corresponding Match or Capture Channel x interrupt flag

In capture operation, this flag is automatically cleared when CCx register is read.

Bit 1 – ERR: Error Interrupt Flag
This flag is set when a new capture occurs on a channel while the corresponding Match or Capture Channel x interrupt flag is set, in which case there is nowhere to store the new capture.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the Error interrupt flag.

Bit 0 – OVF: Overflow Interrupt Flag
This flag is set on the next CLK_TC_CNT cycle after an overflow condition occurs, and will generate an interrupt request if INTENCLR.OVF or INTENSET.OVF is '1'.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the Overflow interrupt flag.

35.7.1.8 Status

This bit is also set when the CCBUFx is written, and cleared on update condition. The bit is automatically cleared when the STATUS.CCBUFx bit is cleared.

Bit 5 – PER: PER Synchronization Busy
This bit is cleared when the synchronization of PER between the clock domains is complete.

This bit is set when the synchronization of PER between clock domains is started.

This bit is also set when the PER is written, and cleared on update condition. The bit is automatically cleared when the STATUS.PERBUF bit is cleared.

Bit 4 – COUNT: COUNT Synchronization Busy
This bit is cleared when the synchronization of COUNT between the clock domains is complete.

This bit is set when the synchronization of COUNT between clock domains is started.

Bit 3 – STATUS: STATUS Synchronization Busy
This bit is cleared when the synchronization of STATUS between the clock domains is complete.

This bit is set when a '1' is written to the Capture Channel Buffer Valid status flags (STATUS.CCBUFVx) and the synchronization of STATUS between clock domains is started.

Bit 2 – CTRLB: CTRLB Synchronization Busy
This bit is cleared when the synchronization of CTRLB between the clock domains is complete.

This bit is set when the synchronization of CTRLB between clock domains is started.

Bit 1 – ENABLE: ENABLE Synchronization Busy
This bit is cleared when the synchronization of ENABLE bit between the clock domains is complete.

This bit is set when the synchronization of ENABLE bit between clock domains is started.

Bit 0 – SWRST: SWRST Synchronization Busy
This bit is cleared when the synchronization of SWRST bit between the clock domains is complete.

This bit is set when the synchronization of SWRST bit between clock domains is started.

35.7.1.13 Counter Value, 8-bit Mode

Note: Prior to any read access, this register must be synchronized by user by writing the according TC Command value to the Control B Set register (CTRLBSET.CMD=READSYNC).

Name: COUNT
Offset: 0x14
Reset: 0x00
Property: PAC Write-Protection, Write-Synchronized, Read-Synchronized

Bit	7	6	5	4	3	2	1	0
	COUNT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – COUNT[7:0]: Counter Value
These bits contain the current counter value.

Condition	Interrupt request	Event output	Event input	DMA request	DMA request is cleared
Capture Overflow Error	Yes				
Debug Fault State	Yes				
Recoverable Faults	Yes				
Non-Recoverable Faults	Yes				
TCCx Event 0 input			Yes(4)		
TCCx Event 1 input			Yes(5)		

Notes:

1. DMA request set on overflow, underflow or re-trigger conditions.
2. Can perform capture or generate recoverable fault on an event input.
3. In capture or circular modes.
4. On event input, either action can be executed:
   - re-trigger counter
   - control counter direction
   - stop the counter
   - decrement the counter
   - perform period and pulse width capture
   - generate non-recoverable fault
5. On event input, either action can be executed:
   - re-trigger counter
   - increment or decrement counter depending on direction
   - start the counter
   - increment or decrement counter based on direction
   - increment counter regardless of direction
   - generate non-recoverable fault

36.6.5.1 DMA Operation

The TCC can generate the following DMA requests:

Counter overflow (OVF)
If the Ones-shot Trigger mode in the control A register (CTRLA.DMAOS) is written to '0', the TCC generates a DMA request on each cycle when an update condition (overflow, underflow or re-trigger) is detected.
When an update condition (overflow, underflow or re-trigger) is detected while CTRLA.DMAOS=1, the TCC generates a DMA trigger on the cycle following the DMA One-Shot Command written to the Control B register (CTRLBSET.CMD=DMAOS).

In both cases, the request is cleared by hardware on DMA acknowledge.

Channel Match (MCx)
A DMA request is set only on a compare match if CTRLA.DMAOS=0. The request is cleared by hardware on DMA acknowledge.
When CTRLA.DMAOS=1, the DMA requests are not generated.

Name: PERBUF
Offset: 0x6C [ID-00002e48]
Reset: 0xFFFFFFFF
Property: Write-Synchronized, Read-Synchronized

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	PERBUF[17:10]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	15	14	13	12	11	10	9	8
	PERBUF[9:2]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
	PERBUF[1:0]		DITHERBUF[5:0]					
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bits 23:6 – PERBUF[17:0]: Period Buffer Value
These bits hold the value of the period buffer register. The value is copied to PER register on UPDATE condition.

Note: When the TCC is configured as 16-bit timer/counter, the excess bits are read zero.

Note: This bit field occupies the MSB of the register, [23:m]. m is dependent on the Resolution bit in the Control A register (CTRLA.RESOLUTION):

CTRLA.RESOLUTION	Bits [23:m]
0x0 - NONE	23:0
0x1 - DITH4	23:4
0x2 - DITH5	23:5
0x3 - DITH6	23:6 (depicted)

Bits 5:0 – DITHERBUF[5:0]: Dithering Buffer Cycle Number
These bits represent the PER.DITHER bits buffer. When the double buffering is enabled, the value of this bit field is copied to the PER.DITHER bits on an UPDATE condition.
Note: This bit field consists of the n LSB of the register. n is dependent on the value of the Resolution bits in the Control A register (CTRLA.RESOLUTION):

2.2. Select the required voltage for the internal voltage reference INTREF by writing to the Voltage Reference Selection bits (SUPC.VREF.SEL). The required value can be found in the Electrical Characteristics.

2.3. Enable routing INTREF to the ADC by writing a '1' to the Voltage Reference Output Enable bit (SUPC.VREF.VREFOE).

3. Configure the ADC:

3.1. Select the internal voltage reference INTREF as ADC reference voltage by writing to the Reference Control register (ADC.REFCTRL.REFSEL).

3.2. Select the temperature sensor vs. internal GND as input by writing TEMP and GND to the positive and negative MUX Input Selection bit fields (ADC.INPUTCTRL.MUXNEG and .MUXPOS, respectively).

3.3. Configure the remaining ADC parameters according to the Electrical Characteristics.

3.4. Enable the ADC and acquire a value, ADC_m.

Calculation Parameter Values

The temperature sensor behavior is linear, but it is sensitive to several parameters such as the internal voltage reference - which itself depends on the temperature. To take this into account, each device contains a Temperature Log row with individual calibration data measured and written during the production tests. These calibration values are read by software to infer the most accurate temperature readings possible.

The Temperature Log Row basically contains the following parameter set for two different temperatures ("ROOM" and "HOT"):

- Calibration temperatures in °C. One at room temperature $temp_R$, one at a higher temperature $temp_H$:
  - ROOM_TEMP_VAL_INT and ROOM_TEMP_VAL_DEC contain the measured temperature at room insertion, $temp_R$, in °C, separated in integer and decimal value.
    Example: For ROOM_TEMP_VAL_INT=0x19=25 and ROOM_TEMP_VAL_DEC=2, the measured temperature at room insertion is 25.2°C.
  - HOT_TEMP_VAL_INT and HOT_TEMP_VAL_DEC contain the measured temperature at hot insertion, $temp_H$, in °C. The integer and decimal value are also separated.
- For each temperature, the corresponding sensor value at the ADC in 12-bit, ADC_R and ADC_H:
  - ROOM_ADC_VAL contains the 12-bit ADC value, ADC_R, corresponding to $temp_R$. Its conversion to Volt is denoted V_{ADCR}.
  - HOT_ADC_VAL contains the 12-bit ADC value, ADC_H, corresponding to $temp_H$. Its conversion to Volt is denoted V_{ADCH}.
- Actual reference voltages at each calibration temperature in Volt, $INT1V_R$ and $INT1V_H$, respectively:
  - ROOM_INT1V_VAL is the 2's complement of the internal 1V reference value at $temp_R$: $INT1V_R$.
  - HOT_INT1V_VAL is the 2's complement of the internal 1V reference value at $temp_H$: $INT1V_H$.
  - Both ROOM_INT1V_VAL and HOT_INT1V_VAL values are centered around 1V with a 0.001V step. In other words, the range of values [0,127] corresponds to [1V, 0.873V] and the range of values [-1, -127] corresponds to [1.001V, 1.127V]. INT1V == 1 - (VAL/1000) is valid for both ranges.

Calculating the Temperature by Linear Interpolation

Using the data pairs ($temp_R$, V_{ADCR}) and ($temp_H$, V_{ADCH}) for a linear interpolation, we have the following equation:

Register Synchronization

Value	Description
0	There is no reset operation ongoing.
1	The reset operation is ongoing.

38.8.2 Control B

Name: CTRLB
Offset: 0x01 [ID-0000120e]
Reset: 0x00
Property: PAC Write-Protection, Enable-Protected

Bit	7	6	5	4	3	2	1	0
						PRESCALER[2:0]		
Access						R/W	R/W	R/W
Reset						0	0	0

Bits 2:0 – PRESCALER[2:0]: Prescaler Configuration
This field defines the ADC clock relative to the peripheral clock.

This field is not synchronized. For the slave ADC, these bits have no effect when the SLAVEEN bit is set (CTRLA.SLAVEEN= 1).

Value	Name	Description
0x0	DIV2	Peripheral clock divided by 2
0x1	DIV4	Peripheral clock divided by 4
0x2	DIV8	Peripheral clock divided by 8
0x3	DIV16	Peripheral clock divided by 16
0x4	DIV32	Peripheral clock divided by 32
0x5	DIV64	Peripheral clock divided by 64
0x6	DIV128	Peripheral clock divided by 128
0x7	DIV256	Peripheral clock divided by 256

38.8.3 Reference Control

Name: REFCTRL
Offset: 0x02 [ID-0000120e]
Reset: 0x00
Property: PAC Write-Protection, Enable-Protected

Bit	7	6	5	4	3	2	1	0
	REFCOMP				REFSEL[3:0]			
Access	R/W				R/W	R/W	R/W	R/W
Reset	0				0	0	0	0

Bit 7 – REFCOMP: Reference Buffer Offset Compensation Enable
The gain error can be reduced by enabling the reference buffer offset compensation. This will decrease the input impedance and thus increase the start-up time of the reference.

Value	Description
0	Disable the digital result correction.
1	Enable the digital result correction. The ADC conversion result in the RESULT register is then corrected for gain and offset based on the values in the GAINCORR and OFFSETCORR registers. Conversion time will be increased by 13 cycles according to the value in the Offset Correction Value bit group in the Offset Correction register.

Bit 2 – FREERUN: Free Running Mode

Value	Description
0	The ADC run in single conversion mode.
1	The ADC is in free running mode and a new conversion will be initiated when a previous conversion completes.

Bit 1 – LEFTADJ: Left-Adjusted Result

Value	Description
0	The ADC conversion result is right-adjusted in the RESULT register.
1	The ADC conversion result is left-adjusted in the RESULT register. The high byte of the 12-bit result will be present in the upper part of the result register. Writing this bit to zero (default) will right-adjust the value in the RESULT register.

Bit 0 – DIFFMODE: Differential Mode

Value	Description
0	The ADC is running in singled-ended mode.
1	The ADC is running in differential mode. In this mode, the voltage difference between the MUXPOS and MUXNEG inputs will be converted by the ADC.

38.8.11 Average Control

Name: AVGCTRL
Offset: 0x0C [ID-0000120e]
Reset: 0x00
Property: PAC Write-Protection, Write-Synchronized

Bit	7	6	5	4	3	2	1	0
		ADJRES[2:0]			SAMPLENUM[3:0]			
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bits 6:4 – ADJRES[2:0]: Adjusting Result / Division Coefficient
These bits define the division coefficient in 2n steps.

Bits 3:0 – SAMPLENUM[3:0]: Number of Samples to be Collected
These bits define how many samples are added together. The result will be available in the Result register (RESULT). Note: if the result width increases, CTRLC.RESSEL must be changed.

Value	Description
0x0	1 sample
0x1	2 samples

Name: ANACTRL
Offset: 0x2C [ID-0000243d]
Reset: 0x00
Property: PAC Write-Protection, Write-Synchronized.

Bit	7	6	5	4	3	2	1	0
	BUFTEST	ONCHOP		CTLSDADC[4:0]				
Access	R/W	R/W		R/W	R/W	R/W	R/W	R/W
Reset	0	0		0	0	0	0	0

Bit 7 – BUFTEST: Buffer Test

Bit 6 – ONCHOP: ONCHOP

Value	Description
0	No Chopper at SDADC input
1	Chopper at SDADC input

Bits 4:0 – CTLSDADC[4:0]: CTLSDADC
SDADC Bias Current Control and used for Debugg/Characterization

39.8.22 Debug Control

Name: DBGCTRL
Offset: 0x2E [ID-0000243d]
Reset: 0x00
Property: PAC Write-Protectedion

Bit	7	6	5	4	3	2	1	0
								DBGRUN
Access								R/W
Reset								0

Bit 0 – DBGRUN: Debug Run
This bit is not reset by a software reset.

This bit controls the functionality when the CPU is halted by an external debugger.

This bit should be written only while a conversion is not ongoing.

Value	Description
0	The SDADC is halted when the CPU is halted by an external debugger.
1	The SDADC continues normal operation when the CPU is halted by an external debugger.