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Details

E·XF

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, WDT
Number of I/O	52
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 20x12b, 3x16b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamc21j16a-mut

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access		•						
Reset								
Bit	15	14	13	12	11	10	9	8
Access		•						
Reset								
Bit	7	6	5	4	3	2	1	0
	REVISION[3:0]			JEPU	JEPIDCH[2:0]			
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	1	0	0	1

Bits 7:4 - REVISION[3:0]: Revision Number

Revision of the peripheral. Starts at 0x0 and increments by one at both major and minor revisions.

Bit 3 – JEPU: JEP-106 Identity Code is used

This bit will always return one when read, indicating that JEP-106 code is used.

Bits 2:0 – JEPIDCH[2:0]: JEP-106 Identity Code High

These bits will always return 0x1 when read, (JEP-106 identity code is 0x1F).

13.13.18 Peripheral Identification 3

 Name:
 PID3

 Offset:
 0x1FEC

 Reset:
 0x0000000

 Property:

Related Links

Peripheral Clock Masking OSC32KCTRL – 32KHz Oscillators Controller

23.5.4 DMA

Not applicable.

23.5.5 Interrupts

The interrupt request line is connected to the interrupt controller. Using the WDT interrupt(s) requires the interrupt controller to be configured first.

Related Links

Nested Vector Interrupt Controller Overview Interrupt Line Mapping

23.5.6 Events

Not applicable.

23.5.7 Debug Operation

When the CPU is halted in debug mode the WDT will halt normal operation.

23.5.8 Register Access Protection

All registers with write-access can be write-protected optionally by the Peripheral Access Controller (PAC), except for the following registers:

• Interrupt Flag Status and Clear (INTFLAG) register

Optional write-protection by the Peripheral Access Controller (PAC) is denoted by the "PAC Write-Protection" property in each individual register description.

PAC write-protection does not apply to accesses through an external debugger.

23.5.9 Analog Connections

Not applicable.

23.6 Functional Description

23.6.1 Principle of Operation

The Watchdog Timer (WDT) is a system for monitoring correct program operation, making it possible to recover from error situations such as runaway code, by issuing a Reset. When enabled, the WDT is a constantly running timer that is configured to a predefined time-out period. Before the end of the time-out period, the WDT should be set back, or else, a system Reset is issued.

The WDT has two modes of operation, Normal mode and Window mode. Both modes offer the option of Early Warning interrupt generation. The description for each of the basic modes is given below. The settings in the Control A register (CTRLA) and the Interrupt Enable register (handled by INTENCLR/INTENSET) determine the mode of operation:

Value	Name	Description
0x6	DIV32	CLK_RTC_CNT = GCLK_RTC/32
0x7	DIV64	CLK_RTC_CNT = GCLK_RTC/64
0x8	DIV128	CLK_RTC_CNT = GCLK_RTC/128
0x9	DIV256	CLK_RTC_CNT = GCLK_RTC/256
0xA	DIV512	CLK_RTC_CNT = GCLK_RTC/512
0xB	DIV1024	CLK_RTC_CNT = GCLK_RTC/1024
0xC-0xF	-	Reserved

Bits 3:2 – MODE[1:0]: Operating Mode

This field defines the operating mode of the RTC. This bit is not synchronized.

Value	Name	Description
0x0	COUNT32	Mode 0: 32-bit counter
0x1	COUNT16	Mode 1: 16-bit counter
0x2	CLOCK	Mode 2: Clock/calendar
0x3	-	Reserved

Bit 1 – ENABLE: Enable

Due to synchronization there is delay from writing CTRLA.ENABLE until the peripheral is enabled/ disabled. The value written to CTRLA.ENABLE will read back immediately and the Enable bit in the Synchronization Busy register (SYNCBUSY.ENABLE) will be set. SYNCBUSY.ENABLE will be cleared when the operation is complete.

Value	Description
0	The peripheral is disabled
1	The peripheral is enabled

Bit 0 – SWRST: Software Reset

Writing a '0' to this bit has no effect.

Writing a '1' to this bit resets all registers in the RTC (except DBGCTRL) to their initial state, and the RTC will be disabled.

Writing a '1' to CTRLA.SWRST will always take precedence, meaning that all other writes in the same write-operation will be discarded.

Due to synchronization there is a delay from writing CTRLA.SWRST until the reset is complete. CTRLA.SWRST will be cleared when the reset is complete.

Value	Description
0	There is not reset operation ongoing
1	The reset operation is ongoing

24.10.2 Event Control in COUNT16 mode (CTRLA.MODE=1)

Name:EVCTRLOffset:0x04Reset:0x00000000Property:PAC Write-Protection, Enable-Protected

more transfer requests while one is already pending, the additional ones will be lost. All channels pending status flags are also available in the Pending Channels register (PENDCH).

When the transfer starts, the corresponding Channel Busy status flag is set in Channel Status register (CHSTATUS.BUSY). When the trigger action is complete, the Channel Busy status flag is cleared. All channel busy status flags are also available in the Busy Channels register (BUSYCH) in DMAC.

25.6.2.7 Addressing

Each block transfer needs to have both a source address and a destination address defined. The source address is set by writing the Transfer Source Address (SRCADDR) register, the destination address is set by writing the Transfer Destination Address (SRCADDR) register.

The addressing of this DMAC module can be static or incremental, for either source or destination of a block transfer, or both.

Incrementation for the source address of a block transfer is enabled by writing the Source Address Incrementation Enable bit in the Block Transfer Control register (BTCTRL.SRCINC=1). The step size of the incrementation is configurable and can be chosen by writing the Step Selection bit in the Block Transfer Control register (BTCTRL.STEPSEL=1) and writing the desired step size in the Address Increment Step Size bit group in the Block Transfer Control register (BTCTRL.STEPSIZE). If BTCTRL.STEPSEL=0, the step size for the source incrementation will be the size of one beat.

When source address incrementation is configured (BTCTRL.SRCINC=1), SRCADDR is calculated as follows:

If **BTCTRL**.STEPSEL=1:

$SRCADDR = SRCADDR_{START} + BTCNT \cdot (BEATSIZE + 1) \cdot 2^{STEPSIZE}$

If **BTCTRL**.STEPSEL=0:

 $SRCADDR = SRCADDR_{START} + BTCNT \cdot (BEATSIZE + 1)$

- SRCADDR_{START} is the source address of the first beat transfer in the block transfer
- BTCNT is the initial number of beats remaining in the block transfer
- BEATSIZE is the configured number of bytes in a beat
- STEPSIZE is the configured number of beats for each incrementation

The following figure shows an example where DMA channel 0 is configured to increment the source address by one beat after each beat transfer (BTCTRL.SRCINC=1), and DMA channel 1 is configured to increment the source address by two beats (BTCTRL.SRCINC=1, BTCTRL.STEPSEL=1, and BTCTRL.STEPSIZE=0x1). As the destination address for both channels are peripherals, destination incrementation is disabled (BTCTRL.DSTINC=0).

Name: CHID Offset: 0x3F [ID-00001ece] Reset: 0x00 Property: -

Bit	7	6	5	4	3	2	1	0
						ID[;	3:0]	
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bits 3:0 – ID[3:0]: Channel ID

These bits define the channel number that will be affected by the channel registers (CH*). Before reading or writing a channel register, the channel ID bit group must be written first.

25.8.18 Channel Control A

This register affects the DMA channel that is selected in the Channel ID register (CHID.ID).

Name: CHCTRLA Offset: 0x40 [ID-00001ece] Reset: 0x00 Property: PAC Write-Protection, Enable-Protected

Bit	7	6	5	4	3	2	1	0
		RUNSTDBY					ENABLE	SWRST
Access	R	R/W	R	R	R	R	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 6 – RUNSTDBY: Channel run in standby

This bit is used to keep the DMAC channel running in standby mode.

This bit is not enable-protected.

Value	Description
0	The DMAC channel is halted in standby.
1	The DMAC channel continues to run in standby.

Bit 1 – ENABLE: Channel Enable

Writing a '0' to this bit during an ongoing transfer, the bit will not be cleared until the internal data transfer buffer is empty and the DMA transfer is aborted. The internal data transfer buffer will be empty once the ongoing burst transfer is completed.

Writing a '1' to this bit will enable the DMA channel.

This bit is not enable-protected.

Value	Description
0	DMA channel is disabled.
1	DMA channel is enabled.

Bit 0 – SWRST: Channel Software Reset

Writing a '0' to this bit has no effect.

Value	Description
0	The NMI edge detection is synchronously operated.
1	The NMI edge detection is asynchronously operated.

Bit 3 – NMIFILTEN: Non-Maskable Interrupt Filter Enable

Value	Description
0	NMI filter is disabled.
1	NMI filter is enabled.

Bits 2:0 – NMISENSE[2:0]: Non-Maskable Interrupt Sense Configuration

These bits define on which edge or level the NMI triggers.

Value	Name	Description
0x0	NONE	No detection
0x1	RISE	Rising-edge detection
0x2	FALL	Falling-edge detection
0x3	BOTH	Both-edge detection
0x4	HIGH	High-level detection
0x5	LOW	Low-level detection
0x6 - 0x7	-	Reserved

26.8.3 Non-Maskable Interrupt Flag Status and Clear



Bit 0 – NMI: Non-Maskable Interrupt

This flag is cleared by writing a '1' to it.

This flag is set when the NMI pin matches the NMI sense configuration, and will generate an interrupt request.

Writing a '0' to this bit has no effect.

26.8.4 Synchronization Busy

CMD[6:0]	Group Configuration	Description
0x48	UDR	Unlock Data Region - Unlocks the data region containing the address location in the ADDR register. When the Security Extension is enabled, only secure access can unlock secure regions.
0x47-0x7F	-	Reserved

27.8.2 Control B

 Name:
 CTRLB

 Offset:
 0x04 [ID-0000b2c]

 Reset:
 0x0000080

 Property:
 PAC Write-Protection

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
						CACHEDIS	READMO	DDE[1:0]
Access						R/W	R/W	R/W
Reset						0	0	0
Bit	15	14	13	12	11	10	9	8
							SLEEPF	PRM[1:0]
Access							R/W	R/W
Reset							0	0
Bit	7	6	5	4	3	2	1	0
	MANW	6[3:0]						
Access	R/W			R/W	R/W	R/W	R/W	
Reset	1			0	0	0	0	

Bit 18 – CACHEDIS: Cache Disable

This bit is used to disable the cache.

Value	Description
0	The cache is enabled
1	The cache is disabled

Bits 17:16 - READMODE[1:0]: NVMCTRL Read Mode

27.8.10 Page Buffer Load Data 0

Name:	PBLDATA0
Offset:	0x28
Reset:	0xFFFFFFF
Property:	-

Bit	31	30	29	28	27	26	25	24
				PBLDAT	A[31:24]			
Access	R	R	R	R	R	R	R	R
Reset	1	1	1	1	1	1	1	1
Bit	23	22	21	20	19	18	17	16
				PBLDAT	A[23:16]			
Access	R	R	R	R	R	R	R	R
Reset	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8
				PBLDA	TA[15:8]			
Access	R	R	R	R	R	R	R	R
Reset	1	1	1	1	1	1	1	1
Bit	7	6	5	4	3	2	1	0
				PBLDA	TA[7:0]			
Access	R	R	R	R	R	R	R	R
Reset	1	1	1	1	1	1	1	1

Bits 31:0 – PBLDATA[31:0]: Page Buffer Load Data

The PBLDATA register is a holding register for partial AHB writes to the same 64-bit page buffer section. Page buffer loads are performed on a 64-bit basis.

This is a read only register.

27.8.11 Page Buffer Load Data 1

Name:PBLDATA1Offset:0x2CReset:0xFFFFFFFProperty: -

D .(0-	
Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access		I		I		Į	ļ	
Reset								
Bit	15	14	13	12	11	10	9	8
					HDRD	LY[1:0]	BRKLE	EN[1:0]
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0
Bit	7	6	5	4	3	2	1	0
							GTIME[2:0]	
Access						R/W	R/W	R/W
Reset						0	0	0

Bits 11:10 – HDRDLY[1:0]: LIN Master Header Delay

These bits define the delay between break and sync transmission in addition to the delay between the sync and identifier (ID) fields when in LIN master mode (CTRLA.FORM=0x2). This field is only valid when using the LIN header command (CTRLB.LINCMD=0x2).

Value	Description
0x0	Delay between break and sync transmission is 1 bit time.
	Delay between sync and ID transmission is 1 bit time.
0x1	Delay between break and sync transmission is 4 bit time.
	Delay between sync and ID transmission is 4 bit time.
0x2	Delay between break and sync transmission is 8 bit time.
	Delay between sync and ID transmission is 4 bit time.
0x3	Delay between break and sync transmission is 14 bit time.
	Delay between sync and ID transmission is 4 bit time.

Bits 9:8 – BRKLEN[1:0]: LIN Master Break Length

These bits define the length of the break field transmitted when in LIN master mode (CTRLA.FORM=0x2).

Value	Description
0x0	Break field transmission is 13 bit times
0x1	Break field transmission is 17 bit times
0x2	Break field transmission is 21 bit times
0x3	Break field transmission is 26 bit times

Bits 2:0 – GTIME[2:0]: Guard Time

These bits define the guard time when using RS485 mode (CTRLA.TXPO=0x3).

Figure 34-3. Pin Control in Bus Monitoring Mode



Bus Monitoring Mode

34.6.2.7 Disabled Automatic Retransmission

According to the CAN Specification (see ISO 11898-1, 6.3.3 Recovery Management), the CAN provides means for automatic retransmission of frames that have lost arbitration or that have been disturbed by errors during transmission. By default automatic retransmission is enabled. To support time-triggered communication as described in ISO 11898-1, chapter 9.2, the automatic retransmission may be disabled via CCCR.DAR.

Frame Transmission in DAR Mode

In DAR mode all transmissions are automatically cancelled after they started on the CAN bus. A Tx Buffer's Tx Request Pending bit TXBRP.TRPx is reset after successful transmission, when a transmission has not yet been started at the point of cancellation, has been aborted due to lost arbitration, or when an error occurred during frame transmission.

- Successful transmission:
 - Corresponding Tx Buffer Transmission Occurred bit TXBTO.TOx set
 - Corresponding Tx Buffer Cancellation Finished bit TXBCF.CFx not set
- Successful transmission in spite of cancellation:
 - Corresponding Tx Buffer Transmission Occurred bit TXBTO.TOx set
 - Corresponding Tx Buffer Cancellation Finished bit TXBCF.CFx set
- Arbitration lost or frame transmission disturbed:
 - Corresponding Tx Buffer Transmission Occurred bit TXBTO.TOx not set
 - Corresponding Tx Buffer Cancellation Finished bit TXBCF.CFx set

In case of a successful frame transmission, and if storage of Tx events is enabled, a Tx Event FIFO element is written with Event Type ET = "10" (transmission in spite of cancellation).

34.6.2.8 Test Modes

To enable write access to register TEST, bit CCCR.TEST has to be set to '1'. This allows the configuration of the test modes and test functions.

Four output functions are available for the CAN transmit pin CAN_TX by programming TEST.TX. Additionally to its default function – the serial data output – it can drive the CAN Sample Point signal to monitor the CAN's bit timing and it can drive constant dominant or recessive values. The actual value at pin CAN_RX can be read from TEST.RX. Both functions can be used to check the CAN bus' physical layer.

- ...
- Tn Bits 31:24 DBm[7:0]: Data Byte m
- Tn Bits 23:16 DBm-1[7:0]: Data Byte m-1
- Tn Bits 15:8 DBm-2[7:0]: Data Byte m-2
- Tn Bits 7:0 DBm-3[7:0]: Data Byte m-3

Note: Depending on the configuration of TXESC, between two and sixteen 32-bit words (Tn = 3 ... 17) are used for storage of a CAN message's data field.

34.9.4 Tx Event FIFO Element

Each element stores information about transmitted messages. By reading the Tx Event FIFO the Host CPU gets this information in the order the messages were transmitted. Status information about the Tx Event FIFO can be obtained from register TXEFS.

 Table 34-10.
 Tx Event FIFO Element

	31	3 0	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Е	Х	R				l	I													1	1	I			l						
E0	S	Т	Т		ID[28:0]																											
	Т	D	R																													
										-	F	В																				
E1		MM[7:0]						E	1	D	R	DLC[3:0]					TXTS[15:0]															
								[[1:	U	F	s																					

- E0 Bit 31 ESI: Error State Indicator
 - 0 : Transmitting node is error active.
 - 1 : Transmitting node is error passive.
- E0 Bit 30 XTD: Extended Identifier
 - 0 : 11-bit standard identifier.
 - 1 : 29-bit extended identifier.
- E0 Bit 29 RTR: Remote Transmission Request
 - 0 : Received frame is a data frame.
 - 1 : Received frame is a remote frame.
- E0 Bits 28:0 ID[28:0]: Identifier
 - Standard or extended identifier depending on bit XTD. A standard identifier is stored into ID[28:18].
- E1 Bits 31:24 MM[7:0]: Message Marker

Copied from Tx Buffer into Tx Event FIFO element for identification of Tx message status.

• E1 Bits 23:22 - ET[1:0]: Event Type

This field defines the event type.



35.6.2.4 Counter Mode

The counter mode is selected by the Mode bit group in the Control A register (CTRLA.MODE). By default, the counter is enabled in the 16-bit counter resolution. Three counter resolutions are available:

- COUNT8: The 8-bit TC has its own Period Value and Period Buffer Value registers (PER and PERBUF).
- COUNT16: 16-bit is the default counter mode. There is no dedicated period register in this mode.
- COUNT32: This mode is achieved by pairing two 16-bit TC peripherals. TC0 is paired with TC1, and TC2 is paired with TC3. TC4 does not support 32-bit resolution.
 When paired, the TC peripherals are configured using the registers of the even-numbered TC (TC0 or TC2 respectively). The odd-numbered partner (TC1 or TC3 respectively) will act as slave, and the Slave bit in the Status register (STATUS.SLAVE) will be set. The register values of a slave will not reflect the registers of the 32-bit counter. Writing to any of the slave registers will not affect the 32-bit counter. Normal access to the slave COUNT and CCx registers is not allowed.

35.6.2.5 Counter Operations

Depending on the mode of operation, the counter is cleared, reloaded, incremented, or decremented at each TC clock input (CLK_TC_CNT). A counter clear or reload marks the end of the current counter cycle and the start of a new one.

The counting direction is set by the Direction bit in the Control B register (CTRLB.DIR). If this bit is zero the counter is counting up, and counting down if CTRLB.DIR=1. The counter will count up or down for each tick (clock or event) until it reaches TOP or ZERO. When it is counting up and TOP is reached, the counter will be set to zero at the next tick (overflow) and the Overflow Interrupt Flag in the Interrupt Flag Status and Clear register (INTFLAG.OVF) will be set. When it is counting down, the counter is reloaded with the TOP value when ZERO is reached (underflow), and INTFLAG.OVF is set.

INTFLAG.OVF can be used to trigger an interrupt, a DMA request, or an event. An overflow/underflow occurrence (i.e. a compare match with TOP/ZERO) will stop counting if the One-Shot bit in the Control B register is set (CTRLBSET.ONESHOT).

It is possible to change the counter value (by writing directly in the COUNT register) even when the counter is running. When starting the TC, the COUNT value will be either ZERO or TOP (depending on the counting direction set by CTRLBSET.DIR or CTRLBCLR.DIR), unless a different value has been written to it, or the TC has been stopped at a value other than ZERO. The write access has higher priority than count, clear, or reload. The direction of the counter can also be changed during normal operation. See also the figure below.

Bit	31	30	29	28	27	26	25	24	
				PER[31:24]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0	0	0	
Bit	23	22	21	20	19	18	17	16	
				PER[2	23:16]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0 0		
Bit	15	14	13	12	11	10	9	8	
				PER	[15:8]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0	
Bit	7	6	5	4	3	2	1	0	
				PER	[7:0]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	1	

Bits 31:0 - PER[31:0]: Period Value

These bits hold the value of the Period Buffer register PERBUF. The value is copied to PER register on UPDATE condition.

35.7.3.15 Channel x Compare/Capture Value, 32-bit Mode

 Name:
 CCx

 Offset:
 0x1C + x*0x04 [x=0..1]

 Reset:
 0x0000000

 Property:
 Write-Synchronized

Analog-to-Digital Converter (ADC) Characteristics

38.6.2.6 ADC Resolution

The ADC supports 8-bit, 10-bit or 12-bit resolution. Resolution can be changed by writing the Resolution bit group in the Control C register (CTRLC.RESSEL). By default, the ADC resolution is set to 12 bits. The resolution affects the propagation delay, see also Conversion Timing and Sampling Rate.

38.6.2.7 Differential and Single-Ended Conversions

The ADC has two conversion options: differential and single-ended:

If the positive input is always positive, the single-ended conversion should be used in order to have full 12-bit resolution in the conversion.

If the positive input may go below the negative input, the differential mode should be used in order to get correct results.

The differential mode is enabled by setting DIFFMODE bit in the Control C register (CTRLC.DIFFMODE). Both conversion types could be run in single mode or in free-running mode. When the free-running mode is selected, an ADC input will continuously sample the input and performs a new conversion. The INTFLAG.RESRDY bit will be set at the end of each conversion.

38.6.2.8 Conversion Timing and Sampling Rate

The following figure shows the ADC timing for one single conversion. A conversion starts after the software or event start are synchronized with the GCLK_ADCx clock. The input channel is sampled in the first half CLK_ADCx period.

Figure 38-3. ADC Timing for One Conversion in 12-bit Resolution



The sampling time can be increased by using the Sampling Time Length bit group in the Sampling Time Control register (SAMPCTRL.SAMPLEN). As example, the next figure is showing the timing conversion with sampling time increased to six CLK_ADC cycles.

Figure 38-4. ADC Timing for One Conversion with Increased Sampling Time, 12-bit



The ADC provides also offset compensation, see the following figure. The offset compensation is enabled by the Offset Compensation bit in the Sampling Control register (SAMPCTRL.OFFCOMP).

Note: If offset compensation is used, the sampling time must be set to one cycle of CLK_ADCx.

In free running mode, the sampling rate R_S is calculated by

 $R_{S} = f_{CLK_ADC} / (n_{SAMPLING} + n_{OFFCOMP} + n_{DATA})$

Here, $n_{SAMPLING}$ is the sampling duration in CLK_ADC cycles, $n_{OFFCOMP}$ is the offset compensation duration in clock cycles, and n_{DATA} is the bit resolution. f_{CLK_ADC} is the ADC clock frequency from the internal prescaler: $f_{CLK_ADC} = f_{GCLK_ADC} / 2^{(1 + CTRLB.PRESCALER)}$

Bit	15	14	13	12	11	10	9	8
						SWTRIG	OFFSETCORR	GAINCORR
Access						R	R	R
Reset						0	0	0
Bit	7	6	5	4	3	2	1	0
	WINUT	WINLT	SAMPCTRL	AVGCTRL	CTRLC	INPUTCTRL	ENABLE	SWRST
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit 10 – SWTRIG: Software Trigger Synchronization Busy

This bit is cleared when the synchronization of SWTRIG register between the clock domains is complete.

This bit is set when the synchronization of SWTRIG register between clock domains is started.

Bit 9 – OFFSETCORR: Offset Correction Synchronization Busy

This bit is cleared when the synchronization of OFFSETCORR register between the clock domains is complete.

This bit is set when the synchronization of OFFSETCORR register between clock domains is started.

Bit 8 – GAINCORR: Gain Correction Synchronization Busy

This bit is cleared when the synchronization of GAINCORR register between the clock domains is complete.

This bit is set when the synchronization of GAINCORR register between clock domains is started.

Bit 7 – WINUT: Window Monitor Lower Threshold Synchronization Busy

This bit is cleared when the synchronization of WINUT register between the clock domains is complete.

This bit is set when the synchronization of WINUT register between clock domains is started.

Bit 6 – WINLT: Window Monitor Upper Threshold Synchronization Busy

This bit is cleared when the synchronization of WINLT register between the clock domains is complete.

This bit is set when the synchronization of WINLT register between clock domains is started.

Bit 5 – SAMPCTRL: Sampling Time Control Synchronization Busy

This bit is cleared when the synchronization of SAMPCTRL register between the clock domains is complete.

This bit is set when the synchronization of SAMPCTRL register between clock domains is started.

Bit 4 – AVGCTRL: Average Control Synchronization Busy

This bit is cleared when the synchronization of AVGCTRL register between the clock domains is complete.

This bit is set when the synchronization of AVGCTRL register between clock domains is started.

Bit 3 – CTRLC: Control C Synchronization Busy

This bit is cleared when the synchronization of CTRLC register between the clock domains is complete.

This bit is set when the synchronization of CTRLC register between clock domains is started.

Symbol	Parameters	Conditions	Та	Тур.	Max	Units
		fs = 10 ksps / Reference buffer disabled / BIASREFBUF = '111', BIASREFCOMP = '111' VDDANA=Vref= 5.5V		437	528	
		fs = 10 ksps / Reference buffer enabled / BIASREFBUF = '111', BIASREFCOMP = '111' VDDANA=Vref= 5.5V		553	675	

1. These are based on characterization.

45.10.5 Sigma-Delta Analog-to-Digital Converter (SDADC) Characteristics Table 45-22. Operating Conditions⁽¹⁾

Symbol	Parameters	Conditions	Min	Тур	Мах	Unit
Res	Resolution	Differential mode	-	16	-	bits
		Single-Ended mode	-	15	-	
CLK_SDADC	Sampling Clock Speed		1	-	6	MHz
CLK_SDADC_FS	Conversion rate		CLK_SDADC/4			
fs	Output Data Rate	Free running mode	CLK_SD	ADC_F	S / OSR	
		Single conversion mode SKPCNT = N	(CLK_SDADC_FS / OSR) x (N+1)			
OSR	Oversampling ratio	Differential mode	64	256	1024	Cycles
	Input Conversion range	Differential mode Gaincorr = 0x1	-0.7xVREF	-	0.7xVREF	V
		Single-Ended mode Gaincorr = 0x1	0	-	0.7xVREF	
Vref	Reference voltage range		1	-	5.5	V
Vcom	Common mode voltage	Differential mode	0	-	AVDD	V
Cin	Input capacitance		0.425	0,5	0.575	pF
Zin	Input impedance	Differential mode	al 1/(Cin x CLK_SDADC_FS)		ADC_FS)	kΩ

46. Electrical Characteristics 105°C (SAM C20/C21 E/G/J)

46.1 Disclaimer

All typical values are measured at Ta = 25°C unless otherwise specified. All minimum and maximum values are valid across operating temperature and voltage unless otherwise specified.

This chapter contains only characteristics specific for the SAM C20/C21 E/G/J (Ta = 105° C). For all other values or missing characteristics, refer to the 85° C chapter.

46.2 General Operating Ratings

The device must operate within the ratings listed in the table below in order for all other electrical characteristics and typical characteristics of the device to be valid.

 Table 46-1. General operating conditions

Symbol	Parameter	Min.	Тур.	Max.	Units
T _A	Temperature range	-40	25	105	°C
TJ	Junction temperature	-	-	125	°C

46.3 Power Consumption

Table 46-2. Power Consumption⁽¹⁾

Mode	Conditions	Та	Vcc	Тур.	Max.	Units	
ACTIVE	CPU running a While 1	25°C	5.0V	3.8	4.2	mA	
	algorithm	105°C	5.0V	4.0	4.5		
	CPU running a While 1	25°C	3.0V	3.7	4.1	mA	
	algorithm	105°C	3.0V	4.0	4.5		
	CPU running a While 1	25°C	5.0V	71*Freq+160	78*Freq+162	μA (with freq	
	algorithm. with GCLKIN as reference	105°C	5.0V	71*Freq+374	72*Freq+819	in MHz)	
	CPU running a Fibonacci algorithm	25°C	5.0V	4.7	5.2	mA	
		105°C	5.0V	5.0	5.5		
	CPU running a Fibonacci	25°C	3.0V	4.7	5.1	mA	
	algorithm	105°C	3.0V	5.0	5.5		
	CPU running a Fibonacci	25°C	5.0V	90*Freq+163	99*Freq+168	μA (with freq	
	algorithm. with GCLKIN as reference	105°C	5.0V	90*Freq+379	92*Freq+820	in MHz)	
	CPU running a CoreMark	25°C	5.0V	5.9	6.4	mA	
	algorithm	105°C	5.0V	6.3	6.9		

Symbol	Parameter	Conditions	Min.	Тур.	Мах	Units
		XOSC.GAIN=0				
		F = 4MHz CL=20pF XOSC.GAIN=1	-	-	218	
		F = 8MHz CL=20pF XOSC.GAIN=2	-	-	114	
		F = 16MHz CL=20pF XOSC.GAIN=3	-	-	58	
		F = 32MHz CL=12pF XOSC.GAIN=4	-	-	62	
Cxin	Parasitic load capacitor		-	6.7	-	pF
Cxout			-	4.1	-	
Tstart	Startup time	F = 2MHz CL=20pF XOSC.GAIN=0	-	12.3	48.7	KCycles
		F = 4MHz CL=20pF XOSC.GAIN=1	-	8.2	30.1	
		F = 8MHz CL=20pF XOSC.GAIN=2	-	6.2	19.9	
		F = 16MHz CL=20pF XOSC.GAIN=3	-	10.8	30.1	
		F = 32MHz CL=12pF XOSC.GAIN=4	-	8.7	23.6	

1. These are based on characterization.

47.6.2 External 32kHz Crystal Oscillator (XOSC32K) Characteristics

The following table describes the characteristics for the oscillator when a digital clock is applied on XIN32 pin.

resistor. External or internal pull up/down resistors can be used, e.g. the pins can be configured in pull-up or pull-down mode eliminating the need for external components. There are no obvious benefit in choosing external vs. internal pull resistors.

Related Links

PORT - I/O Pin Controller

49.7 Clocks and Crystal Oscillators

The SAM C20/C21 can be run from internal or external clock sources, or a mix of internal and external sources. An example of usage will be to use the internal 8MHz oscillator as source for the system clock, and an external 32.768kHz watch crystal as clock source for the Real-Time counter (RTC).

49.7.1 External Clock Source

Figure 49-6. External Clock Source Schematic



Table 49-4. External Clock Source Connections

Signal Name	Recommended Pin Connection	Description
XIN	XIN is used as input for an external clock signal	Input for inverting oscillator pin
XOUT/GPIO	Can be left unconnected or used as normal GPIO	NC/GPIO

49.7.2 Crystal Oscillator

Figure 49-7. Crystal Oscillator Schematic



The crystal should be located as close to the device as possible. Long signal lines may cause too high load to operate the crystal, and cause crosstalk to other parts of the system.

Table 49-5. Crystal Oscillator Checklist

Signal Name	Recommended Pin Connection	Description
XIN	Load capacitor 15pF ⁽¹⁾⁽²⁾	External crystal between 0.4 to 32MHz
XOUT	Load capacitor 15pF ⁽¹⁾⁽²⁾	

V_{DD} Cortex Debug Connector (10-pin) SWDIO VTref RESET GND SWDCLK GND NC SWCLK NC NC RESET NC SWDIO GND

Figure 49-12. Cortex Debug Connector (10-pin)

Table 49-8. Cortex Debug Connector (10-pir	e 49-8. Cortex Debug Connect	or (10-pin)
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Header Signal Name	Description
SWDCLK	Serial wire clock pin
SWDIO	Serial wire bidirectional data pin
RESET	Target device reset pin, active low
VTref	Target voltage sense, should be connected to the device V_{DD}
GND	Ground

49.8.2 10-pin JTAGICE3 Compatible Serial Wire Debug Interface

The JTAGICE3 debugger and programmer does not support the Cortex Debug Connector (10-pin) directly, hence a special pinout is needed to directly connect the SAM C20/C21 to the JTAGICE3, alternatively one can use the JTAGICE3 squid cable and manually match the signals between the JTAGICE3 and SAM C20/C21. Figure 49-13 describes how to connect a 10-pin header that support connecting the JTAGICE3 directly to the SAM C20/C21 without the need for a squid cable. This can also be used for the Atmel-ICE AVR connector port.

The JTAGICE3 squid cable or the JTACICE3 50mil cable can be used to connect the JTAGICE3 programmer and debugger to the SAM C20/C21. 10-pin JTAGICE3 Compatible Serial Wire Debug Interface illustrates the correct pinout for the JTAGICE3 50 mil, and details are given in Table 49-9.