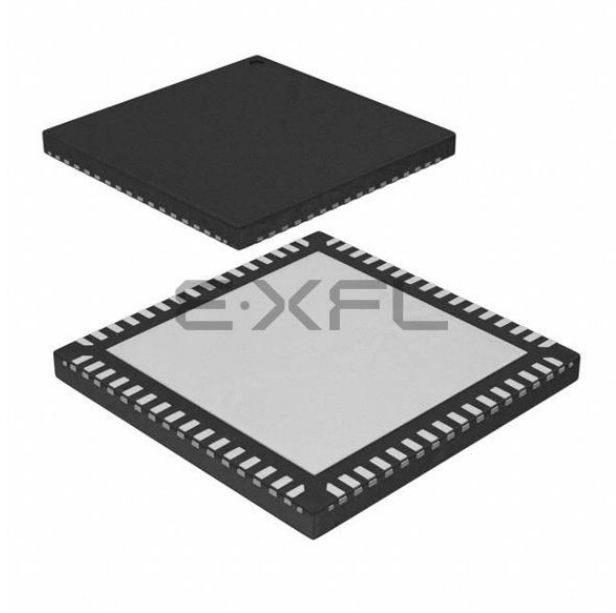

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

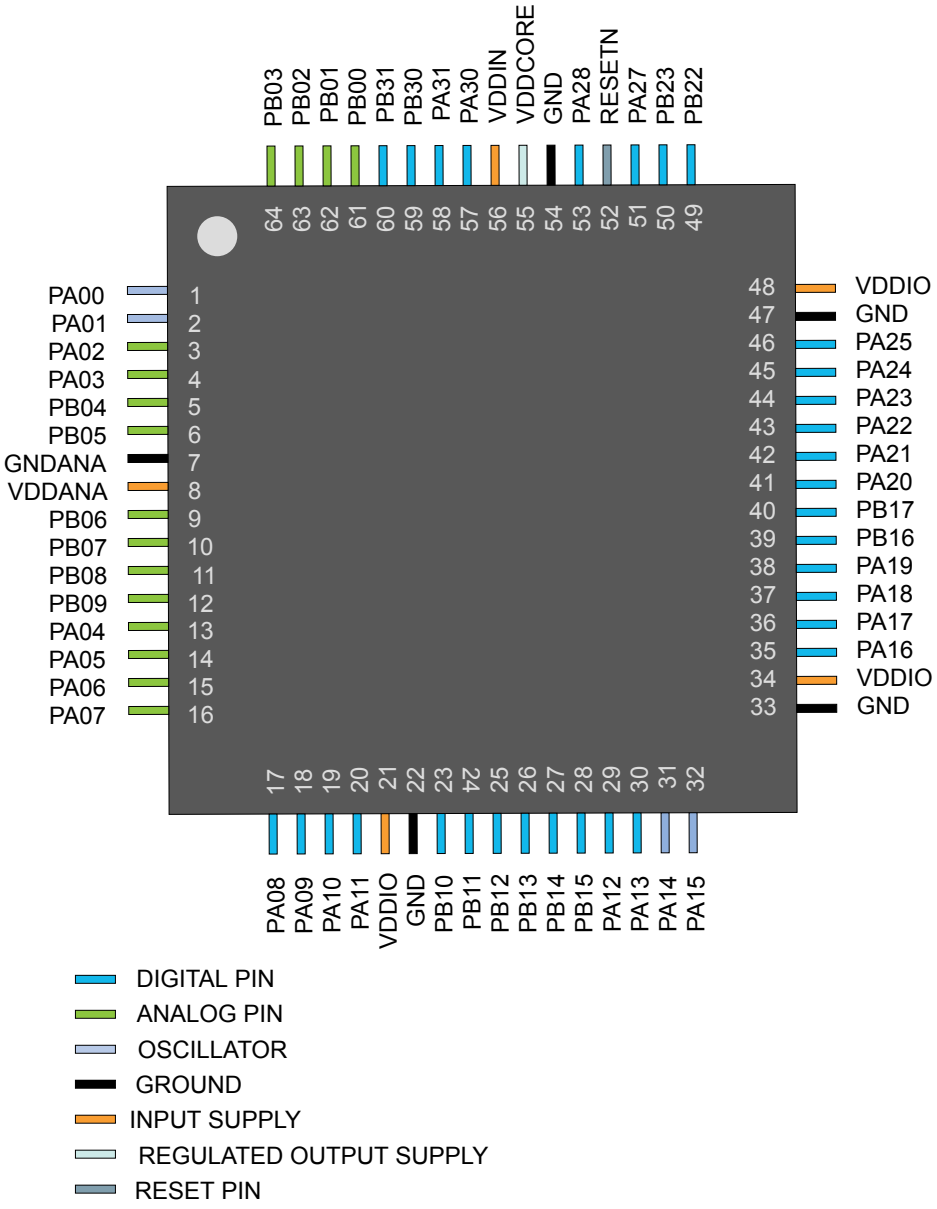
Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, WDT
Number of I/O	52
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 20x12b, 3x16b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamc21j17a-mnt

3. Block Diagram

Note: Not all features are available for all devices. Please refer to Table 1-3 and Table 1-4 to determine feature availability for the particular device.

4.3 SAM C21J / SAM C20J

4.3.1 QFN64/TQFP64



9. Memories

9.1 Embedded Memories

- Internal high-speed Flash with read-while-write capability on section of the array
- Internal high-speed RAM, single-cycle access at full speed

9.2 Physical Memory Map

The High-Speed bus is implemented as a bus matrix. All High-Speed bus addresses are fixed, and they are never remapped in any way, even during boot. The 32-bit physical address space is mapped as follows:

Table 9-1. SAM C20/C21 Physical Memory Map(1)

Memory	Start address	Size	Size	Size	Size
		x18	x17	x16	x15
Embedded Flash	0x00000000	256Kbytes	128Kbytes	64Kbytes	32Kbytes
Embedded RWW section	0x00400000	8Kbytes	4Kbytes	2Kbytes	1Kbytes
Embedded high-speed SRAM	0x20000000	32Kbytes	16Kbytes	8Kbytes	4Kbytes
AHB-APB Bridge A	0x40000000	64Kbytes	64Kbytes	64Kbytes	64Kbytes
AHB-APB Bridge B	0x41000000	64Kbytes	64Kbytes	64Kbytes	64Kbytes
AHB-APB Bridge C	0x42000000	64Kbytes	64Kbytes	64Kbytes	64Kbytes
AHB-APB Bridge D	0x43000000	64Kbytes	-	-	-
AHB DIVAS	0x48000000	64Kbytes	64Kbytes	64Kbytes	64Kbytes
IOBUS	0x60000000	64Kbytes	64Kbytes	64Kbytes	64Kbytes

Note: 1. x = SAM C20/C21 G/J/E/N. The N-series (100-pin devices) does not include x16 and x15 option.

Table 9-2. SAM C20/C21 Flash Memory Parameters(1)

Device	Flash size (FLASH_PM)	Number of pages (FLASH_P)	Page size (FLASH_W)
x18	256Kbytes	4096	64 bytes
x17	128Kbytes	2048	64 bytes
x16	64Kbytes	1024	64 bytes
x15	32Kbytes	512	64 bytes

Note: 1. x = SAM C20/C21 G/J/E/N. The N-series (100-pin devices) does not include x16 and x15 option.

12. Peripherals Configuration Summary

12.1 SAM C20/C21 N

Table 12-1. Peripherals Configuration Summary SAM C21 N

Peripheral Name	Base Address	IRQ Line	AHB Clock		APB Clock		Generic Clock	PAC		Events		DMA	
			Index	Enabled at Reset	Index	Enabled at Reset	Index	Index	Prot at Reset	User	Generator	Index	Sleep Walking
AHB-APB Bridge A	0x40000000		0	Y									N/A
PAC	0x40000000	0	10	Y	0	Y		0	N		85 : ACCERR		N/A
PM	0x40000400	0			1	Y		1	N				N/A
MCLK	0x40000800	0			2	Y		2	N				Y
RSTC	0x40000C00				3	Y		3	N				N/A
OSCCTRL	0x40001000	0			4	Y	0: FDPLL96M clk source 1: FDPLL96M 32kHz	4	N		0: XOSC_FAIL		Y
OSC32KCTRL	0x40001400	0			5	Y		5	N		1: XOSC32K_FAIL		Y
SUPC	0x40001800	0			6	Y		6	N				N/A
GCLK	0x40001C00				7	Y		7	N				N/A
WDT	0x40002000	1			8	Y		8	N				Y
RTC	0x40002400	2			9	Y		9	N		2: CMP0/ALARM0 3: CMP1 4: OVF5-1 5:12: PER0-7		Y
EIC	0x40002800	3, NMI			10	Y	2	10	N		13-28: EXTINT0-15		Y
FREQM	0x40002C00	4			11	Y	3: Measure 4: Reference	11	N				N/A
TSENS	0x40003000	5			12	N	5	12	N	0: START	29: WINMON	1: RESRDY	A
AHB-APB Bridge B	0x41000000		1	Y									N/A
PORT	0x41000000				0	Y		0	N	1-4 : EV0-3			Y
DSU	0x41002000		3	Y	1	Y		1	Y				N/A
NVMCTRL	0x41004000	6	5	Y	2	Y	39	2	N				Y
DMAC	0x41006000	7	7	Y				3	N	5-8: CH0-3	30-33: CH0-3		Y
MTB	0x41008000								N	45: START 46: STOP			N/A
AHB-APB Bridge C	0x42000000		2	Y									N/A
EVSYS	0x42000000	8			0	N	6-17: one per CHANNEL	0	N				Y
SERCOM0	0x42000400	9			1	N	19: CORE 18: SLOW	1	N			2: RX 3: TX	Y
SERCOM1	0x42000800	10			2	N	20: CORE 18: SLOW	2	N			4: RX 5: TX	Y
SERCOM2	0x42000C00	11			3	N	21: CORE 18: SLOW	3	N			6: RX 7: TX	Y
SERCOM3	0x42001000	12			4	N	22: CORE 18: SLOW	4	N			8: RX 9: TX	Y

index(m)	Name	Description
9	GCLK_EVSYS_CHANNEL_3	EVSYS_CHANNEL_3
10	GCLK_EVSYS_CHANNEL_4	EVSYS_CHANNEL_4
11	GCLK_EVSYS_CHANNEL_5	EVSYS_CHANNEL_5
12	GCLK_EVSYS_CHANNEL_6	EVSYS_CHANNEL_6
13	GCLK_EVSYS_CHANNEL_7	EVSYS_CHANNEL_7
14	GCLK_EVSYS_CHANNEL_8	EVSYS_CHANNEL_8
15	GCLK_EVSYS_CHANNEL_9	EVSYS_CHANNEL_9
16	GCLK_EVSYS_CHANNEL_10	EVSYS_CHANNEL_10
17	GCLK_EVSYS_CHANNEL_11	EVSYS_CHANNEL_11
18	GCLK_SERCOM[0,1,2,3]_SLOW	SERCOM[0,1,2,3]_SLOW
19	GCLK_SERCOM0_CORE	SERCOM0_CORE
20	GCLK_SERCOM1_CORE	SERCOM1_CORE
21	GCLK_SERCOM2_CORE	SERCOM2_CORE
22	GCLK_SERCOM3_CORE	SERCOM3_CORE
23		
24	GCLK_SERCOM5_SLOW	
25	GCLK_SERCOM5_CORE	SERCOM5_CORE
26	GCLK_CAN0	CAN0
27	GCLK_CAN1	CAN1
28	GCLK_TCC0, GCLK_TCC1	TCC0,TCC1
29	GCLK_TCC2	TCC2
30	GCLK_TC0, GCLK_TC1	TC0,TC1
31	GCLK_TC2, GCLK_TC3	TC2,TC3
32	GCLK_TC4	TC4
33	GCLK_ADC0	ADC0
34	GCLK_ADC1	ADC1
35	GCLK_SDADC	SDADC
36	GCLK_DAC	DAC
37	GCLK_PTC	PTC
38	GCLK_CCL	CCL
39	-	Reserved
40	GCLK_AC	AC

18. RSTC – Reset Controller

18.1 Overview

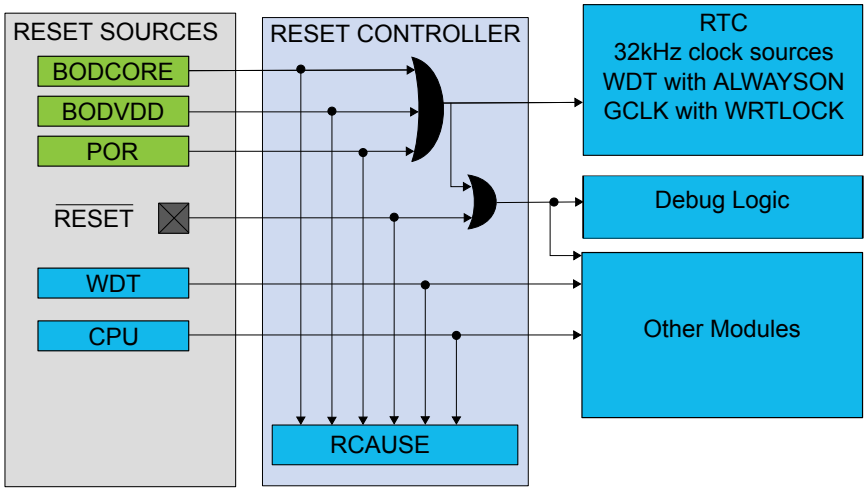
The Reset Controller (RSTC) manages the reset of the microcontroller. It issues a microcontroller reset, sets the device to its initial state and allows the reset source to be identified by software.

18.2 Features

- Reset the microcontroller and set it to an initial state according to the reset source
- Reset cause register for reading the reset source from the application code
- Multiple reset sources
  - Power supply reset sources: POR, BODCORE, BODVDD
  - User reset sources: External reset ($\overline{\text{RESET}}$), Watchdog reset, and System Reset Request

18.3 Block Diagram

Figure 18-1. Reset System



18.4 Signal Description

Signal Name	Type	Description
$\overline{\text{RESET}}$	Digital input	External reset

One signal can be mapped on several pins.

Related Links

I/O Multiplexing and Considerations

18.5 Product Dependencies

In order to use this peripheral, other parts of the system must be configured correctly, as described below.

18.7 Register Summary

Offset	Name	Bit Pos.								
0x00	RCAUSE	7:0		SYST	WDT	EXT		BODVDD	BODCORE	POR

18.8 Register Description

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16- and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly.

Some registers are optionally write-protected by the Peripheral Access Controller (PAC). Optional PAC write-protection is denoted by the "PAC Write-Protection" property in each individual register description. For details, refer to Register Access Protection.

18.8.1 Reset Cause

When a Reset occurs, the bit corresponding to the Reset source is set to '1' and all other bits are written to '0'.

Name: RCAUSE
Offset: 0x00
Property: –

Bit	7	6	5	4	3	2	1	0
		SYST	WDT	EXT		BODVDD	BODCORE	POR
Access		R	R	R		R	R	R
Reset		x	x	x		x	x	x

Bit 6 – SYST: System Reset Request
This bit is set if a System Reset Request has occurred. Refer to the Cortex processor documentation for more details.

Bit 5 – WDT: Watchdog Reset
This bit is set if a Watchdog Timer Reset has occurred.

Bit 4 – EXT: External Reset
This bit is set if an external Reset has occurred.

Bit 2 – BODVDD: Brown Out VDD Detector Reset
This bit is set if a BODVDD Reset has occurred.

Bit 1 – BODCORE: Brown Out CORE Detector Reset
This bit is set if a BODCORE Reset has occurred.

Bit 0 – POR: Power On Reset
This bit is set if a POR has occurred.

(BODVDD.STBYCFG=1). The frequency of the clock ticks ($F_{clksampling}$) is controlled by the Prescaler Select bit groups in the BODVDD register (BODVDD.PSEL).

$$F_{clksampling} = \frac{F_{clkprescaler}}{2^{(\mathrm{PSEL}+1)}}$$

The prescaler signal ($F_{clkprescaler}$) is a 1KHz clock, output by the 32KHz Ultra Low Power Oscillator OSCULP32K.

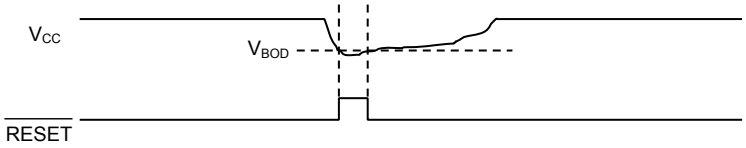
As the sampling clock is different from the APB clock domain, synchronization among the clocks is necessary. See also Synchronization.

22.6.3.7 Hysteresis

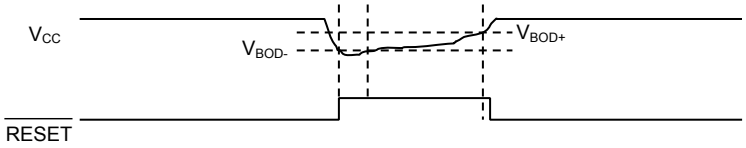
A hysteresis on the trigger threshold of a BOD will reduce the sensitivity to ripples on the monitored voltage: instead of switching $\overline{\text{RESET}}$ at each crossing of V_{BOD}, the thresholds for switching $\overline{\text{RESET}}$ on and off are separated (V_{BOD-} and V_{BOD+}, respectively).

Figure 22-2. BOD Hysteresis Principle

Hysteresis OFF:



Hysteresis ON:



Enabling the BODVDD hysteresis by writing the Hysteresis bit in the BODVDD register (BODVDD.HYST) to '1' will add hysteresis to the BODVDD threshold level.

The hysteresis functionality can be used in both Continuous and Sampling Mode.

22.6.3.8 Sleep Mode Operation

Standby Mode

The BODVDD can be used in standby mode if the BOD is enabled and the corresponding Run in Standby bit is written to '1' (BODVDD.RUNSTDBY).

The BODVDD can be configured to work in either Continuous or Sampling Mode by writing a '1' to the Configuration in Standby Sleep Mode bit (BODVDD.STDBYCFG).

22.6.4 Interrupts

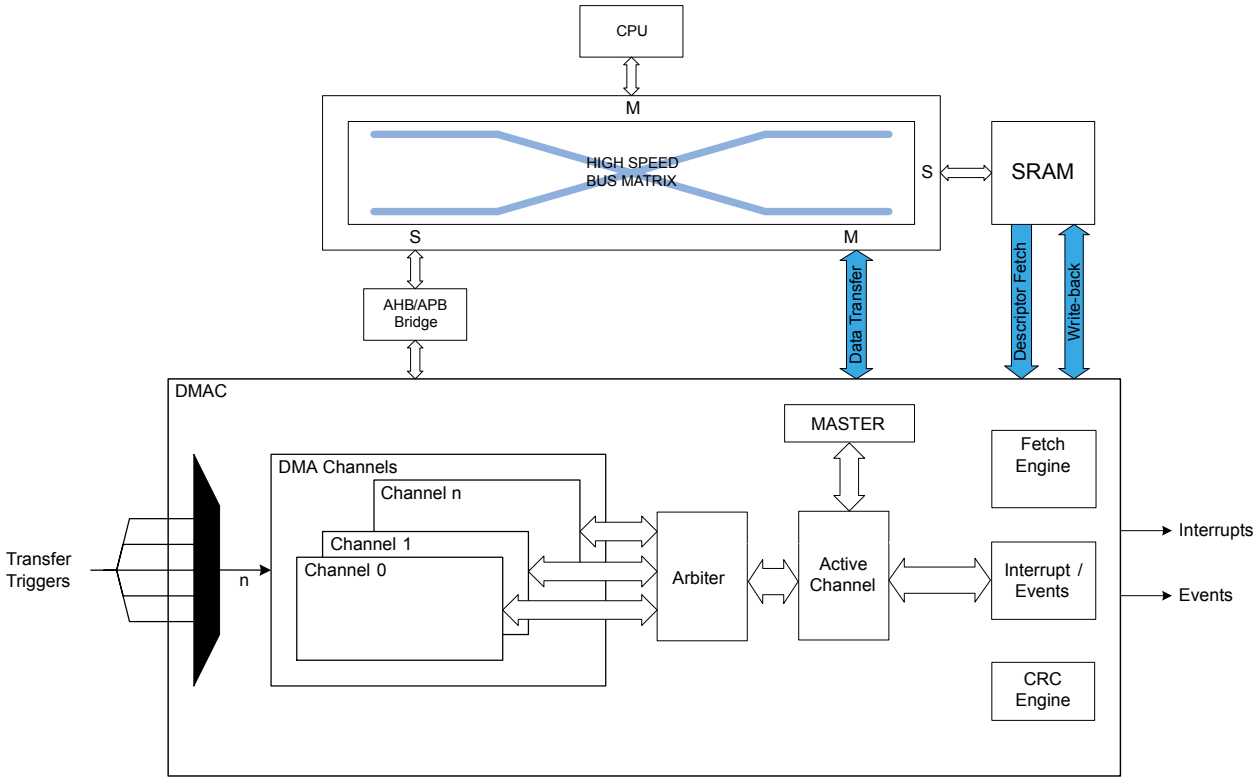
The SUPC has the following interrupt sources, which are either synchronous or asynchronous wake-up sources:

- BODVDD Ready (BODVDDRDY), synchronous
- BODVDD Detection (BODVDDDET), asynchronous
- BODVDD Synchronization Ready (BVDDSRDY), synchronous

Each interrupt source has an interrupt flag associated with it. The interrupt flag in the Interrupt Flag Status and Clear register (INTFLAG) is set when the interrupt condition occurs.

25.3 Block Diagram

Figure 25-1. DMAC Block Diagram



25.4 Signal Description

Not applicable.

25.5 Product Dependencies

In order to use this peripheral, other parts of the system must be configured correctly, as described below.

25.5.1 I/O Lines

Not applicable.

25.5.2 Power Management

The DMAC will continue to operate in any sleep mode where the selected source clock is running. The DMAC's interrupts can be used to wake up the device from sleep modes. Events connected to the event system can trigger other operations in the system without exiting sleep modes. On hardware or software reset, all registers are set to their reset value.

Related Links

PM – Power Manager

25.5.3 Clocks

The DMAC bus clock (CLK_DMAC_APB) must be configured and enabled in the Main Clock module before using the DMAC.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					HDRDLY[1:0]		BRKLEN[1:0]	
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
						GTIME[2:0]		
Access						R/W	R/W	R/W
Reset						0	0	0

Bits 11:10 – HDRDLY[1:0]: LIN Master Header Delay

These bits define the delay between break and sync transmission in addition to the delay between the sync and identifier (ID) fields when in LIN master mode (CTRLA.FORM=0x2).
This field is only valid when using the LIN header command (CTRLB.LINCMD=0x2).

Value	Description
0x0	Delay between break and sync transmission is 1 bit time. Delay between sync and ID transmission is 1 bit time.
0x1	Delay between break and sync transmission is 4 bit time. Delay between sync and ID transmission is 4 bit time.
0x2	Delay between break and sync transmission is 8 bit time. Delay between sync and ID transmission is 4 bit time.
0x3	Delay between break and sync transmission is 14 bit time. Delay between sync and ID transmission is 4 bit time.

Bits 9:8 – BRKLEN[1:0]: LIN Master Break Length

These bits define the length of the break field transmitted when in LIN master mode (CTRLA.FORM=0x2).

Value	Description
0x0	Break field transmission is 13 bit times
0x1	Break field transmission is 17 bit times
0x2	Break field transmission is 21 bit times
0x3	Break field transmission is 26 bit times

Bits 2:0 – GTIME[2:0]: Guard Time

These bits define the guard time when using RS485 mode (CTRLA.TXPO=0x3).

Related Links

PORT: IO Pin Controller

32.5.2 Power Management

This peripheral can continue to operate in any sleep mode where its source clock is running. The interrupts can wake up the device from sleep modes.

Related Links

PM – Power Manager

32.5.3 Clocks

The SERCOM bus clock (CLK_SERCOMx_APB) can be enabled and disabled in the Main Clock Controller. Refer to *Peripheral Clock Masking* for details and default status of this clock.

A generic clock (GCLK_SERCOMx_CORE) is required to clock the SPI. This clock must be configured and enabled in the Generic Clock Controller before using the SPI.

This generic clock is asynchronous to the bus clock (CLK_SERCOMx_APB). Therefore, writes to certain registers will require synchronization to the clock domains.

Related Links

GCLK - Generic Clock Controller

Peripheral Clock Masking

Synchronization

32.5.4 DMA

The DMA request lines are connected to the DMA Controller (DMAC). In order to use DMA requests with this peripheral the DMAC must be configured first. Refer to *DMAC – Direct Memory Access Controller* for details.

Related Links

DMAC – Direct Memory Access Controller

32.5.5 Interrupts

The interrupt request line is connected to the Interrupt Controller. In order to use interrupt requests of this peripheral, the Interrupt Controller (NVIC) must be configured first. Refer to *Nested Vector Interrupt Controller* for details.

Related Links

Nested Vector Interrupt Controller

32.5.6 Events

Not applicable.

32.5.7 Debug Operation

When the CPU is halted in debug mode, this peripheral will continue normal operation. If the peripheral is configured to require periodical service by the CPU through interrupts or similar, improper operation or data loss may result during debugging. This peripheral can be forced to halt operation during debugging - refer to the Debug Control (DBGCTRL) register for details.

32.5.8 Register Access Protection

Registers with write-access can be write-protected optionally by the peripheral access controller (PAC).

PAC Write-Protection is not available for the following registers:

Value	Description
0	Data Register Empty interrupt is disabled.
1	Data Register Empty interrupt is enabled.

32.8.5 Interrupt Enable Set

This register allows the user to disable an interrupt without read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Clear register (INTENCLR).

Name: INTENSET
Offset: 0x16 [ID-00000e74]
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
	ERROR				SSL	RXC	TXC	DRE
Access	R/W				R/W	R/W	R/W	R/W
Reset	0				0	0	0	0

Bit 7 – ERROR: Error Interrupt Enable
Writing '0' to this bit has no effect.

Writing '1' to this bit will set the Error Interrupt Enable bit, which enables the Error interrupt.

Value	Description
0	Error interrupt is disabled.
1	Error interrupt is enabled.

Bit 3 – SSL: Slave Select Low Interrupt Enable
Writing '0' to this bit has no effect.

Writing '1' to this bit will set the Slave Select Low Interrupt Enable bit, which enables the Slave Select Low interrupt.

Value	Description
0	Slave Select Low interrupt is disabled.
1	Slave Select Low interrupt is enabled.

Bit 2 – RXC: Receive Complete Interrupt Enable
Writing '0' to this bit has no effect.

Writing '1' to this bit will set the Receive Complete Interrupt Enable bit, which enables the Receive Complete interrupt.

Value	Description
0	Receive Complete interrupt is disabled.
1	Receive Complete interrupt is enabled.

Bit 1 – TXC: Transmit Complete Interrupt Enable
Writing '0' to this bit has no effect.

Writing '1' to this bit will set the Transmit Complete Interrupt Enable bit, which enables the Transmit Complete interrupt.

Writes to any register while synchronization is on-going will be discarded and an APB error will be generated.

Value	Description
0	SWRST synchronization is not busy.
1	SWRST synchronization is busy.

33.10.9 Address

Name: ADDR
Offset: 0x24
Reset: 0x0000
Property: Write-Synchronized

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	LEN[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TENBITEN	HS	LENEN			ADDR[10:8]		
Access	R/W	R/W	R/W			R/W	R/W	R/W
Reset	0	0	0			0	0	0

Bit	7	6	5	4	3	2	1	0
	ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 23:16 – LEN[7:0]: Transaction Length
These bits define the transaction length of a DMA transaction from 0 to 255 bytes. The Transfer Length Enable (LENEN) bit must be written to '1' in order to use DMA.

Bit 15 – TENBITEN: Ten Bit Addressing Enable
This bit enables 10-bit addressing. This bit can be written simultaneously with ADDR to indicate a 10-bit or 7-bit address transmission.

Value	Description
0	10-bit addressing disabled.
1	10-bit addressing enabled.

Bit 14 – HS: High Speed
This bit enables High-speed mode for the current transfer from repeated START to STOP. This bit can be written simultaneously with ADDR for a high speed transfer.

Table 34-15. Extended Message ID Filter Element

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F0	EFEC [2:0]			EFID1[28:0]																												
F1	EFT [1:0]			EFID2[28:0]																												

- F0 Bits 31:29 - EFEC[2:0]: Extended Filter Element Configuration

  All enabled filter elements are used for acceptance filtering of extended frames. Acceptance filtering stops at the first matching enabled filter element or when the end of the filter list is reached. If EFEC = “100”, “101”, or “110” a match sets interrupt flag IR.HPM and, if enabled, an interrupt is generated. In this case register HPMS is updated with the status of the priority match.

Table 34-16. Extended Filter Element Configuration

Value	Name	Description
0x0	DISABLE	Disable filter element.
0x1	STF0M	Store in Rx FIFO 0 if filter matches.
0x2	STF1M	Store in Rx FIFO 1 if filter matches.
0x3	REJECT	Reject ID if filter matches.
0x4	PRIORITY	Set priority if filter matches.
0x5	PRIF0M	Set priority and store in FIFO 0 if filter matches.
0x6	PRIF1M	Set priority and store in FIFO 1 if filter matches.
0x7	STRXBUF	Store into Rx Buffer or as debug message, configuration of EFT[1:0] ignored.

- F0 Bits 28:0 - EFID1[28:0]: Extended Filter ID 1

  First ID of extended ID filter element.

  When filtering for Rx Buffers or for debug messages this field defines the ID of a extended mesage to be stored. The received identifiers must match exactly, only XIDAM masking mechanism is used.
- F1 Bits 31:30 - EFT[1:0]: Extended Filter Type

  This field defines the extended filter type.

Table 34-17. Extended Filter Type

Value	Name	Description
0x0	RANGEM	Range filter from EFID1 to EFID2 (EFID2 >= EFID1).
0x1	DUAL	Dual ID filter for EFID1 or EFID2.
0x2	CLASSIC	Classic filter: EFID1 = filter, EFID2 = mask.
0x3	RANGE	Range filter from EFID1 to EFID2 (EFID2 >= EFID1), XIDAM mask not applied.

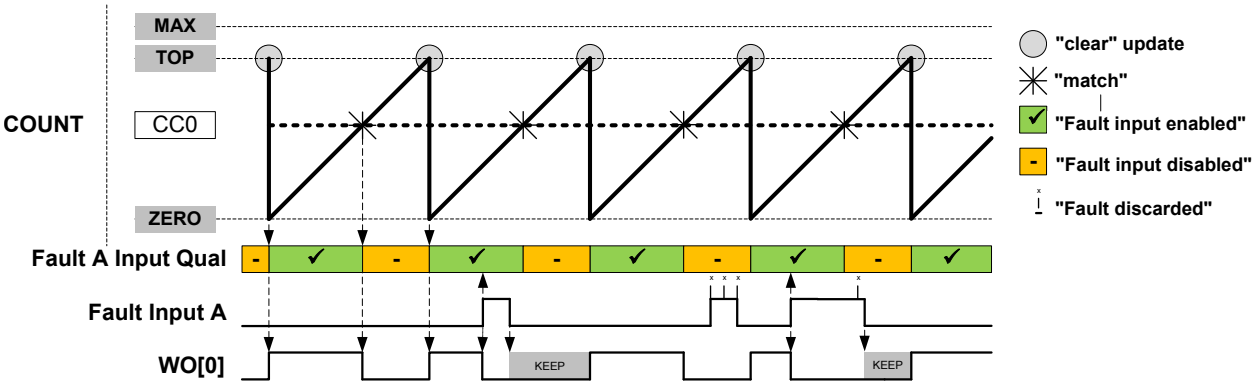
- F1 Bits 28:0 - EFID2[28:0]: Extended Filter ID 2

Fault Actions

Different fault actions can be configured individually for Fault A and Fault B. Most fault actions are not mutually exclusive; hence two or more actions can be enabled at the same time to achieve a result that is a combination of fault actions.

Keep Action This is enabled by writing the Fault n Keeper bit in the Recoverable Fault n Configuration register (FCTRLn.KEEP) to '1'. When enabled, the corresponding channel output will be clamped to zero as long as the fault condition is present. The clamp will be released on the start of the first cycle after the fault condition is no longer present, see next Figure.

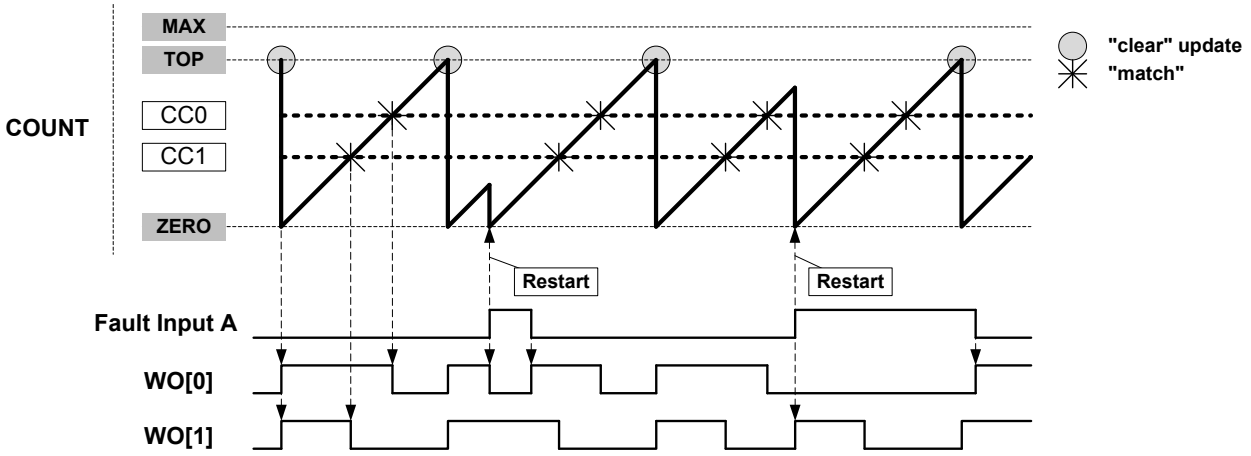
Figure 36-25. Waveform Generation with Fault Qualification and Keep Action



Restart Action This is enabled by writing the Fault n Restart bit in Recoverable Fault n Configuration register (FCTRLn.RESTART) to '1'. When enabled, the timer/counter will be restarted as soon as the corresponding fault condition is present. The ongoing cycle is stopped and the timer/counter starts a new cycle, see Figure 36-26. In Ramp 1 mode, when the new cycle starts, the compare outputs will be clamped to inactive level as long as the fault condition is present.

Note: For RAMP2 operation, when a new timer/counter cycle starts the cycle index will change automatically, see Figure 36-27. Fault A and Fault B are qualified only during the cycle A and cycle B respectively: Fault A is disabled during cycle B, and Fault B is disabled during cycle A.

Figure 36-26. Waveform Generation in RAMP1 mode with Restart Action



Bit	31	30	29	28	27	26	25	24
					FILTERVAL[3:0]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	23	22	21	20	19	18	17	16
	BLANKVAL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
		CAPTURE[2:0]			CHSEL[1:0]		HALT[1:0]	
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RESTART	BLANK[1:0]		QUAL	KEEP		SRC[1:0]	
Access	R/W	R/W	R/W	R/W	R/W		R/W	R/W
Reset	0	0	0	0	0		0	0

Bits 27:24 – FILTERVAL[3:0]: Recoverable Fault n Filter Value
These bits define the filter value applied on MCEx (x=0,1) event input line. The value must be set to zero when MCEx event is used as synchronous event.

Bits 23:16 – BLANKVAL[7:0]: Recoverable Fault n Blanking Value
These bits determine the duration of the blanking of the fault input source. Activation and edge selection of the blank filtering are done by the BLANK bits (FCTRLn.BLANK).

When enabled, the fault input source is internally disabled for BLANKVAL* prescaled GCLK_TCC periods after the detection of the waveform edge.

Bits 14:12 – CAPTURE[2:0]: Recoverable Fault n Capture Action
These bits select the capture and Fault n interrupt/event conditions.

Table 36-8. Fault n Capture Action

Value	Name	Description
0x0	DISABLE	Capture on valid recoverable Fault n is disabled
0x1	CAPT	On rising edge of a valid recoverable Fault n, capture counter value on channel selected by CHSEL[1:0]. INTFLAG.FAULTn flag rises on each new captured value.
0x2	CAPTMIN	On rising edge of a valid recoverable Fault n, capture counter value on channel selected by CHSEL[1:0], if COUNT value is lower than the last stored capture value (CC). INTFLAG.FAULTn flag rises on each local minimum detection.
0x3	CAPTMAX	On rising edge of a valid recoverable Fault n, capture counter value on channel selected by CHSEL[1:0], if COUNT value is higher than the last stored capture value (CC).

Name: SHIFTCORR
Offset: 0x1A [ID-0000243d]
Reset: 0x00
Property: PAC Write-Protection, Write-Synchronized

Bit	7	6	5	4	3	2	1	0
					SHIFTCORR[3:0]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bits 3:0 – SHIFTCORR[3:0]: Shift Correction
A specific offset, gain and shift can be applied to SDADC by performing the following operation:

```
(RESULT + OFFSETCORR)*GAINCORR/2^SHIFTCORR
```

39.8.17 Software Trigger

Name: SWTRIG
Offset: 0x1C [ID-0000243d]
Reset: 0x00
Property: PAC Write-Protection, Write-Synchronized

Bit	7	6	5	4	3	2	1	0
							START	FLUSH
Access							W	W
Reset							0	0

Bit 1 – START: SDADC Start Conversion
Writing a one to this bit will start a conversion or sequence. The bit is cleared by hardware when the conversion has started. Setting this bit when it is already set has no effect.

Writing this bit to zero will have no effect.

Bit 0 – FLUSH: SDADC Conversion Flush
Writing a one to this bit will be flush the SDADC pipeline. A flush will restart the SDADC conversion and all conversions in progress will be aborted and lost. This bit is cleared until the SDADC has been flushed.

After the flush, the ADC will resume where it left off; i.e., if a conversion was pending, the ADC will start a new conversion.

Writing this bit to zero will have no effect.

39.8.18 Synchronization Busy

Name: SYNCBUSY
Offset: 0x20 [ID-0000243d]
Reset: 0x00000000
Property: -

Nested Vector Interrupt Controller

40.6.13 Events

The AC can generate the following output events:

- Comparator (COMP0, COMP1, COMP2, COMP3): Generated as a copy of the comparator status
- Window (WIN0, WIN1): Generated as a copy of the window inside/outside status

Writing a one to an Event Output bit in the Event Control Register (EVCTRL.xxEO) enables the corresponding output event. Writing a zero to this bit disables the corresponding output event. Refer to the Event System chapter for details on configuring the event system.

The AC can take the following action on an input event:

- Start comparison (START0, START1, START2, START3): Start a comparison.

Writing a one to an Event Input bit into the Event Control register (EVCTRL.COMPEIx) enables the corresponding action on input event. Writing a zero to this bit disables the corresponding action on input event. Note that if several events are connected to the AC, the enabled action will be taken on any of the incoming events. Refer to the Event System chapter for details on configuring the event system.

When EVCTRL.COMPEIx is one, the event will start a comparison on COMPx after the start-up time delay. In normal mode, each comparator responds to its corresponding input event independently. For a pair of comparators in window mode, either comparator event will trigger a comparison on both comparators simultaneously.

40.6.14 Sleep Mode Operation

The Run in Standby bits in the Comparator x Control registers (COMPCTRLx.RUNSTDBY) control the behavior of the AC during standby sleep mode. Each RUNSTDBY bit controls one comparator. When the bit is zero, the comparator is disabled during sleep, but maintains its current configuration. When the bit is one, the comparator continues to operate during sleep. Note that when RUNSTDBY is zero, the analog blocks are powered off for the lowest power consumption. This necessitates a start-up time delay when the system returns from sleep.

For Window Mode operation, both comparators in a pair must have the same RUNSTDBY configuration.

When RUNSTDBY is one, any enabled AC interrupt source can wake up the CPU. The AC can also be used during sleep modes where the clock used by the AC is disabled, provided that the AC is still powered (not in shutdown). In this case, the behavior is slightly different and depends on the measurement mode, as listed in Table 40-1.

Table 40-1. Sleep Mode Operation

COMPCTRLx.MODE	RUNSTDBY=0	RUNSTDBY=1
0 (Continuous)	COMPx disabled	GCLK_AC stopped, COMPx enabled
1 (Single-shot)	COMPx disabled	GCLK_AC stopped, COMPx enabled only when triggered by an input event

40.6.14.1 Continuous Measurement during Sleep

When a comparator is enabled in continuous measurement mode and GCLK_AC is disabled during sleep, the comparator will remain continuously enabled and will function asynchronously. The current state of the comparator is asynchronously monitored for changes. If an edge matching the interrupt condition is found, GCLK_AC is started to register the interrupt condition and generate events. If the interrupt is enabled in the Interrupt Enable registers (INTENCLR/SET), the AC can wake up the device;

Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the Window x interrupt flag.

Bits 3,2,1,0 – COMPx: Comparator x
Reading this bit returns the status of the Comparator x interrupt flag. If comparator x is not implemented, COMPx always reads as zero.

This flag is set according to the Interrupt Selection bit group in the Comparator x Control register (COMPCTRLx.INTSEL) and will generate an interrupt if INTENCLR/SET.COMPx is also one.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the Comparator x interrupt flag.

40.8.7 Status A

Name: STATUSA
Offset: 0x07
Reset: 0x00
Property: Read-Only

Bit	7	6	5	4	3	2	1	0
	WSTATE1[1:0]		WSTATE0[1:0]		STATEx	STATEx	STATEx	STATEx
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 7:6 – WSTATE1[1:0]: Window 1 Current State
These bits show the current state of the signal if the window 1 mode is enabled.

Value	Name	Description
0x0	ABOVE	Signal is above window
0x1	INSIDE	Signal is inside window
0x2	BELOW	Signal is below window
0x3		Reserved

Bits 5:4 – WSTATE0[1:0]: Window 0 Current State
These bits show the current state of the signal if the window 0 mode is enabled.

Value	Name	Description
0x0	ABOVE	Signal is above window
0x1	INSIDE	Signal is inside window
0x2	BELOW	Signal is below window
0x3		Reserved

Bits 3,2,1,0 – STATEx: Comparator x Current State
This bit shows the current state of the output signal from COMPx. STATEx is valid only when STATUSB.READYx is one.

40.8.8 Status B

NVM erase operations are not protected by the BODVDD and BODCORE in debugger cold-plugging mode. NVM erase operation at supply voltages below product specification minimum can cause corruption of the calibration and other areas mandatory for a correct product behavior.

Table 45-2. General operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{DDIN}	Power supply voltage	2.7(1)	5.0	5.5	V
V_{DDANA}	Analog supply voltage	2.7(1)	5.0	5.5	V
V_{DDIO}	IO supply voltage	2.7(1)	5.0	5.5	V
T_A	Temperature range	-40	25	85	°C
T_J	Junction temperature	-	-	100	°C

1. With BODVDD disabled. If the BODVDD is enabled, refer to Table 45-14

Note:
The same voltage must be applied to VDDIN and VDDANA. VDDIO should be lower or equal to VDDIN / VDDANA. The common voltage is referred to as VDD in the datasheet.

Some I/O are in the VDDIO cluster, but can be multiplexed as analog outputs (e.g. PTC.X[n] pads). In such a case, VDDANA is used to power the I/O. Using this configuration may result in an electrical conflict if the VDDIO voltage is lower than the VDDIN/VDDANA.

Related Links

Brown Out Detectors Characteristics

45.4 Injection Current

Stresses beyond those listed in the table below may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 45-3. Injection Current(1)

Symbol	Description	min	max	Unit
I_{INJ1}(2)	IO pin injection current	-1	+1	mA
I_{INJ2}(3)	IO pin injection current	-15	+15	mA
$I_{INJtotal}$	Sum of IO pins injection current	-45	+45	mA

1. Injecting current may have an effect on the accuracy of the analog blocks.
2. Conditions for V_{PIN}: V_{PIN}<GND-0.6V or 5.5V<V_{PIN}<=6.1V.

   Conditions for VDD 4.9V<VDD<=5.5V.

   If Vpin is lower than GND-0.6V, then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as R = |(GND-0.6V – V_{PIN})/I_{INJ1}|. If Vpin is greater than VDD+0.6V, then a current limiting resistor is required. The positive DC injection current limiting resistor is calculated as R = (V_{PIN}-(VDD+0.6))/I_{INJ1}.
3. Conditions for V_{PIN}: V_{PIN}<GND-0.6V or V_{PIN}<=5.5V.