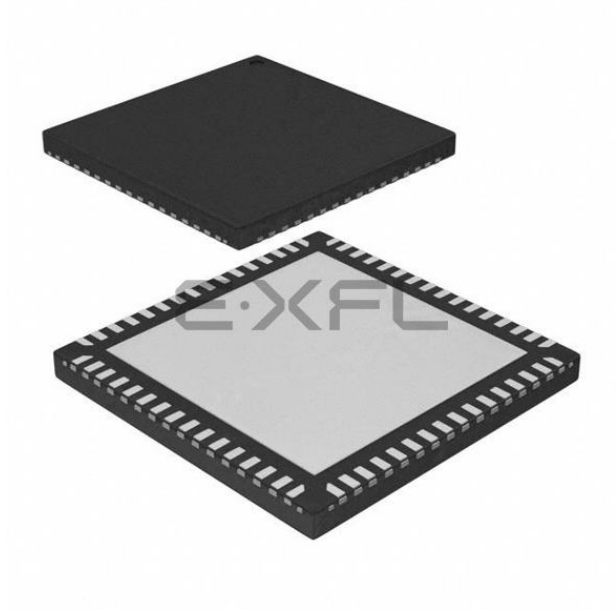

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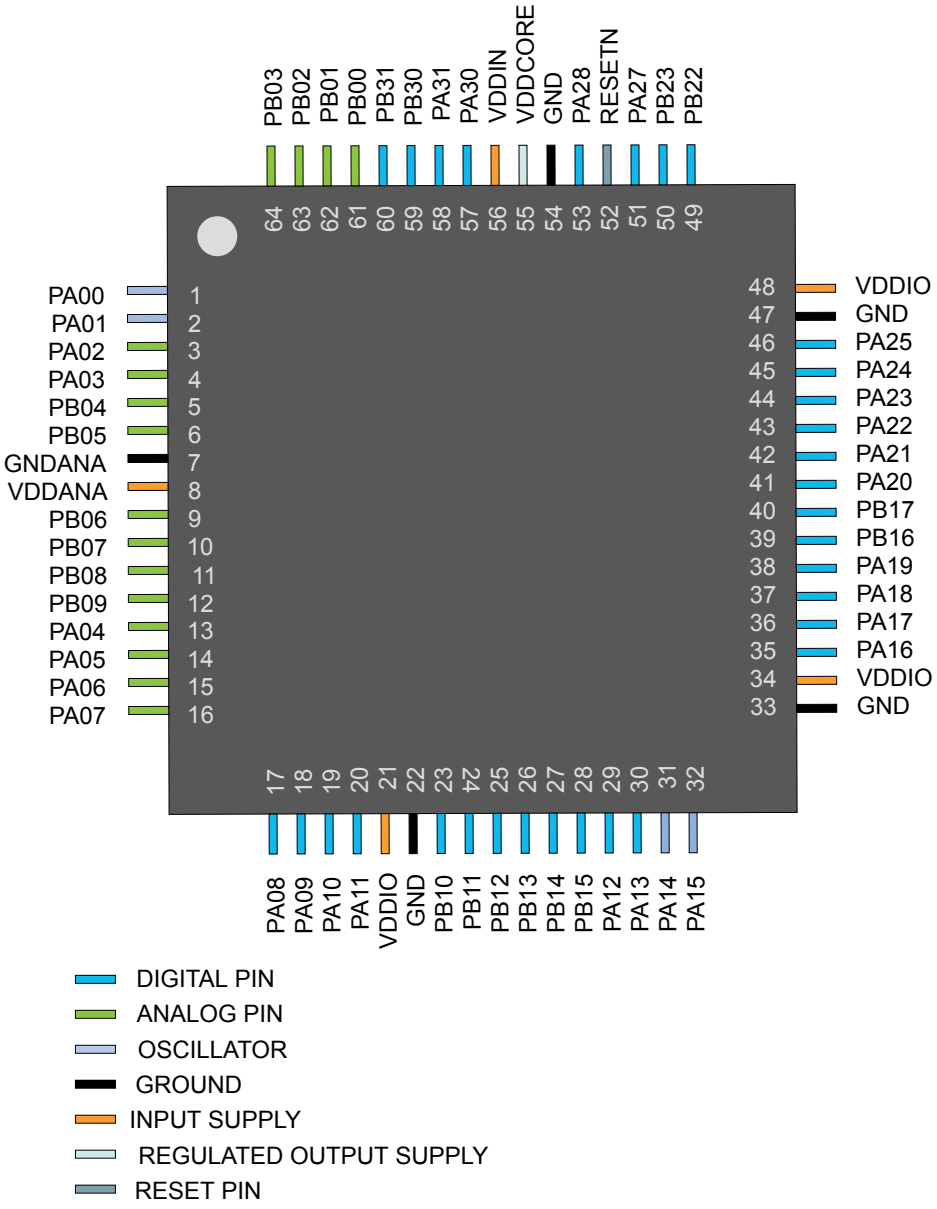
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, WDT
Number of I/O	52
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 20x12b, 3x16b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamc21j17a-mut

4.3 SAM C21J / SAM C20J

4.3.1 QFN64/TQFP64



9. Memories

9.1 Embedded Memories

- Internal high-speed Flash with read-while-write capability on section of the array
- Internal high-speed RAM, single-cycle access at full speed

9.2 Physical Memory Map

The High-Speed bus is implemented as a bus matrix. All High-Speed bus addresses are fixed, and they are never remapped in any way, even during boot. The 32-bit physical address space is mapped as follows:

Table 9-1. SAM C20/C21 Physical Memory Map(1)

Memory	Start address	Size	Size	Size	Size
		x18	x17	x16	x15
Embedded Flash	0x00000000	256Kbytes	128Kbytes	64Kbytes	32Kbytes
Embedded RWW section	0x00400000	8Kbytes	4Kbytes	2Kbytes	1Kbytes
Embedded high-speed SRAM	0x20000000	32Kbytes	16Kbytes	8Kbytes	4Kbytes
AHB-APB Bridge A	0x40000000	64Kbytes	64Kbytes	64Kbytes	64Kbytes
AHB-APB Bridge B	0x41000000	64Kbytes	64Kbytes	64Kbytes	64Kbytes
AHB-APB Bridge C	0x42000000	64Kbytes	64Kbytes	64Kbytes	64Kbytes
AHB-APB Bridge D	0x43000000	64Kbytes	-	-	-
AHB DIVAS	0x48000000	64Kbytes	64Kbytes	64Kbytes	64Kbytes
IOBUS	0x60000000	64Kbytes	64Kbytes	64Kbytes	64Kbytes

Note: 1. x = SAM C20/C21 G/J/E/N. The N-series (100-pin devices) does not include x16 and x15 option.

Table 9-2. SAM C20/C21 Flash Memory Parameters(1)

Device	Flash size (FLASH_PM)	Number of pages (FLASH_P)	Page size (FLASH_W)
x18	256Kbytes	4096	64 bytes
x17	128Kbytes	2048	64 bytes
x16	64Kbytes	1024	64 bytes
x15	32Kbytes	512	64 bytes

Note: 1. x = SAM C20/C21 G/J/E/N. The N-series (100-pin devices) does not include x16 and x15 option.

17.6.2.4 Selecting the Synchronous Clock Division Ratio

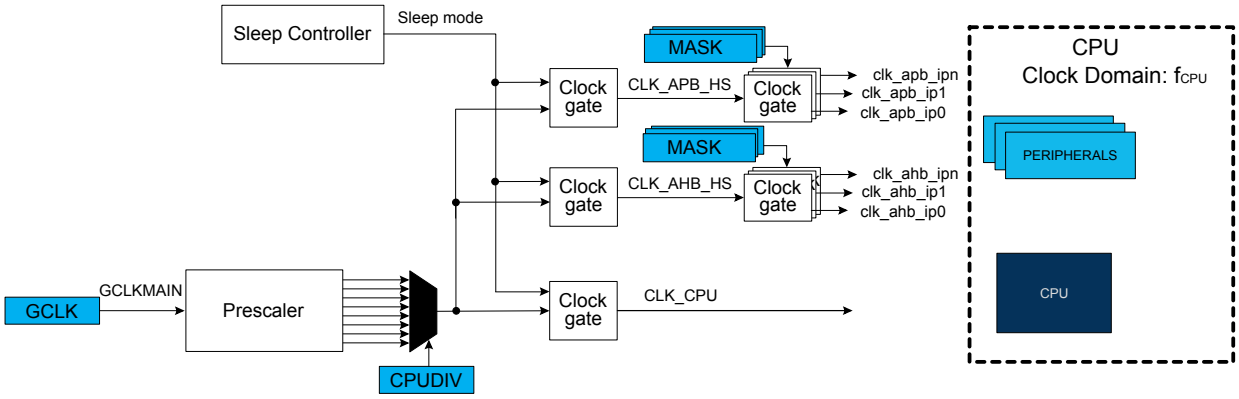
The main clock GCLK_MAIN feeds an 8-bit prescaler, which can be used to generate the synchronous clocks. By default, the synchronous clocks run on the undivided main clock. The user can select a prescaler division for the CPU clock domain by writing the Division (DIV) bits in the CPU Clock Division register CPUDIV, resulting in a CPU clock domain frequency determined by this equation:

$$f_{CPU} = \frac{f_{main}}{CPUDIV}$$

If the application attempts to write forbidden values in CPUDIV register, registers are written but these bad values are not used and a violation is reported to the PAC module.

Division bits (DIV) can be written without halting or disabling peripheral modules. Writing DIV bits allows a new clock setting to be written to all synchronous clocks belonging to the corresponding clock domain at the same time.

Figure 17-2. Synchronous Clock Selection and Prescaler



17.6.2.5 Clock Ready Flag

There is a slight delay between writing to CPUDIV until the new clock settings become effective.

During this interval, the Clock Ready flag in the Interrupt Flag Status and Clear register (INTFLAG.CKRDY) will return zero when read. If CKRDY in the INTENSET register is set to '1', the Clock Ready interrupt will be triggered when the new clock setting is effective. The clock settings (CLKCFG) must not be re-written while INTFLAG. CKRDY reads '0'. The system may become unstable or hang, and a violation is reported to the PAC module.

Related Links

PAC - Peripheral Access Controller

17.6.2.6 Peripheral Clock Masking

It is possible to disable/enable the AHB or APB clock for a peripheral by writing the corresponding bit in the Clock Mask registers (APBxMASK) to '0'/'1'. The default state of the peripheral clocks is shown here.

Table 17-1. Peripheral Clock Default State

CPU Clock Domain	
Peripheral Clock	**Default State**
CLK_AC_APB	Disabled
CLK_ADC0_APB	Disabled

20. OSCCTRL – Oscillators Controller

20.1 Overview

The Oscillators Controller (OSCCTRL) provides a user interface to the XOSC, OSC48M and FDPLL96M.

Through the interface registers, it is possible to enable, disable, calibrate, and monitor the OSCCTRL oscillators.

All oscillators statuses are collected in the Status register (STATUS). They can additionally trigger interrupts upon status changes via the INTENSET, INTENCLR, and INTFLAG registers.

Related Links

INTENCLR

INTENSET

INTFLAG

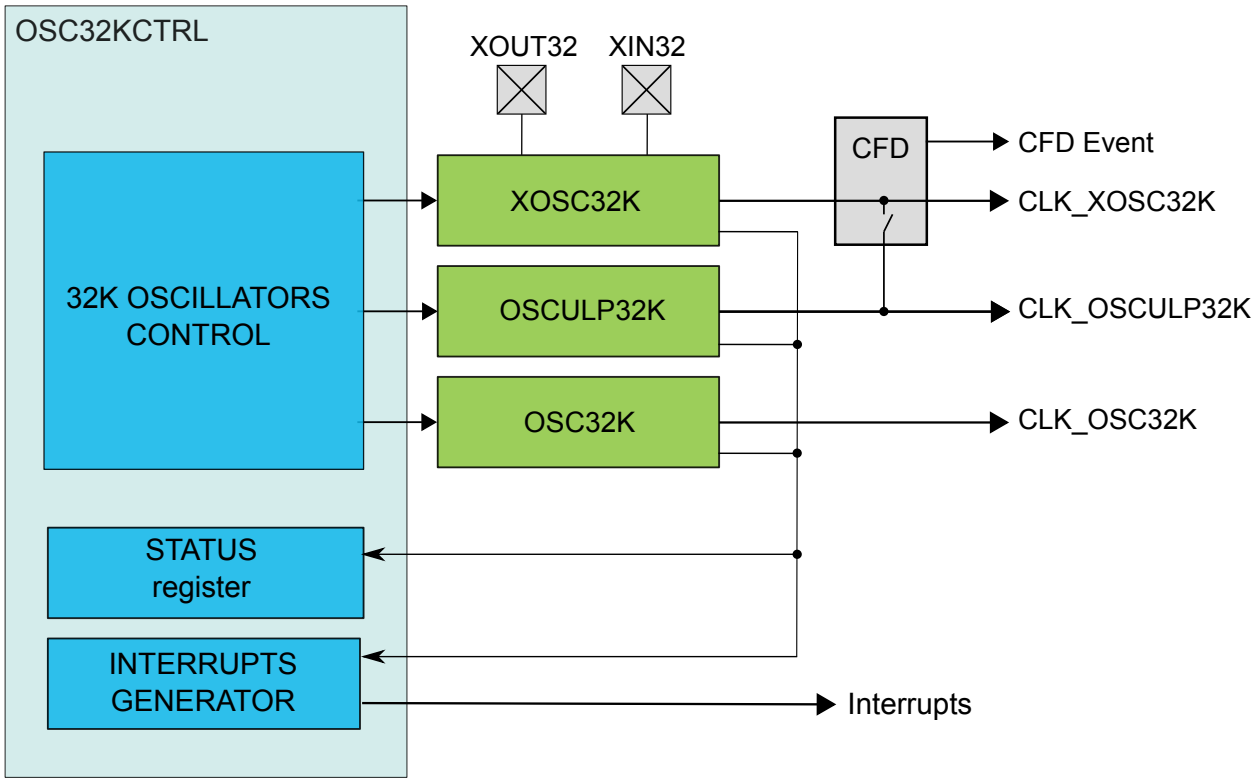
STATUS

20.2 Features

- 0.4-32MHz Crystal Oscillator (XOSC)
  - Tunable gain control
  - Programmable start-up time
  - Crystal or external input clock on XIN I/O
  - Clock failure detection with safe clock switch
  - Clock failure event output
- 48MHz Internal Oscillator (OSC48M)
  - Fast start-up
  - Programmable start-up time
  - 4-bit linear divider available
- Fractional Digital Phase Locked Loop (FDPLL96M)
  - 48MHz to 96MHz output frequency
  - 32kHz to 2MHz reference clock
  - A selection of sources for the reference clock
  - Adjustable proportional integral controller
  - Fractional part used to achieve 1/16th of reference clock step

21.3 Block Diagram

Figure 21-1. OSC32KCTRL Block Diagram



21.4 Signal Description

Signal	Description	Type
XIN32	Analog Input	32.768kHz Crystal Oscillator or external clock generator input
XOUT32	Analog Output	32.768kHz Crystal Oscillator output

The I/O lines are automatically selected when XOSC32K is enabled.

Note: The signal of the external crystal oscillator may affect the jitter of neighboring pads.

21.5 Product Dependencies

In order to use this peripheral, other parts of the system must be configured correctly, as described below.

21.5.1 I/O Lines

I/O lines are configured by OSC32KCTRL when XOSC32K is enabled, and need no user configuration.

21.5.2 Power Management

The OSC32KCTRL will continue to operate in any sleep mode where a 32KHz oscillator is running as source clock. The OSC32KCTRL interrupts can be used to wake up the device from sleep modes.

Related Links

PM – Power Manager

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
		CALIB[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
				WRTLOCK		STARTUP[2:0]		
Access				R/W		R/W	R/W	R/W
Reset				0		0	0	0

Bit	7	6	5	4	3	2	1	0
	ONDEMAND	RUNSTDBY			EN1K	EN32K	ENABLE	
Access	R/W	R/W			R/W	R/W	R/W	
Reset	1	0			0	0	0	

Bits 22:16 – CALIB[6:0]: Oscillator Calibration
These bits control the oscillator calibration. The calibration values must be loaded by the user from the NVM Software Calibration Area.

Bit 12 – WRTLOCK: Write Lock
This bit locks the OSC32K register for future writes, effectively freezing the OSC32K configuration.

Value	Description
0	The OSC32K configuration is not locked.
1	The OSC32K configuration is locked.

Bits 10:8 – STARTUP[2:0]: Oscillator Start-Up Time
These bits select start-up time for the oscillator.

The OSCULP32K oscillator is used as input clock to the start-up counter.

Table 21-4. Start-Up Time for 32KHz Internal Oscillator

STARTUP[2:0]	Number of OSC32K clock cycles	Approximate Equivalent Time [ms]
0x0	3	0.092
0x1	4	0.122
0x2	6	0.183
0x3	10	0.305
0x4	18	0.549
0x5	34	1.038
0x6	66	2.014
0x7	130	3.967

Name: CLOCK
Offset: 0x18
Reset: 0x00000000
Property: PAC Write-Protection, Write-Synchronized, Read-Synchronized

Bit	31	30	29	28	27	26	25	24
	YEAR[5:0]						MONTH[3:2]	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	MONTH[1:0]		DAY[4:0]					HOUR[4:4]
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	HOUR[3:0]				MINUTE[5:2]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	MINUTE[1:0]		SECOND[5:0]					
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:26 – YEAR[5:0]: Year
The year offset with respect to the reference year (defined in software).

The year is considered a leap year if YEAR[1:0] is zero.

Bits 25:22 – MONTH[3:0]: Month
1 – January

2 – February

...

12 – December

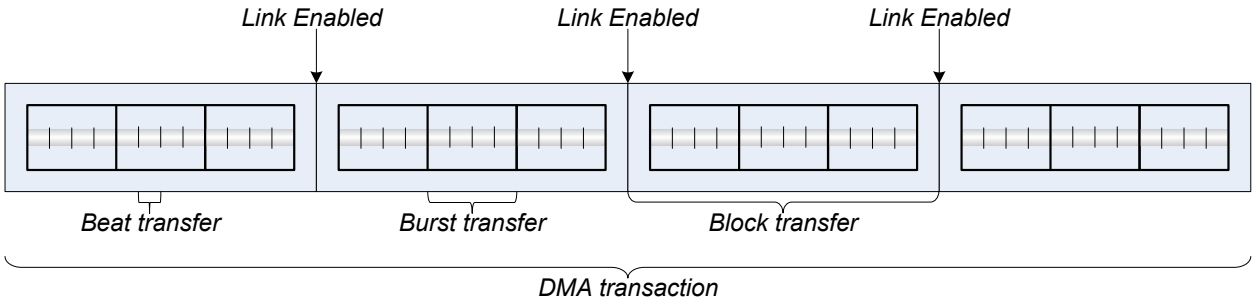
Bits 21:17 – DAY[4:0]: Day
Day starts at 1 and ends at 28, 29, 30, or 31, depending on the month and year.

Bits 16:12 – HOUR[4:0]: Hour
When CTRLA.CLKREP=0, the Hour bit group is in 24-hour format, with values 0-23. When CTRLA.CLKREP=1, HOUR[3:0] has values 1-12, and HOUR[4] represents AM (0) or PM (1).

Bits 11:6 – MINUTE[5:0]: Minute
0 – 59

Bits 5:0 – SECOND[5:0]: Second
0 – 59

Figure 25-2. DMA Transfer Sizes



- Beat transfer: The size of one data transfer bus access, and the size is selected by writing the Beat Size bit group in the Block Transfer Control register (BTCTRL.BEATSIZE)
- Burst transfer: Defined as n beat transfers, where n will differ from one device family to another. A burst transfer is atomic, cannot be interrupted and the length of the burst is selected by writing the Burst Length bit group in each Channel n Control A register (CHCTRLA.BURSTLEN).
- Block transfer: The amount of data one transfer descriptor can transfer, and the amount can range from 1 to 64k beats. A block transfer can be interrupted, in contrast to the burst transfer.
- Transaction: The DMAC can link several transfer descriptors by having the first descriptor pointing to the second and so forth, as shown in the figure above. A DMA transaction is the complete transfer of all blocks within a linked list.

A transfer descriptor describes how a block transfer should be carried out by the DMAC, and it must remain in SRAM. For further details on the transfer descriptor refer to Transfer Descriptors.

The figure above shows several block transfers linked together, which are called linked descriptors. For further information about linked descriptors, refer to Linked Descriptors.

A DMA transfer is initiated by an incoming transfer trigger on one of the DMA channels. This trigger can be configured to be either a software trigger, an event trigger, or one of the dedicated peripheral triggers. The transfer trigger will result in a DMA transfer request from the specific channel to the arbiter. If there are several DMA channels with pending transfer requests, the arbiter chooses which channel is granted access to become the active channel. The DMA channel granted access as the active channel will carry out the transaction as configured in the transfer descriptor. A current transaction can be interrupted by a higher prioritized channel after each burst transfer, but will resume the block transfer when the according DMA channel is granted access as the active channel again.

For each beat transfer, an optional output event can be generated. For each block transfer, optional interrupts and an optional output event can be generated. When a transaction is completed, dependent of the configuration, the DMA channel will either be suspended or disabled.

25.6.1.2 CRC

The internal CRC engine supports two commonly used CRC polynomials: CRC-16 (CRC-CCITT) and CRC-32 (IEEE 802.3). It can be used on a selectable DMA channel, or on the I/O interface. Refer to CRC Operation for details.

25.6.2 Basic Operation

25.6.2.1 Initialization

The following DMAC registers are enable-protected, meaning that they can only be written when the DMAC is disabled (CTRL.DMAENABLE=0):

- Descriptor Base Memory Address register (BASEADDR)
- Write-Back Memory Base Address register (WRBADDR)

Value	Name	Description
0x16	TCC1 MC0	TCC1 Match/Compare 0 Trigger
0x17	TCC1 MC1	TCC1 Match/Compare 1 Trigger
0x18	TCC2 OVF	TCC2 Overflow Trigger
0x19	TCC2 MC0	TCC2 Match/Compare 0 Trigger
0x1A	TCC2 MC1	TCC2 Match/Compare 1 Trigger
0x1B	TC0 OVF	TC0 Overflow Trigger
0x1C	TC0 MC0	TC0 Match/Compare 0 Trigger
0x1D	TC0 MC1	TC0 Match/Compare 1 Trigger
0x1E	TC1 OVF	TC1 Overflow Trigger
0x1F	TC1 MC0	TC1 Match/Compare 0 Trigger
0x20	TC1 MC1	TC1 Match/Compare 1 Trigger
0x21	TC2 OVF	TC2 Overflow Trigger
0x22	TC2 MC0	TC2 Match/Compare 0 Trigger
0x23	TC2 MC1	TC2 Match/Compare 1 Trigger
0x24	TC3 OVF	TC3 Overflow Trigger
0x25	TC3 MC0	TC3 Match/Compare 0 Trigger
0x26	TC3 MC1	TC3 Match/Compare 1 Trigger
0x27	TC4 OVF	TC4 Overflow Trigger
0x28	TC4 MC0	TC4 Match/Compare 0 Trigger
0x29	TC4 MC1	TC4 Match/Compare 1 Trigger
0x2A	ADC0 RESRDY	ADC0 Result Ready Trigger
0x2B	ADC1 RESRDY	ADC1 Result Ready Trigger
0x2C	SDADC RESRDY	SDADC Result Ready Trigger
0x2D	DAC EMPTY	DAC Empty Trigger
0x2E	PTC EOC	PTC End of Conversion Trigger
0x2F	PTC WCOMP	PTC Window Compare Trigger
0x30	PTC SEQ	PTC Sequence Trigger
0x31	SERCOM6 RX	SERCOM6 RX Trigger
0x32	SERCOM6 TX	SERCOM6 TX Trigger
0x33	SERCOM7 RX	SERCOM6 RX Trigger
0x34	SERCOM7 TX	SERCOM6 TX Trigger
0x35	TC5 OVF	TC5 Overflow Trigger

CMD[6:0]	Group Configuration	Description
0x48	UDR	Unlock Data Region - Unlocks the data region containing the address location in the ADDR register. When the Security Extension is enabled, only secure access can unlock secure regions.
0x47-0x7F	-	Reserved

27.8.2 Control B

Name: CTRLB
Offset: 0x04 [ID-00000b2c]
Reset: 0x00000080
Property: PAC Write-Protection

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
						CACHEDIS	READMODE[1:0]	
Access						R/W	R/W	R/W
Reset						0	0	0

Bit	15	14	13	12	11	10	9	8
							SLEEPPRM[1:0]	
Access							R/W	R/W
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	MANW			RWS[3:0]				
Access	R/W			R/W	R/W	R/W	R/W	
Reset	1			0	0	0	0	

Bit 18 – CACHEDIS: Cache Disable
This bit is used to disable the cache.

Value	Description
0	The cache is enabled
1	The cache is disabled

Bits 17:16 – READMODE[1:0]: NVMCTRL Read Mode

counter is stopped. At this moment, the 13 most significant bits of the counter (value divided by 8) give the new clock divider (BAUD.BAUD), and the 3 least significant bits of this value (the remainder) give the new Fractional Part (BAUD.FP).

When the Sync Field has been received, the clock divider (BAUD.BAUD) and the Fractional Part (BAUD.FP) are updated after a synchronization delay. After the Break and Sync Fields are received, multiple characters of data can be received.

31.6.3.5 LIN Master

LIN master is available with the following configuration:

- LIN master format (CTRLA.FORM = 0x02)
- Asynchronous mode (CTRLA.CMODE = 0)
- 16x sample rate using fractional baud rate generation (CTRLA.SAMPR = 1)

LIN frames start with a header transmitted by the master. The header consists of the break, sync, and identifier fields. After the master transmits the header, the addressed slave will respond with 1-8 bytes of data plus checksum.

Figure 31-12. LIN Frame Format

Using the LIN command field (CTRLB.LINCMD), the complete header can be automatically transmitted, or software can control transmission of the various header components.

When CTRLB.LINCMD=0x1, software controls transmission of the LIN header. In this case, software uses the following sequence.

- CTRLB.LINCMD is written to 0x1.
- DATA register written to 0x00. This triggers transmission of the break field by hardware. Note that writing the DATA register with any other value will also result in the transmission of the break field by hardware.
- DATA register written to 0x55. The 0x55 value (sync) is transmitted.
- DATA register written to the identifier. The identifier is transmitted.

When CTRLB.LINCMD=0x2, hardware controls transmission of the LIN header. In this case, software uses the following sequence.

- CTRLB.LINCMD is written to 0x2.
- DATA register written to the identifier. This triggers transmission of the complete header by hardware. First the break field is transmitted. Next, the sync field is transmitted, and finally the identifier is transmitted.

In LIN master mode, the length of the break field is programmable using the break length field (CTRLC.BRKLEN). When the LIN header command is used (CTRLB.LINCMD=0x2), the delay between the break and sync fields, in addition to the delay between the sync and ID fields are configurable using the header delay field (CTRLC.HDRDLY). When manual transmission is used (CTRLB.LINCMD=0x1), software controls the delay between break and sync.

Name: PSR
Offset: 0x44 [ID-0000a4bb]
Reset: 0x00000707
Property: Read-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
		TDCV[6:0]						
Access		R	R	R	R	R	R	R
Reset		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
		PXE	RFDF	RBRS	RESI	DLEC[2:0]		
Access		R	R	R	R	R	R	R
Reset		0	0	0	0	1	1	1

Bit	7	6	5	4	3	2	1	0
	BO	EW	EP	ACT[1:0]		LEC[2:0]		
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	1	1	1

Bits 22:16 – TDCV[6:0]: Transmitter Delay Compensation Value

Value	Description
0x00 - 0x7F	Position of the secondary sample point, defined by the sum of the measured delay from CAN_TX to CAN_RX and TDCR.TDCO. The SSP position is, in the data phase, the number of mtq between the start of the transmitted bit and the secondary sample point. Valid values are 0 to 127 mtq.

Bit 14 – PXE: Protocol Exception Event
This field is cleared on read access.

Value	Description
0	No protocol exception event occurred since last read access.
1	Protocol exception event occurred.

Bit 13 – RFDF: Received a CAN FD Message
This field is cleared on read access.

Value	Description
0	Since this bit was reset by the CPU, no CAN FD message has been received.
1	Message in CAN FD format with FDF flag set has been received. This bit is set independent of acceptance filtering.

Bit 12 – RBRS: BRS flag of last received CAN FD Message
This field is cleared on read access.

Bit	31	30	29	28	27	26	25	24
	CFn	CFn	CFn	CFn	CFn	CFn	CFn	CFn
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	CFn	CFn	CFn	CFn	CFn	CFn	CFn	CFn
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CFn	CFn	CFn	CFn	CFn	CFn	CFn	CFn
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CFn	CFn	CFn	CFn	CFn	CFn	CFn	CFn
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – CFn: Cancellation Finished
Each Tx Buffer has its own Cancellation Finished bit.

The bits are set when the corresponding TXBRP bit is cleared after a cancellation was requested via TXBCR. In case the corresponding TXBRP bit was not set at the point of cancellation, CF is set immediately.

The bits are reset when a new transmission is requested by writing ‘1’ to the corresponding bit of register TXBAR.

34.8.43 Tx Buffer Transmission Interrupt Enable

Name: TXBTIE
Offset: 0xE0 [ID-0000a4bb]
Reset: 0x00000000
Property: -

This bit field has a different meaning depending on the configuration of EFEC.
1) EFEC = “001” ... “110” Second ID of standard ID filter element.
2) EFEC = “111” Filter for Rx Buffers or for debug messages.

EFID2[10:9] decides whether the received message is stored into an Rx Buffer or treated as message A, B, or C of the debug message sequence.

00 = Store message into an Rx Buffer

01 = Debug Message A

10 = Debug Message B

11 = Debug Message C

EFID2[8:6] is used to control the filter event pins at the Extension Interface. A ‘1’ at the respective bit position enables generation of a pulse at the related filter event pin with the duration of one CLK_CAN_APB period in case the filter matches.

EFID2[5:0] defines the offset to the Rx Buffer Start Address RXBC.RBSA for storage of a matching message.

Bit	7	6	5	4	3	2	1	0
							WAVEGEN[1:0]	
Access							R/W	R/W
Reset							0	0

Bits 1:0 – WAVEGEN[1:0]: Waveform Generation Mode
These bits select the waveform generation operation. They affect the top value, as shown in Waveform Output Operations. They also control whether frequency or PWM waveform generation should be used. The waveform generation operations are explained in Waveform Output Operations.

These bits are not synchronized.

Value	Name	Operation	Top Value	Output Waveform on Match	Output Waveform on Wraparound
0x0	NFRQ	Normal frequency	PER[1] / Max	Toggle	No action
0x1	MFRQ	Match frequency	CC0	Toggle	No action
0x2	NPWM	Normal PWM	PER[1] / Max	Set	Clear
0x3	MPWM	Match PWM	CC0	Set	Clear

1) This depends on the TC mode: In 8-bit mode, the top value is the Period Value register (PER). In 16- and 32-bit mode it is the respective MAX value.

35.7.1.10 Driver Control

Name: DRVCTRL
Offset: 0x0D
Reset: 0x00
Property: PAC Write-Protection, Enable-Protected

Bit	7	6	5	4	3	2	1	0
								INVENx
Access								R/W
Reset								0

Bit 0 – INVENx: Output Waveform x Invert Enable
Bit x of INVEN[1:0] selects inversion of the output or capture trigger input of channel x.

Value	Description
0	Disable inversion of the WO[x] output and IO input pin.
1	Enable inversion of the WO[x] output and IO input pin.

35.7.1.11 Debug Control

Value	Name	Description
0x2	FALL	Blanking applied from falling edge of the waveform output
0x3	BOTH	Blanking applied from each toggle of the waveform output

Bit 4 – QUAL: Recoverable Fault n Qualification
Setting this bit enables the recoverable Fault n input qualification.

Value	Description
0	The recoverable Fault n input is not disabled on CMPx value condition.
1	The recoverable Fault n input is disabled when output signal is at inactive level (CMPx == 0).

Bit 3 – KEEP: Recoverable Fault n Keep
Setting this bit enables the Fault n keep action.

Value	Description
0	The Fault n state is released as soon as the recoverable Fault n is released.
1	The Fault n state is released at the end of TCC cycle.

Bits 1:0 – SRC[1:0]: Recoverable Fault n Source
These bits select the TCC event input for recoverable Fault n.

Event system channel connected to MCEx event input, must be configured to route the event asynchronously, when used as a recoverable Fault n input.

Value	Name	Description
0x0	DISABLE	Fault input disabled
0x1	ENABLE	MCEx (x=0,1) event input
0x2	INVERT	Inverted MCEx (x=0,1) event input
0x3	ALTFAULT	Alternate fault (A or B) state at the end of the previous period.

36.8.6 Waveform Extension Control

Name: WEXCTRL
Offset: 0x14 [ID-00002e48]
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected

Value	Description
0x2	4 samples
0x3	8 samples
0x4	16 samples
0x5	32 samples
0x6	64 samples
0x7	128 samples
0x8	256 samples
0x9	512 samples
0xA	1024 samples
0xB - 0xF	Reserved

38.8.12 Sampling Time Control

Name: SAMPCTRL
Offset: 0x0D [ID-0000120e]
Reset: 0x00
Property: PAC Write-Protection, Write-Synchronized

Bit	7	6	5	4	3	2	1	0
	OFFCOMP		SAMPLEN[5:0]					
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0		0	0	0	0	0	0

Bit 7 – OFFCOMP: Comparator Offset Compensation Enable
Setting this bit enables the offset compensation for each sampling period to ensure low offset and immunity to temperature or voltage drift. This compensation increases the sampling time by three clock cycles.

This bit must be set to zero to validate the SAMPLEN value. It's not possible to use OFFCOMP=1 and SAMPLEN>0.

Bits 5:0 – SAMPLEN[5:0]: Sampling Time Length
These bits control the ADC sampling time in number of CLK_ADC cycles, depending of the prescaler value, thus controlling the ADC input impedance. Sampling time is set according to the equation:

$$\text{Sampling time} = (\text{SAMPLEN}+1) \cdot \left(\text{CLK}_{\text{ADC}}\right)$$

38.8.13 Window Monitor Lower Threshold

Name: WINLT
Offset: 0x0E [ID-0000120e]
Reset: 0x0000
Property: PAC Write-Protection, Write-Synchronized

43.7 Register Summary

Offset	Name	Bit Pos.								
0x00	CTRLA	7:0		RUNSTDBY					ENABLE	SWRST
0x01	CTRLB	7:0								START
0x02	CTRLC	7:0				FREERUN		WINMODE[2:0]		
0x03	EVCTRL	7:0						WINEO	STARTINV	STARTEI
0x04	INTENCLR	7:0					OVF	WINMON	OVERRUN	RESRDY
0x05	INTENSET	7:0					OVF	WINMON	OVERRUN	RESRDY
0x06	INTFLAG	7:0					OVF	WINMON	OVERRUN	RESRDY
0x07	STATUS	7:0								OVF
0x08	SYNCBUSY	7:0							ENABLE	SWRST
0x09		15:8								
0x0A		23:16								
0x0B		31:24								
0x0C	VALUE	7:0	VALUE[7:0]							
0x0D		15:8	VALUE[15:8]							
0x0E		23:16	VALUE[23:16]							
0x0F		31:24								
0x10	WINLT	7:0	WINLT[7:0]							
0x11		15:8	WINLT[15:8]							
0x12		23:16	WINLT[23:16]							
0x13		31:24								
0x14	WINUT	7:0	WINUT[7:0]							
0x15		15:8	WINUT[15:8]							
0x16		23:16	WINUT[23:16]							
0x17		31:24								
0x18	GAIN	7:0	GAIN[7:0]							
0x19		15:8	GAIN[15:8]							
0x1A		23:16	GAIN[23:16]							
0x1B		31:24								
0x1C	OFFSET	7:0	OFFSETC[7:0]							
0x1D		15:8	OFFSETC[15:8]							
0x1E		23:16	OFFSETC[23:16]							
0x1F		31:24								
0x20	CAL	7:0			FCAL[5:0]					
0x21		15:8			TCAL[5:0]					
0x22		23:16								
0x23		31:24								
0x24	DBGCTRL	7:0								DBGRUN

43.8 Register Description

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16-, and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly.

NVM erase operations are not protected by the BODVDD and BODCORE in debugger cold-plugging mode. NVM erase operation at supply voltages below product specification minimum can cause corruption of the calibration and other areas mandatory for a correct product behavior.

Table 45-2. General operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{DDIN}	Power supply voltage	2.7(1)	5.0	5.5	V
V_{DDANA}	Analog supply voltage	2.7(1)	5.0	5.5	V
V_{DDIO}	IO supply voltage	2.7(1)	5.0	5.5	V
T_A	Temperature range	-40	25	85	°C
T_J	Junction temperature	-	-	100	°C

1. With BODVDD disabled. If the BODVDD is enabled, refer to Table 45-14

Note:
The same voltage must be applied to VDDIN and VDDANA. VDDIO should be lower or equal to VDDIN / VDDANA. The common voltage is referred to as VDD in the datasheet.

Some I/O are in the VDDIO cluster, but can be multiplexed as analog outputs (e.g. PTC.X[n] pads). In such a case, VDDANA is used to power the I/O. Using this configuration may result in an electrical conflict if the VDDIO voltage is lower than the VDDIN/VDDANA.

Related Links

Brown Out Detectors Characteristics

45.4 Injection Current

Stresses beyond those listed in the table below may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 45-3. Injection Current(1)

Symbol	Description	min	max	Unit
I_{INJ1}(2)	IO pin injection current	-1	+1	mA
I_{INJ2}(3)	IO pin injection current	-15	+15	mA
$I_{INJtotal}$	Sum of IO pins injection current	-45	+45	mA

1. Injecting current may have an effect on the accuracy of the analog blocks.
2. Conditions for V_{PIN}: V_{PIN}<GND-0.6V or 5.5V<V_{PIN}<=6.1V.

   Conditions for VDD 4.9V<VDD<=5.5V.

   If Vpin is lower than GND-0.6V, then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as R = |(GND-0.6V – V_{PIN})/I_{INJ1}|. If Vpin is greater than VDD+0.6V, then a current limiting resistor is required. The positive DC injection current limiting resistor is calculated as R = (V_{PIN}-(VDD+0.6))/I_{INJ1}.
3. Conditions for V_{PIN}: V_{PIN}<GND-0.6V or V_{PIN}<=5.5V.

Table 45-12. I/O Pins Dynamic Characteristics (1)

Symbol	Parameter	Conditions	Normal pins	High Sink pins	Normal pins	High Sink pins	Units
			DRVSTR=0		DRVSTR=1		
t_{RISE}	Maximum rise time	VDD = 5.0V, load = 20pF	15	12	8	7	ns
t_{FALL}	Maximum fall time	VDD = 5.0V, load = 20pF	14	11	7	7	

1. These values are based on simulation. These values are not covered by test limits in production or characterization.
2. The following pins are High Sink pins and have different properties than normal pins: PA10, PA11, PB10, PB11.

Related Links

I/O Multiplexing and Considerations

PINCFG

45.10 Analog Characteristics

45.10.1 POR - Power On Reset Characteristics

Table 45-13. POR Characteristics

Symbol	Parameters	Min	Typ	Max	Unit
V_{POT+}	Voltage threshold Level on Vddin rising	-	2.55	-	V
V_{POT-}	Voltage threshold Level on Vddin falling	1.53	1.75	1.97	