

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	40 MIPs
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 18x10b, 18x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24hj256gp206t-i-pt

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Communication Modules:

- 3-wire SPI (up to two modules):
 - Framing supports I/O interface to simple codecs
 - Supports 8-bit and 16-bit data
 - Supports all serial clock formats and sampling modes
- I²C[™] (up to two modules):
 - Full Multi-Master Slave mode support
 - 7-bit and 10-bit addressing
 - Bus collision detection and arbitration
 - Integrated signal conditioning
 - Slave address masking
- UART (up to two modules):
 - Interrupt on address bit detect
 - Interrupt on UART error
 - Wake-up on Start bit from Sleep mode
 - 4-character TX and RX FIFO buffers
 - LIN bus support
 - $\ensuremath{\text{IrDA}}\xspace^{\ensuremath{\mathbb{R}}}$ encoding and decoding in hardware
 - High-Speed Baud mode
 - Hardware Flow Control with CTS and RTS
- Enhanced CAN (ECAN™ module) 2.0B active (up to two modules):
 - Up to eight transmit and up to 32 receive buffers
 - 16 receive filters and 3 masks
 - Loopback, Listen Only and Listen All Messages modes for diagnostics and bus monitoring
 - Wake-up on CAN message
 - Automatic processing of Remote Transmission Requests
 - FIFO mode using DMA
 - DeviceNet[™] addressing support

Analog-to-Digital Converters:

- Up to two Analog-to-Digital Converter (ADC) modules in a device
- 10-bit, 1.1 Msps or 12-bit, 500 ksps conversion:
 Two, four, or eight simultaneous samples
 - Up to 32 input channels with auto-scanning
 - Conversion start can be manual or synchronized with one of four trigger sources
 - Conversion possible in Sleep mode
 - ±1 LSb max integral nonlinearity
 - ±1 LSb max differential nonlinearity

CMOS Flash Technology:

- · Low-power, high-speed Flash technology
- · Fully static design
- 3.3V (±10%) operating voltage
- · Industrial temperature
- Low-power consumption

Packaging:

- 100-pin TQFP (14x14x1 mm and 12x12x1 mm)
- 64-pin TQFP (10x10x1 mm)

Note: See the device variant tables for exact peripheral features per device.

Pin Diagrams (Continued)



Pin Diagrams (Continued)



SR: CPU STATUS REGISTER **REGISTER 3-1:** U-0 U-0 U-0 U-0 U-0 U-0 U-0 R/W-0 DC bit 15 bit 8 R/W-0⁽¹⁾ R/W-0⁽²⁾ R/W-0⁽²⁾ R-0 R/W-0 R/W-0 R/W-0 R/W-0 IPL<2:0>(2) RA Ν OV Ζ С bit 7 bit 0 Leaend: C = Clear only bit U = Unimplemented bit, read as '0' R = Readable bit S = Set only bit W = Writable bit -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown bit 15-9 Unimplemented: Read as '0' bit 8 DC: MCU ALU Half Carry/Borrow bit 1 = A carry-out from the 4th low-order bit (for byte sized data) or 8th low-order bit (for word sized data) of the result occurred 0 = No carry-out from the 4th low-order bit (for byte sized data) or 8th low-order bit (for word sized data) of the result occurred IPL<2:0>: CPU Interrupt Priority Level Status bits⁽²⁾ bit 7-5 111 = CPU Interrupt Priority Level is 7 (15), user interrupts disabled 110 = CPU Interrupt Priority Level is 6 (14) 101 = CPU Interrupt Priority Level is 5 (13) 100 = CPU Interrupt Priority Level is 4 (12) 011 = CPU Interrupt Priority Level is 3 (11) 010 = CPU Interrupt Priority Level is 2 (10) 001 = CPU Interrupt Priority Level is 1 (9) 000 = CPU Interrupt Priority Level is 0 (8) bit 4 **RA:** REPEAT Loop Active bit 1 = REPEAT loop in progress 0 = REPEAT loop not in progress bit 3 N: MCU ALU Negative bit 1 = Result was negative 0 = Result was non-negative (zero or positive) bit 2 OV: MCU ALU Overflow bit This bit is used for signed arithmetic (2's complement). It indicates an overflow of the magnitude which causes the sign bit to change state. 1 = Overflow occurred for signed arithmetic (in this arithmetic operation) 0 = No overflow occurred Z: MCU ALU Zero bit bit 1 1 = An operation which affects the Z bit has set it at some time in the past 0 = The most recent operation which affects the Z bit has cleared it (i.e., a non-zero result) bit 0 C: MCU ALU Carry/Borrow bit 1 = A carry-out from the Most Significant bit (MSb) of the result occurred 0 = No carry-out from the Most Significant bit of the result occurred Note 1: The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL if IPL<3> = 1. User interrupts are disabled when IPL<3> = 1.

2: The IPL<2:0> Status bits are read only when NSTDIS = 1 (INTCON1<15>).



4.2.6 SOFTWARE STACK

In addition to its use as a working register, the W15 register in the PIC24HJXXXGPX06/X08/X10 devices is also used as a software Stack Pointer. The Stack Pointer always points to the first available free word and grows from lower to higher addresses. It pre-decrements for stack pops and post-increments for stack pushes, as shown in Figure 4-5. For a PC push during any CALL instruction, the MSB of the PC is zero-extended before the push, ensuring that the MSB is always clear.

Note:	A PC push during exception processing						
	concatenates the SRL register to the MSB						
	of the PC prior to the push.						

The Stack Pointer Limit register (SPLIM) associated with the Stack Pointer sets an upper address boundary for the stack. SPLIM is uninitialized at Reset. As is the case for the Stack Pointer, SPLIM<0> is forced to '0' because all stack operations must be word-aligned. Whenever an EA is generated using W15 as a source or destination pointer, the resulting address is compared with the value in SPLIM. If the contents of the Stack Pointer (W15) and the SPLIM register are equal and a push operation is performed, a stack error trap will not occur. The stack error trap will occur on a subsequent push operation. Thus, for example, if it is desirable to cause a stack error trap when the stack grows beyond address 0x2000 in RAM, initialize the SPLIM with the value 0x1FFE.

Similarly, a Stack Pointer underflow (stack error) trap is generated when the Stack Pointer address is found to be less than 0x0800. This prevents the stack from interfering with the Special Function Register (SFR) space.

A write to the SPLIM register should not be immediately followed by an indirect read operation using W15.





4.2.7 DATA RAM PROTECTION FEATURE

The PIC24H product family supports Data RAM protection features that enable segments of RAM to be protected when used in conjunction with Boot and Secure Code Segment Security. BSRAM (Secure RAM segment for BS) is accessible only from the Boot Segment Flash code, when enabled. SSRAM (Secure RAM segment for RAM) is accessible only from the Secure Segment Flash code, when enabled. See Table 4-1 for an overview of the BSRAM and SSRAM SFRs.

4.3 Instruction Addressing Modes

The addressing modes in Table 4-34 form the basis of the addressing modes optimized to support the specific features of individual instructions. The addressing modes provided in the MAC class of instructions are somewhat different from those in the other instruction types.

4.3.1 FILE REGISTER INSTRUCTIONS

Most file register instructions use a 13-bit address field (f) to directly address data present in the first 8192 bytes of data memory (Near Data Space). Most file register instructions employ a working register, W0, which is denoted as WREG in these instructions. The destination is typically either the same file register or WREG (with the exception of the MUL instruction), which writes the result to a register or register pair. The MOV instruction allows additional flexibility and can access the entire data space.

4.3.2 MCU INSTRUCTIONS

The 3-operand MCU instructions are of the form:

Operand 3 = Operand 1 < function> Operand 2

where Operand 1 is always a working register (i.e., the addressing mode can only be Register Direct) which is referred to as Wb. Operand 2 can be a W register, fetched from data memory, or a 5-bit literal. The result location can be either a W register or a data memory location. The following addressing modes are supported by MCU instructions:

- Register Direct
- · Register Indirect
- · Register Indirect Post-Modified
- Register Indirect Pre-Modified
- 5-bit or 10-bit Literal

Note:	Not	all	instructions	support	all	the	
	addressing modes given above. Individual						
	instructions may support different subsets						
	of these addressing modes.						

REGISTER 7-8: IFS3: INTERRUPT FLAG STATUS REGISTER 3

U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	R/W-0	
	_	DMA5IF	—	_	_	—	C2IF	
bit 15				•			bit 8	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
C2RXIF	INT4IF	INT3IF	T9IF	T8IF	MI2C2IF	SI2C2IF	T7IF	
bit 7							bit 0	
Lananda								
Legena:	hit	M = M/ritable	hit	II – Unimplor	montod bit road	as 'O'		
n = Value at P		'1' = Bit is set	UIL	0° – Onimplet	nenteu bit, reau	as u v = Bit is unkr		
	UK	I - DILISSEL			aleu		IOWII	
bit 15-14	Unimplemen	ted: Read as ')'					
bit 13	DMA5IF: DM	A Channel 5 Da	ata Transfer C	omplete Interr	upt Flag Status	bit		
	1 = Interrupt r	equest has occ	curred	- F				
	0 = Interrupt r	request has not	occurred					
bit 12-9	Unimplemen	ted: Read as 'o)'					
bit 8	C2IF: ECAN2	Event Interrup	t Flag Status I	bit				
	1 = Interrupt r	equest has occ	concurred					
bit 7	C2RXIE: ECA	N2 Receive D	ata Ready Inte	errunt Flag Sta	tus bit			
Sit	1 = Interrupt r	request has occ	curred	indpir lag old				
	0 = Interrupt r	equest has not	occurred					
bit 6	INT4IF: Exter	nal Interrupt 4	Flag Status bit	t				
	1 = Interrupt r	equest has occ	curred					
h:+ F	0 = Interrupt r	request has not	Coccurred	L L				
	1 = Interrupt r	nai interrupt 3	Flag Status Di	L				
	0 = Interrupt r	request has not	occurred					
bit 4	T9IF: Timer9	Interrupt Flag S	Status bit					
	1 = Interrupt r	equest has occ	curred					
	0 = Interrupt r	equest has not	occurred					
bit 3	T8IF: Timer8	Interrupt Flag S	Status bit					
	<pre>1 = Interrupt r 0 = Interrupt r</pre>	request has occ	currea					
bit 2	MI2C2IF: 12C	2 Master Even	ts Interrupt Fla	ag Status bit				
	1 = Interrupt r	equest has occ	curred	0				
	 Interrupt request has not occurred 							
bit 1	SI2C2IF: 12C2	2 Slave Events	Interrupt Flag	Status bit				
	1 = Interrupt r	equest has occ	curred					
hit 0	T7IF · Timer7	Interrunt Flag	Status hit					
Situ	1 = nterrupt r	request has occ	curred					
	0 = Interrupt r	request has not	occurred					



8.1 DMAC Registers

Each DMAC Channel x (x = 0, 1, 2, 3, 4, 5, 6 or 7) contains the following registers:

- A 16-bit DMA Channel Control register (DMAxCON)
- A 16-bit DMA Channel IRQ Select register (DMAxREQ)
- A 16-bit DMA RAM Primary Start Address Offset register (DMAxSTA)
- A 16-bit DMA RAM Secondary Start Address Offset register (DMAxSTB)
- A 16-bit DMA Peripheral Address register (DMAxPAD)
- A 10-bit DMA Transfer Count register (DMAxCNT)

An additional pair of status registers, DMACS0 and DMACS1 are common to all DMAC channels.

REGISTER 8-9: DSADR: MOST RECENT DMA RAM ADDRESS

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
			DSAE)R<15:8>			
bit 15							bit 8
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
			DSA	DR<7:0>			
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'				d as '0'			
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is clea	red	x = Bit is unkno	own

bit 15-0 DSADR<15:0>: Most Recent DMA RAM Address Accessed by DMA Controller bits

13.0 TIMER2/3, TIMER4/5, TIMER6/7 AND TIMER8/9

Note:	This data sheet summarizes the features of the PIC24HJXXXGPX06/X08/X10 fam- ily of devices. However, it is not intended
	to be a comprehensive reference source.
	sheet, refer to the "PIC24H Family Refer-
	ence Manual", Section 11. "Timers"
	(DS70244), which is available from the
	Microchip website (www.microchip.com).

The Timer2/3, Timer4/5, Timer6/7 and Timer8/9 modules are 32-bit timers, which can also be configured as four independent 16-bit timers with selectable operating modes.

As a 32-bit timer, Timer2/3, Timer4/5, Timer6/7 and Timer8/9 operate in three modes:

- Two Independent 16-bit Timers (e.g., Timer2 and Timer3) with all 16-bit operating modes (except Asynchronous Counter mode)
- Single 32-bit Timer
- Single 32-bit Synchronous Counter

They also support these features:

- Timer Gate Operation
- Selectable Prescaler Settings
- · Timer Operation during Idle and Sleep modes
- Interrupt on a 32-bit Period Register Match
- Time Base for Input Capture and Output Compare Modules (Timer2 and Timer3 only)
- ADC1 Event Trigger (Timer2/3 only)
- ADC2 Event Trigger (Timer4/5 only)

Individually, all eight of the 16-bit timers can function as synchronous timers or counters. They also offer the features listed above, except for the event trigger; this is implemented only with Timer2/3. The operating modes and enabled features are determined by setting the appropriate bit(s) in the T2CON, T3CON, T4CON, T5CON, T6CON, T7CON, T8CON and T9CON registers. T2CON, T4CON, T6CON and T8CON are shown in generic form in Register 13-1. T3CON, T5CON, T7CON and T9CON are shown in Register 13-2. For 32-bit timer/counter operation, Timer2, Timer4, Timer6 or Timer8 is the least significant word; Timer3, Timer5, Timer7 or Timer9 is the most significant word of the 32-bit timers.

Note:	For 32-bit operation, T3CON, T5CON,
	T7CON and T9CON control bits are
	ignored. Only T2CON, T4CON, T6CON
	and T8CON control bits are used for setup
	and control. Timer2, Timer4, Timer6 and
	Timer8 clock and gate inputs are utilized
	for the 32-bit timer modules, but an inter-
	rupt is generated with the Timer3, Timer5,
	Ttimer7 and Timer9 interrupt flags.

To configure Timer2/3, Timer4/5, Timer6/7 or Timer8/9 for 32-bit operation:

- 1. Set the corresponding T32 control bit.
- 2. Select the prescaler ratio for Timer2, Timer4, Timer6 or Timer8 using the TCKPS<1:0> bits.
- 3. Set the Clock and Gating modes using the corresponding TCS and TGATE bits.
- 4. Load the timer period value. PR3, PR5, PR7 or PR9 contains the most significant word of the value, while PR2, PR4, PR6 or PR8 contains the least significant word.
- If interrupts are required, set the interrupt enable bit, T3IE, T5IE, T7IE or T9IE. Use the priority bits, T3IP<2:0>, T5IP<2:0>, T7IP<2:0> or T9IP<2:0>, to set the interrupt priority. While Timer2, Timer4, Timer6 or Timer8 control the timer, the interrupt appears as a Timer3, Timer5, Timer7 or Timer9 interrupt.
- 6. Set the corresponding TON bit.

The timer value at any point is stored in the register pair, TMR3:TMR2, TMR5:TMR4, TMR7:TMR6 or TMR9:TMR8. TMR3, TMR5, TMR7 or TMR9 always contains the most significant word of the count, while TMR2, TMR4, TMR6 or TMR8 contains the least significant word.

To configure any of the timers for individual 16-bit operation:

- 1. Clear the T32 bit corresponding to that timer.
- Select the timer prescaler ratio using the TCKPS<1:0> bits.
- 3. Set the Clock and Gating modes using the TCS and TGATE bits.
- 4. Load the timer period value into the PRx register.
- 5. If interrupts are required, set the interrupt enable bit, TxIE. Use the priority bits, TxIP<2:0>, to set the interrupt priority.
- 6. Set the TON bit.

REGISTER 19-15: CIBUFPNT4: ECAN™ MODULE FILTER 12-15 BUFFER POINTER REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
	F15B	P<3:0>			F14E	3P<3:0>		
bit 15							bit 8	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
	F13B	P<3:0>			F12E	3P<3:0>		
bit 7				•			bit 0	
Legend:								
R = Readabl	e bit	W = Writable	bit	U = Unimplemented bit, read as '0'				
-n = Value at POR '1' = Bit is set			'0' = Bit is cle	ared	x = Bit is unki	nown		
bit 15-12	F15BP<3:0>: RX Buffer Written when Filter 15 Hits bits							
bit 11-8	F14BP<3:0>: RX Buffer Written when Filter 14 Hits bits							
bit 7-4	-4 F13BP<3:0>: RX Buffer Written when Filter 13 Hits bits							

bit 3-0 F12BP<3:0>: RX Buffer Written when Filter 12 Hits bits

REGISTER 19-20: CIRXMnSID: ECAN™ MODULE ACCEPTANCE FILTER MASK n STANDARD IDENTIFIER

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3
bit 15			•		•	•	bit 8
R/W-x	R/W-x	R/W-x	U-0	R/W-x	U-0	R/W-x	R/W-x
SID2	SID1	SID0	—	MIDE	_	EID17	EID16
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	d as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unki	nown
bit 15-5	SID<10:0>: \$	Standard Identi	fier bits				
	1 = Include bi 0 = Bit SIDx i	it SIDx in filter o s don't care in f	comparison filter comparis	son			
bit 4	Unimplemen	ted: Read as '	0'				
bit 3	MIDE: Identi	fier Receive Mo	ode bit				
 1 = Match only message types (standard or extended address) that correspond to EXIDE bit in filter 0 = Match either standard or extended address message if filters match (i.e., if (Filter SID) = (Message SID) or if (Filter SID/EID) = (Message SID/EID)) 							
bit 2	Unimplemen	ted: Read as '	0'				
bit 1-0	EID<17:16>:	Extended Ider	ntifier bits				
	 1 = Include bit EIDx in filter comparison 0 = Bit EIDx is don't care in filter comparison 						

REGISTER 19-21: CIRXMnEID: ECAN™ TECHNOLOGY ACCEPTANCE FILTER MASK n EXTENDED IDENTIFIER

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID15	EID14	EID13	EID12	EID11	EID10	EID9	EID8
bit 15							bit 8

| R/W-x |
|-------|-------|-------|-------|-------|-------|-------|-------|
| EID7 | EID6 | EID5 | EID4 | EID3 | EID2 | EID1 | EID0 |
| bit 7 | | | | | | | bit 0 |

Legend:				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 15-0 EID<15:0>: Extended Identifier bits

1 = Include bit EIDx in filter comparison

0 = Bit EIDx is don't care in filter comparison

23.7 MPLAB ICE 2000 High-Performance In-Circuit Emulator

The MPLAB ICE 2000 In-Circuit Emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PIC microcontrollers. Software control of the MPLAB ICE 2000 In-Circuit Emulator is advanced by the MPLAB Integrated Development Environment, which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICE 2000 is a full-featured emulator system with enhanced trace, trigger and data monitoring features. Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The architecture of the MPLAB ICE 2000 In-Circuit Emulator allows expansion to support new PIC microcontrollers.

The MPLAB ICE 2000 In-Circuit Emulator system has been designed as a real-time emulation system with advanced features that are typically found on more expensive development tools. The PC platform and Microsoft[®] Windows[®] 32-bit operating system were chosen to best make these features available in a simple, unified application.

23.8 MPLAB REAL ICE In-Circuit Emulator System

MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs PIC[®] Flash MCUs and dsPIC[®] Flash DSCs with the easy-to-use, powerful graphical user interface of the MPLAB Integrated Development Environment (IDE), included with each kit.

The MPLAB REAL ICE probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with the popular MPLAB ICD 2 system (RJ11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

MPLAB REAL ICE is field upgradeable through future firmware downloads in MPLAB IDE. In upcoming releases of MPLAB IDE, new devices will be supported, and new features will be added, such as software breakpoints and assembly code trace. MPLAB REAL ICE offers significant advantages over competitive emulators including low-cost, full-speed emulation, real-time variable watches, trace analysis, complex breakpoints, a ruggedized probe interface and long (up to three meters) interconnection cables.

23.9 MPLAB ICD 2 In-Circuit Debugger

Microchip's In-Circuit Debugger, MPLAB ICD 2, is a powerful, low-cost, run-time development tool, connecting to the host PC via an RS-232 or high-speed USB interface. This tool is based on the Flash PIC MCUs and can be used to develop for these and other PIC MCUs and dsPIC DSCs. The MPLAB ICD 2 utilizes the in-circuit debugging capability built into the Flash devices. This feature, along with Microchip's In-Circuit Serial Programming[™] (ICSP[™]) protocol, offers costeffective, in-circuit Flash debugging from the graphical user interface of the MPLAB Integrated Development Environment. This enables a designer to develop and debug source code by setting breakpoints, single stepping and watching variables, and CPU status and peripheral registers. Running at full speed enables testing hardware and applications in real time. MPLAB ICD 2 also serves as a development programmer for selected PIC devices.

23.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices and incorporates an SD/MMC card for file storage and secure data applications.

TABLE 24-5: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial				
Parameter No.	Typical ⁽¹⁾	Мах	Units	Conditions			
Operating Cur	rent (IDD) ⁽²⁾						
DC20d	27	30	mA	-40°C		10 MIPS	
DC20a	27	30	mA	+25°C	3.3V		
DC20b	27	30	mA	+85°C			
DC21d	36	40	mA	-40°C		16 MIPS	
DC21a	37	40	mA	+25°C	3.3V		
DC21b	38	45	mA	+85°C			
DC22d	43	50	mA	-40°C		20 MIPS	
DC22a	46	50	mA	+25°C	3.3V		
DC22b	46	55	mA	+85°C			
DC23d	65	70	mA	-40°C		30 MIPS	
DC23a	65	70	mA	+25°C	3.3V		
DC23b	65	70	mA	+85°C			
DC24d	84	90	mA	-40°C			
DC24a	84	90	mA	+25°C	3.3V	40 MIPS	
DC24b	84	90	mA	+85°C			

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all IDD measurements are as follows: OSC1 driven with external square wave from rail to rail. All I/O pins are configured as inputs and pulled to Vss. MCLR = VDD, WDT and FSCM are disabled. CPU, SRAM, program memory and data memory are operational. No peripheral modules are operating; however, every peripheral is being clocked (PMD bits are all zeroed).

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial				
Parameter No.	Typical ⁽¹⁾	Мах	Units	Conditions			
Idle Current (II	Idle Current (IIDLE): Core OFF Clock ON Base Current ⁽²⁾						
DC40d	3	25	mA	-40°C		10 MIPS	
DC40a	3	25	mA	+25°C	3 3\/		
DC40b	3	25	mA	+85°C	0.01		
DC41d	4	25	mA	-40°C		16 MIPS	
DC41a	5	25	mA	+25°C	3.3V		
DC41b	6	25	mA	+85°C			
DC42d	8	25	mA	-40°C		20 MIPS	
DC42a	9	25	mA	+25°C	3.3V		
DC42b	10	25	mA	+85°C			
DC43a	15	25	mA	+25°C		30 MIPS	
DC43d	15	25	mA	-40°C	3.3V		
DC43b	15	25	mA	+85°C			
DC44d	16	25	mA	-40°C		40 MIPS	
DC44a	16	25	mA	+25°C	3.3V		
DC44b	16	25	mA	+85°C			

TABLE 24-6: DC CHARACTERISTICS: IDLE CURRENT (IIDLE)

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated.

2: Base IIDLE current is measured with core off, clock on and all modules turned off. Peripheral Module Disable SFR registers are zeroed. All I/O pins are configured as inputs and pulled to Vss.

TABLE 24-21: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER TIMING REQUIREMENTS

		Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial					
Param No.	Symbol	Characteristic ⁽¹⁾	Min	Typ ⁽²⁾	Мах	Units	Conditions
SY10	ТмсL	MCLR Pulse-Width (low)	2			μs	-40°C to +85°C
SY11	TPWRT	Power-up Timer Period		2 4 16 32 64 128		ms	-40°C to +85°C User programmable
SY12	TPOR	Power-on Reset Delay	3	10	30	μs	-40°C to +85°C
SY13	Tioz	I/O High-Impedance from MCLR Low or Watchdog Timer Reset	0.68	0.72	1.2	μs	_
SY20	Twdt1	Watchdog Timer Time-out Period	_	_		_	See Section 21.4 "Watchdog Timer (WDT)" and LPRC specification F21 (Table 24-19)
SY30	Tost	Oscillator Start-up Timer Period	—	1024 Tosc	_	—	Tosc = OSC1 period
SY35	TFSCM	Fail-Safe Clock Monitor Delay	_	500	900	μs	-40°C to +85°C

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated.

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial				
Param No.	Symbol	Characteristic ⁽¹⁾	Min	Typ ⁽²⁾	Мах	Units	Conditions
SP70	TscL	SCKx Input Low Time	30			ns	_
SP71	TscH	SCKx Input High Time	30	_	_	ns	—
SP72	TscF	SCKx Input Fall Time ⁽³⁾	_	10	25	ns	—
SP73	TscR	SCKx Input Rise Time ⁽³⁾	—	10	25	ns	—
SP30	TdoF	SDOx Data Output Fall Time ⁽³⁾	_	_	_	ns	See parameter D032
SP31	TdoR	SDOx Data Output Rise Time ⁽³⁾	—	_	_	ns	See parameter D031
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—		30	ns	—
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	20	_	_	ns	—
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	20			ns	_
SP50	TssL2scH, TssL2scL	SSx ↓ to SCKx ↓ or SCKx ↑ Input	120	_	_	ns	_
SP51	TssH2doZ	SSx	10	_	50	ns	_
SP52	TscH2ssH TscL2ssH	SSx ↑ after SCKx Edge	1.5 TCY + 40	_	_	ns	—
SP60	TssL2doV	SDOx Data Output Valid after SSx Edge	—	_	50	ns	_

TABLE 24-31: SPIX MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated.

3: The minimum clock period for SCKx is 100 ns. The clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.







100-Lead Plastic Thin Quad Flatpack (PF) – 14x14x1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Chamfers at corners are optional; size may vary.

3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.

4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-110B

Section Name	Update Description
Section 19.0 "Enhanced CAN (ECAN™) Module"	Changed bit 11 in the ECAN Control Register 1 (CiCTRL1) to Reserved (see Register 19-1).
	Added the ECAN Filter 15-8 Mask Selection (CiFMSKSEL2) register (see Register 19-19).
Section 20.0 "10-Bit/12-Bit Analog-to- Digital Converter (ADC)"	Replaced the ADC Module Block Diagram (see Figure 20-1) and removed Figure 21-2.
Section 21.0 "Special Features"	Added Note 2 to the Device Configuration Register Map (see Table 21-1)
Section 24.0 "Electrical Characteristics"	Updated Typical values for Thermal Packaging Characteristics (see Table 24-3).
	Updated Min and Max values for parameter DC12 (RAM Data Retention Voltage) and added Note 4 (see Table 24-4).
	Updated Power-Down Current Max values for parameters DC60b and DC60c (see Table 24-7).
	Updated Characteristics for I/O Pin Input Specifications (see Table 24-9).
	Updated Program Memory values for parameters 136, 137 and 138 (renamed to 136a, 137a and 138a), added parameters 136b, 137b and 138b, and added Note 2 (see Table 24-12).
	Added parameter OS42 (GM) to the External Clock Timing Requirements (see Table 24-16).
	Updated Watchdog Timer Time-out Period parameter SY20 (see Table 24-21).

TABLE A-2: MAJOR SECTION UPDATES (CONTINUED)