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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | STM8 |
| Core Size | 8-Bit |
| Speed | 16MHz |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, POR, PWM, WDT |
| Number of I/O | 41 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 2K x 8 |
| RAM Size | 4K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.65V ~ 3.6V |
| Data Converters | A/D 25x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-LQFP |
| Supplier Device Package | 48-LQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm8al31e88tay |

STM8AL ultra-low-power microcontrollers operates either from 1.8 to 3.6 V (down to 1.65 V at power-down) or from 1.65 to 3.6 V. They are available in the -40 to +85 °C and -40 to +125 °C temperature ranges.

These features make the STM8AL ultra-low-power microcontroller families suitable for a wide range of applications.

The devices are offered in one 48-pin package. Different sets of peripherals are included depending on the device. Refer to *Section 3* for an overview of the complete range of peripherals proposed in this family.

All STM8AL ultra-low-power products are based on the same architecture with the same memory mapping and a coherent pinout.

*Figure 1* shows the block diagram of the high-density STM8AL3xE8x families.

## 3.3 Reset and supply management

### 3.3.1 Power supply scheme

The device requires a 1.65 V to 3.6 V operating supply voltage ($V_{DD}$). The external power supply pins must be connected as follows:

- $V_{SS1}$, $V_{DD1}$, $V_{SS2}$, $V_{DD2}$, $V_{SS3}$, $V_{DD3}$, $V_{SS4}$, $V_{DD4}$= 1.65 to 3.6 V: external power supply for I/Os and for the internal regulator. Provided externally through $V_{DD}$ pins, the corresponding ground pin is $V_{SS}$. $V_{SS1}$/$V_{SS2}$/$V_{SS3}$/$V_{SS4}$ and $V_{DD1}$/$V_{DD2}$/$V_{DD3}$/$V_{DD4}$ must not be left unconnected.
- $V_{SSA}$, $V_{DDA}$ = 1.65 to 3.6 V: external power supplies for analog peripherals (minimum voltage to be applied to $V_{DDA}$ is 1.8 V when the ADC1 is used). $V_{DDA}$ and $V_{SSA}$ must be connected to $V_{DD}$ and $V_{SS}$, respectively.
- $V_{REF+}$, $V_{REF-}$ (for ADC1): external reference voltage for ADC1. Must be provided externally through $V_{REF+}$ and $V_{REF-}$ pin.
- $V_{REF+}$ (for DAC1/2): external voltage reference for DAC1 and DAC2 must be provided externally through $V_{REF+}$.

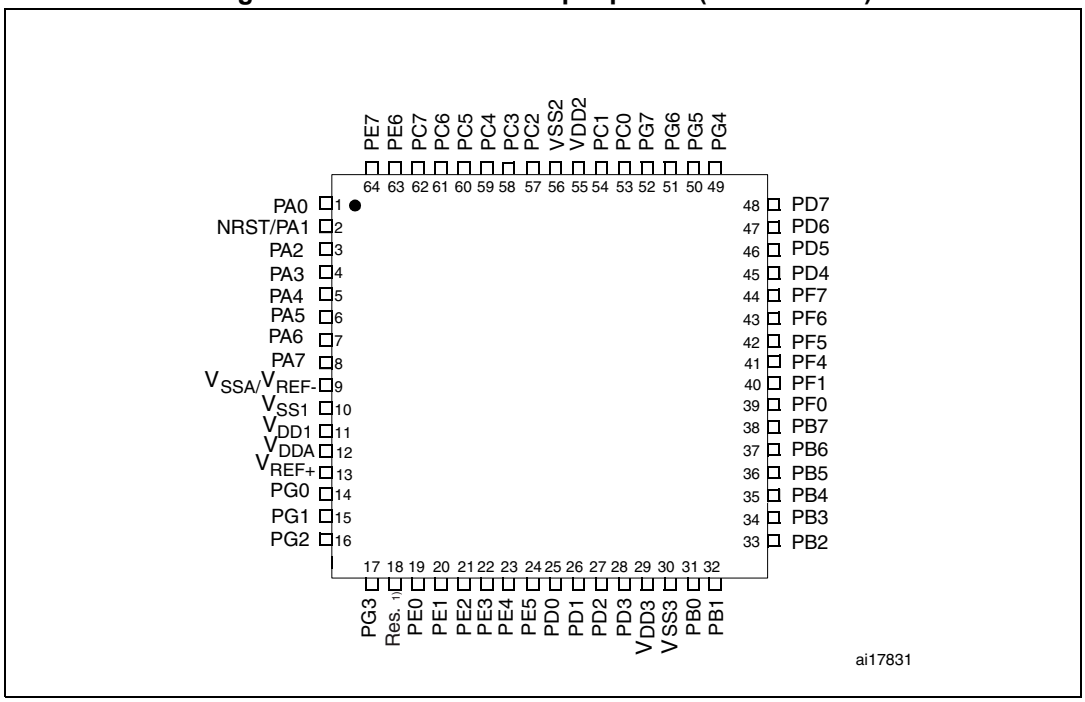
### 3.3.2 Power supply supervisor

The device has an integrated ZEROPOWER power-on reset (POR)/power-down reset (PDR), coupled with a brownout reset (BOR) circuitry. At power-on, BOR is always active, and ensures proper operation starting from 1.8 V. As soon as the 1.8 V BOR threshold is reached, the option byte loading process starts, either to confirm or modify the default thresholds, or to disable BOR permanently. In this latter case, the $V_{DD}$ min value at power down is 1.65 V.

Five BOR thresholds are available through option byte, starting from 1.8 V to 3 V. To reduce the power consumption in Halt mode, it is possible to automatically switch off the internal reference voltage (and consequently the BOR) in Halt mode. The device remains in reset state when $V_{DD}$ is below a specified threshold, $V_{POR/PDR}$ or $V_{BOR}$, without the need for any external reset circuit.

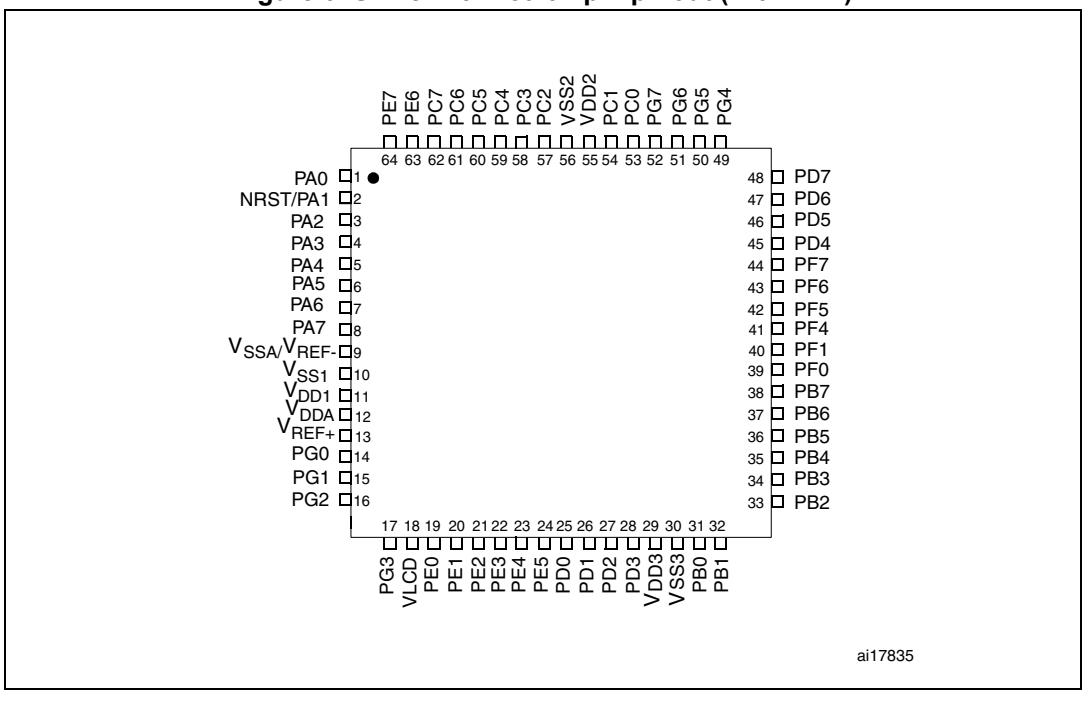
The device features an embedded programmable voltage detector (PVD) that monitors the $V_{DD}$/$V_{DDA}$ power supply and compares it to the $V_{PVD}$ threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt is generated when $V_{DD}$/$V_{DDA}$ drops below the $V_{PVD}$ threshold and/or when $V_{DD}$/$V_{DDA}$ is higher than the $V_{PVD}$ threshold. The interrupt service routine generates then a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

**Figure 5. STM8AL31E89 64-pin pinout (without LCD)**




1. Pin 18 is reserved and must be tied to $V_{DD}$.
2. The above figure shows the package top view.

**Figure 6. STM8AL3LE89 64-pin pinout (with LCD)**




1. The above figure shows the package top view.

**Table 5. High-density STM8AL3xE8x pin description (continued)**

| Pin number | | | Pin name | Type | I/O level | Input | | | Output | | | Main function (after reset) | Default alternate function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP80 | LQFP64 | LQFP48 | | | | floating | wpu | Ext. interrupt | High sink/source | OD | PP | | |
| 5 | 1 | 1 | PA0[8]/*[USART1_CK]*[2]/ SWIM/BEEP/IR_TIM [9] | I/O | - | X | **X** | X | HS | X | X | **Port A0** | *[USART1 synchronous clock]*[2] / SWIM input and output / Beep output / Infrared Timer output |
| 68 | 56 | 40 | $V_{SS2}$ | S | - | **-** | - | - | - | - | - | IOs ground voltage | |
| 67 | 55 | 39 | $V_{DD2}$ | S | - | **-** | - | - | - | - | - | IOs supply voltage | |
| 48 | - | - | $V_{SS4}$ | S | - | **-** | - | - | - | - | - | IOs ground voltage | |
| 47 | - | - | $V_{DD4}$ | S | - | **-** | - | - | - | - | - | IOs supply voltage | |

1. At power-up, the PA1/NRST pin is a reset input pin with pull-up. To be used as a general purpose pin (PA1), it can be configured only as output open-drain or push-pull, not as a general purpose input. Refer to Section *Configuring NRST/PA1 pin as general purpose output* in STM8L051/L052 Value Line, STM8L151/L152, STM8L162, STM8AL31, STM8AL3L MCU lines reference manual (RM0031).
2. [ ] Alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).
3. Available onSTM8AL3LE8xdevices only.
4. A pull-up is applied to PB0 and PB4 during the reset phase. These two pins are input floating after reset release.
5. In the 5 V tolerant I/Os, the protection diode to $V_{DD}$ is not implemented.
6. In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer, weak pull-up and protection diode to $V_{DD}$ are not implemented).
7. Available on STM8AL3LE8x devices only. On STM8AL31E8x devices it is reserved and must be tied to $V_{DD}$.
8. The PA0 pin is in input pull-up during the reset phase and after reset release.
9. High Sink LED driver capability available on PA0.

*Note: The slope control of all GPIO pins, except true open drain pins, are programmable. By default the slope control is limited to 2 MHz.*

### System configuration options

As shown in *Table 5: High-density STM8AL3xE8x pin description*, some alternate functions can be remapped on different I/O ports by programming one of the two remapping registers described in the "Routing interface (RI) and system configuration controller" section in STM8L051/L052 Value Line, STM8L151/L152, STM8L162, STM8AL31, STM8AL3L MCU lines reference manual (RM0031).

**Table 9. General hardware register map**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 502E to 0x00 5049 | Reserved area (44 byte) | | | |
| 0x00 5050 | Flash | FLASH_CR1 | Flash control register 1 | 0x00 |
| 0x00 5051 | | FLASH_CR2 | Flash control register 2 | 0x00 |
| 0x00 5052 | | FLASH _PUKR | Flash program memory unprotection key register | 0x00 |
| 0x00 5053 | | FLASH _DUKR | Data EEPROM unprotection key register | 0x00 |
| 0x00 5054 | | FLASH _IAPSR | Flash in-application programming status register | 0x00 |
| 0x00 5055 to 0x00 506F | Reserved area (27 byte) | | | |
| 0x00 5070 | DMA1 | DMA1_GCSR | DMA1 global configuration & status register | 0xFC |
| 0x00 5071 | | DMA1_GIR1 | DMA1 global interrupt register 1 | 0x00 |
| 0x00 5072 to 0x00 5074 | Reserved area (3 byte) | | | |
| 0x00 5075 | DMA1 | DMA1_C0CR | DMA1 channel 0 configuration register | 0x00 |
| 0x00 5076 | | DMA1_C0SPR | DMA1 channel 0 status & priority register | 0x00 |
| 0x00 5077 | | DMA1_C0NDTR | DMA1 number of data to transfer register (channel 0) | 0x00 |
| 0x00 5078 | | DMA1_C0PARH | DMA1 peripheral address high register (channel 0) | 0x52 |
| 0x00 5079 | | DMA1_C0PARL | DMA1 peripheral address low register (channel 0) | 0x00 |
| 0x00 507A | | Reserved area (1 byte) | | |
| 0x00 507B | | DMA1_C0M0ARH | DMA1 memory 0 address high register (channel 0) | 0x00 |
| 0x00 507C | | DMA1_C0M0ARL | DMA1 memory 0 address low register (channel 0) | 0x00 |
| 0x00 507D to 0x00 507E | Reserved area (2 byte) | | | |
| 0x00 507F | DMA1 | DMA1_C1CR | DMA1 channel 1 configuration register | 0x00 |
| 0x00 5080 | | DMA1_C1SPR | DMA1 channel 1 status & priority register | 0x00 |
| 0x00 5081 | | DMA1_C1NDTR | DMA1 number of data to transfer register (channel 1) | 0x00 |
| 0x00 5082 | | DMA1_C1PARH | DMA1 peripheral address high register (channel 1) | 0x52 |
| 0x00 5083 | | DMA1_C1PARL | DMA1 peripheral address low register (channel 1) | 0x00 |

**Table 9. General hardware register map (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 5084 | Reserved area (1 byte) | | | |
| 0x00 5085 | DMA1 | DMA1_C1M0ARH | DMA1 memory 0 address high register (channel 1) | 0x00 |
| 0x00 5086 | | DMA1_C1M0ARL | DMA1 memory 0 address low register (channel 1) | 0x00 |
| 0x00 5087<br>0x00 5088 | Reserved area (2 byte) | | | |
| 0x00 5089 | DMA1 | DMA1_C2CR | DMA1 channel 2 configuration register | 0x00 |
| 0x00 508A | | DMA1_C2SPR | DMA1 channel 2 status & priority register | 0x00 |
| 0x00 508B | | DMA1_C2NDTR | DMA1 number of data to transfer register (channel 2) | 0x00 |
| 0x00 508C | | DMA1_C2PARH | DMA1 peripheral address high register (channel 2) | 0x52 |
| 0x00 508D | | DMA1_C2PARL | DMA1 peripheral address low register (channel 2) | 0x00 |
| 0x00 508E | | Reserved area (1 byte) | | |
| 0x00 508F | | DMA1_C2M0ARH | DMA1 memory 0 address high register (channel 2) | 0x00 |
| 0x00 5090 | | DMA1_C2M0ARL | DMA1 memory 0 address low register (channel 2) | 0x00 |
| 0x00 5091<br>0x00 5092 | Reserved area (2 byte) | | | |
| 0x00 5093 | DMA1 | DMA1_C3CR | DMA1 channel 3 configuration register | 0x00 |
| 0x00 5094 | | DMA1_C3SPR | DMA1 channel 3 status & priority register | 0x00 |
| 0x00 5095 | | DMA1_C3NDTR | DMA1 number of data to transfer register (channel 3) | 0x00 |
| 0x00 5096 | | DMA1_C3PARH_ C3M1ARH | DMA1 peripheral address high register (channel 3) | 0x40 |
| 0x00 5097 | | DMA1_C3PARL_ C3M1ARL | DMA1 peripheral address low register (channel 3) | 0x00 |
| 0x00 5098 | | DMA_C3M0EAR | DMA channel 3 memory 0 extended address register | 0x00 |
| 0x00 5099 | | DMA1_C3M0ARH | DMA1 memory 0 address high register (channel 3) | 0x00 |
| 0x00 509A | | DMA1_C3M0ARL | DMA1 memory 0 address low register (channel 3) | 0x00 |
| 0x00 509B to 0x00 509C | Reserved area (3 byte) | | | |

**Table 9. General hardware register map (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 5148 | RTC | RTC_CR1 | Control register 1 | 0x00(1) |
| 0x00 5149 | | RTC_CR2 | Control register 2 | 0x00(1) |
| 0x00 514A | | RTC_CR3 | Control register 3 | 0x00(1) |
| 0x00 514B | | Reserved area (1 byte) | | |
| 0x00 514C | | RTC_ISR1 | Initialization and status register 1 | 0x01 |
| 0x00 514D | | RTC_ISR2 | Initialization and Status register 2 | 0x00 |
| 0x00 514E<br>0x00 514F | Reserved area (2 byte) | | | |
| 0x00 5150 | RTC | RTC_SPRERH | Synchronous prescaler register high | 0x00(1) |
| 0x00 5151 | | RTC_SPRERL | Synchronous prescaler register low | 0xFF(1) |
| 0x00 5152 | | RTC_APRER | Asynchronous prescaler register | 0x7F(1) |
| 0x00 5153 | Reserved area (1 byte) | | | |
| 0x00 5154 | RTC | RTC_WUTRH | Wakeup timer register high | 0xFF(1) |
| 0x00 5155 | | RTC_WUTRL | Wakeup timer register low | 0xFF(1) |
| 0x00 5156 | Reserved area (1 byte) | | | |
| 0x00 5157 | RTC | RTC_SSRL | Subsecond register low | 0x00 |
| 0x00 5158 | | RTC_SSRH | Subsecond register high | 0x00 |
| 0x00 5159 | | RTC_WPR | Write protection register | 0x00 |
| 0x00 5158 | | RTC_SSRH | Subsecond register high | 0x00 |
| 0x00 5159 | | RTC_WPR | Write protection register | 0x00 |
| 0x00 515A | | RTC_SHIFTRH | Shift register high | 0x00 |
| 0x00 515B | | RTC_SHIFTRL | Shift register low | 0x00 |
| 0x00 515C | | RTC_ALRMAR1 | Alarm A register 1 | 0x00(1) |
| 0x00 515D | | RTC_ALRMAR2 | Alarm A register 2 | 0x00(1) |
| 0x00 515E | | RTC_ALRMAR3 | Alarm A register 3 | 0x00(1) |
| 0x00 515F | | RTC_ALRMAR4 | Alarm A register 4 | 0x00(1) |
| 0x00 5160 to<br>0x00 5163 | Reserved area (4 byte) | | | |
| 0x00 5164 | RTC | RTC_ALRMASSRH | Alarm A subsecond register high | 0x00(1) |
| 0x00 5165 | | RTC_ALRMASSRL | Alarm A subsecond register low | 0x00(1) |
| 0x00 5166 | | RTC_ALRMASSMSKR | Alarm A masking register | 0x00(1) |
| 0x00 5167 to<br>0x00 5169 | Reserved area (3 byte) | | | |

**Table 9. General hardware register map (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 52B0 | TIM1 | TIM1_CR1 | TIM1 control register 1 | 0x00 |
| 0x00 52B1 | | TIM1_CR2 | TIM1 control register 2 | 0x00 |
| 0x00 52B2 | | TIM1_SMCR | TIM1 Slave mode control register | 0x00 |
| 0x00 52B3 | | TIM1_ETR | TIM1 external trigger register | 0x00 |
| 0x00 52B4 | | TIM1_DER | TIM1 DMA1 request enable register | 0x00 |
| 0x00 52B5 | | TIM1_IER | TIM1 Interrupt enable register | 0x00 |
| 0x00 52B6 | | TIM1_SR1 | TIM1 status register 1 | 0x00 |
| 0x00 52B7 | | TIM1_SR2 | TIM1 status register 2 | 0x00 |
| 0x00 52B8 | | TIM1_EGR | TIM1 event generation register | 0x00 |
| 0x00 52B9 | | TIM1_CCMR1 | TIM1 Capture/Compare mode register 1 | 0x00 |
| 0x00 52BA | | TIM1_CCMR2 | TIM1 Capture/Compare mode register 2 | 0x00 |
| 0x00 52BB | | TIM1_CCMR3 | TIM1 Capture/Compare mode register 3 | 0x00 |
| 0x00 52BC | | TIM1_CCMR4 | TIM1 Capture/Compare mode register 4 | 0x00 |
| 0x00 52BD | | TIM1_CCER1 | TIM1 Capture/Compare enable register 1 | 0x00 |
| 0x00 52BE | | TIM1_CCER2 | TIM1 Capture/Compare enable register 2 | 0x00 |
| 0x00 52BF | | TIM1_CNTRH | TIM1 counter high | 0x00 |
| 0x00 52C0 | | TIM1_CNTRL | TIM1 counter low | 0x00 |
| 0x00 52C1 | | TIM1_PSCRH | TIM1 prescaler register high | 0x00 |
| 0x00 52C2 | | TIM1_PSCRL | TIM1 prescaler register low | 0x00 |
| 0x00 52C3 | | TIM1_ARRH | TIM1 Auto-reload register high | 0xFF |
| 0x00 52C4 | | TIM1_ARRL | TIM1 Auto-reload register low | 0xFF |
| 0x00 52C5 | | TIM1_RCR | TIM1 Repetition counter register | 0x00 |
| 0x00 52C6 | | TIM1_CCR1H | TIM1 Capture/Compare register 1 high | 0x00 |
| 0x00 52C7 | | TIM1_CCR1L | TIM1 Capture/Compare register 1 low | 0x00 |
| 0x00 52C8 | | TIM1_CCR2H | TIM1 Capture/Compare register 2 high | 0x00 |
| 0x00 52C9 | | TIM1_CCR2L | TIM1 Capture/Compare register 2 low | 0x00 |
| 0x00 52CA | | TIM1_CCR3H | TIM1 Capture/Compare register 3 high | 0x00 |
| 0x00 52CB | | TIM1_CCR3L | TIM1 Capture/Compare register 3 low | 0x00 |
| 0x00 52CC | | TIM1_CCR4H | TIM1 Capture/Compare register 4 high | 0x00 |
| 0x00 52CD | | TIM1_CCR4L | TIM1 Capture/Compare register 4 low | 0x00 |
| 0x00 52CE | | TIM1_BKR | TIM1 break register | 0x00 |
| 0x00 52CF | | TIM1_DTR | TIM1 dead-time register | 0x00 |
| 0x00 52D0 | | TIM1_OISR | TIM1 output idle state register | 0x00 |
| 0x00 52D1 | | TIM1_DCR1 | DMA1 control register 1 | 0x00 |

**Table 9. General hardware register map (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 5400 | LCD | LCD_CR1 | LCD control register 1 | 0x00 |
| 0x00 5401 | | LCD_CR2 | LCD control register 2 | 0x00 |
| 0x00 5402 | | LCD_CR3 | LCD control register 3 | 0x00 |
| 0x00 5403 | | LCD_FRQ | LCD frequency selection register | 0x00 |
| 0x00 5404 | | LCD_PM0 | LCD Port mask register 0 | 0x00 |
| 0x00 5405 | | LCD_PM1 | LCD Port mask register 1 | 0x00 |
| 0x00 5406 | | LCD_PM2 | LCD Port mask register 2 | 0x00 |
| 0x00 5407 | | LCD_PM3 | LCD Port mask register 3 | 0x00 |
| 0x00 5408 | | LCD_PM4 | LCD Port mask register 4 | 0x00 |
| 0x00 5409 | | LCD_PM5 | LCD Port mask register 5 | 0x00 |
| 0x00 540A to 0x00 540B | Reserved area (2 byte) | | | |
| 0x00 540C | LCD | LCD_RAM0 | LCD display memory 0 | 0x00 |
| 0x00 540D | | LCD_RAM1 | LCD display memory 1 | 0x00 |
| 0x00 540E | | LCD_RAM2 | LCD display memory 2 | 0x00 |
| 0x00 540F | | LCD_RAM3 | LCD display memory 3 | 0x00 |
| 0x00 5410 | | LCD_RAM4 | LCD display memory 4 | 0x00 |
| 0x00 5411 | | LCD_RAM5 | LCD display memory 5 | 0x00 |
| 0x00 5412 | | LCD_RAM6 | LCD display memory 6 | 0x00 |
| 0x00 5413 | | LCD_RAM7 | LCD display memory 7 | 0x00 |
| 0x00 5414 | | LCD_RAM8 | LCD display memory 8 | 0x00 |
| 0x00 5415 | | LCD_RAM9 | LCD display memory 9 | 0x00 |
| 0x00 5416 | | LCD_RAM10 | LCD display memory 10 | 0x00 |
| 0x00 5417 | | LCD_RAM11 | LCD display memory 11 | 0x00 |
| 0x00 5418 | | LCD_RAM12 | LCD display memory 12 | 0x00 |
| 0x00 5419 | | LCD_RAM13 | LCD display memory 13 | 0x00 |
| 0x00 541A | | LCD_RAM14 | LCD display memory 14 | 0x00 |
| 0x00 541B | | LCD_RAM15 | LCD display memory 15 | 0x00 |
| 0x00 541C | | LCD_RAM16 | LCD display memory 16 | 0x00 |
| 0x00 541D | | LCD_RAM17 | LCD display memory 17 | 0x00 |
| 0x00 541E | | LCD_RAM18 | LCD display memory 18 | 0x00 |
| 0x00 541F | | LCD_RAM19 | LCD display memory 19 | 0x00 |
| 0x00 5420 | | LCD_RAM20 | LCD display memory 20 | 0x00 |
| 0x00 5421 | | LCD_RAM21 | LCD display memory 21 | 0x00 |

In the following table, data are based on characterization results, unless otherwise specified.

**Table 22. Total current consumption in Wait mode**

| Symbol | Parameter | Conditions[1] | | | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $I_{DD(Wait)}$ | Supply current in Wait mode | CPU not clocked, all peripherals OFF, code executed from RAM with Flash in $I_{DDQ}$ mode,[2] $V_{DD}$ from 1.65 V to 3.6 V | HSI | $f_{CPU}$ = 125 kHz | 0.35 | 0.45[4] | mA |
| | | | | $f_{CPU}$ = 1 MHz | 0.35 | 0.50[4] | |
| | | | | $f_{CPU}$ = 4 MHz | 0.40 | 0.60[4] | |
| | | | | $f_{CPU}$ = 8 MHz | 0.50 | 0.60[4] | |
| | | | | $f_{CPU}$ = 16 MHz | 0.70 | 0.85 | |
| | | | HSE external clock ($f_{CPU}$=$f_{HSE}$)[3] | $f_{CPU}$ = 125 kHz | 0.05 | 0.10[4] | |
| | | | | $f_{CPU}$ = 1 MHz | 0.10 | 0.20[4] | |
| | | | | $f_{CPU}$ = 4 MHz | 0.20 | 0.40[4] | |
| | | | | $f_{CPU}$ = 8 MHz | 0.40 | 0.65[4] | |
| | | | | $f_{CPU}$ = 16 MHz | 0.76 | 1.15[4] | |
| | | | LSI | $f_{CPU}$ = $f_{LSI}$ | 60 | 80[4] | µA |
| | | | LSE[5] external clock (32.768 kHz) | $f_{CPU}$ = $f_{LSE}$ | 50 | 70[4] | |
| $I_{DD(Wait)}$ | Supply current in Wait mode | CPU not clocked, all peripherals OFF, code executed from Flash, $V_{DD}$ from 1.65 V to 3.6 V | HSI | $f_{CPU}$ = 125 kHz | 0.38 | 0.55[4] | mA |
| | | | | $f_{CPU}$ = 1 MHz | 0.40 | 0.60[4] | |
| | | | | $f_{CPU}$ = 4 MHz | 0.50 | 0.65[4] | |
| | | | | $f_{CPU}$ = 8 MHz | 0.60 | 0.75[4] | |
| | | | | $f_{CPU}$ = 16 MHz | 0.80 | 0.90 | |
| | | | HSE[3] external clock ($f_{CPU}$= HSE) | $f_{CPU}$ = 125 kHz | 0.07 | 0.15[4] | |
| | | | | $f_{CPU}$ = 1 MHz | 0.10 | 0.20[4] | |
| | | | | $f_{CPU}$ = 4 MHz | 0.25 | 0.45[4] | |
| | | | | $f_{CPU}$ = 8 MHz | 0.50 | 0.65[4] | |
| | | | | $f_{CPU}$ = 16 MHz | 1.00 | 1.20[4] | |
| | | | LSI | $f_{CPU}$ = $f_{LSI}$ | 50 | 100[4] | µA |
| | | | LSE[5] external clock (32.768 kHz) | $f_{CPU}$ = $f_{LSE}$ | 50 | 80[4] | |

1. All peripherals OFF, $V_{DD}$ from 1.65 V to 3.6 V, HSI internal RC osc., $f_{CPU}$ = $f_{SYSCLK}$
2. Flash is configured in $I_{DDQ}$ mode in Wait mode by setting the EPM or WAITM bit in the Flash_CR1 register.
3. Oscillator bypassed (HSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the HSE consumption ($I_{DD\ HSE}$) must be added. Refer to *Table 32*.
4. Guaranteed by characterization results.
5. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ HSE}$) must be added. Refer to *Table 33*

### LSE external clock (LSEBYP=1 in CLK_ECKCR)

The LSE is available on STM8AL31E8x devices only.

Subject to general operating conditions for $V_{DD}$ and $T_A$.

**Table 31. LSE external clock characteristics**

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $f_{LSE\_ext}$ | External clock source frequency | - | 32.768 | - | kHz |
| $V_{LSEH}$ | OSC32_IN input pin high-level voltage | $0.7xV_{DD}$(1) | - | $V_{DD}$(1) | V |
| $V_{LSEL}$ | OSC32_IN input pin low-level voltage | $V_{SS}$(1) | | $0.3xV_{DD}$(1) | |
| $C_{in(LSE)}$ | OSC32_IN input capacitance | - | 0.6 | - | pF |
| $I_{LEAK\_LSE}$ | OSC32_IN input leakage current | - | - | ±500 | nA |

1. Guaranteed by characterization results.

### HSE crystal/ceramic resonator oscillator

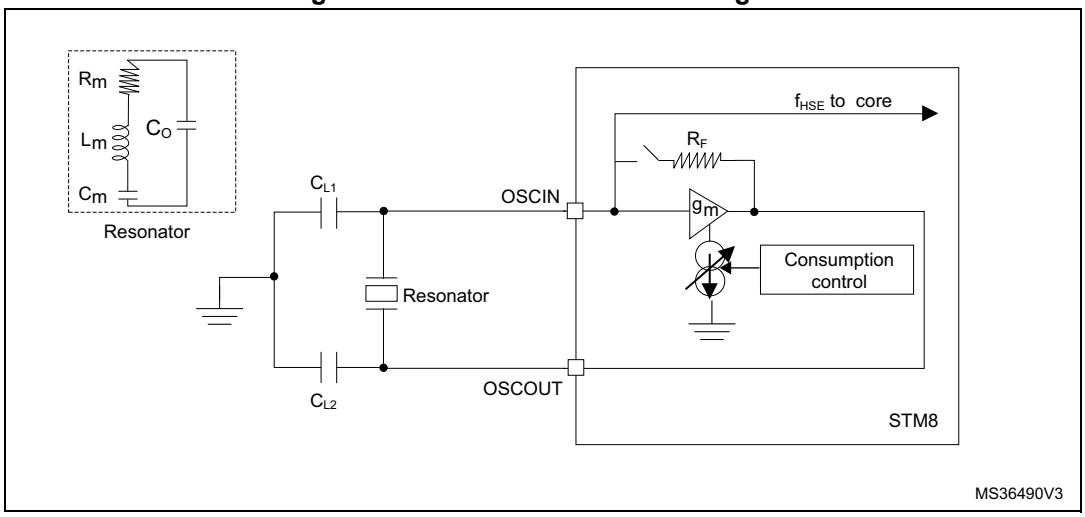
The HSE clock can be supplied with a 1 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

**Table 32. HSE oscillator characteristics**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $f_{HSE}$ | High speed external oscillator frequency | - | 1 | - | 16 | MHz |
| $R_F$ | Feedback resistor | - | - | 200 | - | kΩ |
| C(1)(2) | Recommended load capacitance | - | - | 20 | - | pF |
| $I_{DD(HSE)}$ | HSE oscillator power consumption | C = 20 pF, $f_{OSC}$ = 16 MHz | - | - | 2.5 (startup) 0.7 (stabilized)(3) | mA |
| | | C = 10 pF, $f_{OSC}$ =16 MHz | - | - | 2.5 (startup) 0.46 (stabilized)(3) | |
| $g_m$ | Oscillator transconductance | - | 3.5(3) | - | - | mA/V |
| $t_{SU(HSE)}$(4) | Startup time | $V_{DD}$ is stabilized | | 1 | - | ms |

1. $C=C_{L1}=C_{L2}$ is approximately equivalent to 2 x crystal $C_{LOAD}$.
2. The oscillator selection can be optimized in terms of supply current using a high quality resonator with small $R_m$ value. Refer to crystal manufacturer for more details
3. Guaranteed by design.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 16 MHz oscillation. This value is measured for a standard crystal resonator and it varies significantly with the crystal manufacturer.

**Figure 21. HSE oscillator circuit diagram**




### HSE oscillator critical $g_m$ formula

$$g_{mcrit} = (2 \times \Pi \times f_{HSE})^2 \times R_m(2Co + C)^2$$

$R_m$: Motional resistance (see crystal specification), $L_m$: Motional inductance (see crystal specification), $C_m$: Motional capacitance (see crystal specification), Co: Shunt capacitance (see crystal specification), $C_{L1}$=$C_{L2}$=C: Grounded external capacitance

$g_m >> g_{mcrit}$

## LSE crystal/ceramic resonator oscillator

The LSE is available on STM8AL31E8x devices only.

The LSE clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

**Figure 29. Typical $V_{OL}$ @ $V_{DD}$ = 3.0 V (high sink ports)**

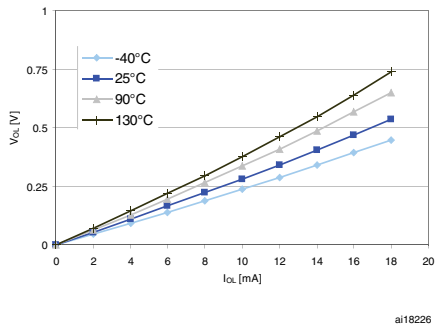



**Figure 30. Typical $V_{OL}$ @ $V_{DD}$ = 1.8 V (high sink ports)**

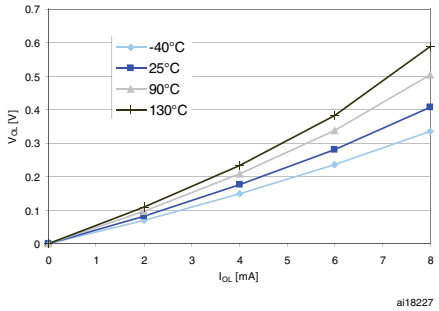



**Figure 31. Typical $V_{OL}$ @ $V_{DD}$ = 3.0 V (true open drain ports)**

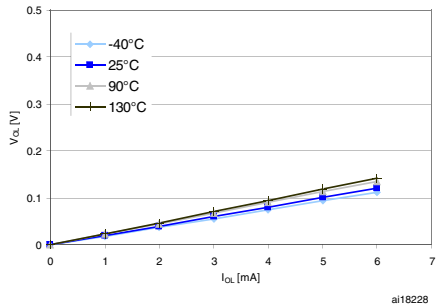



**Figure 32. Typical $V_{OL}$ @ $V_{DD}$ = 1.8 V (true open drain ports)**

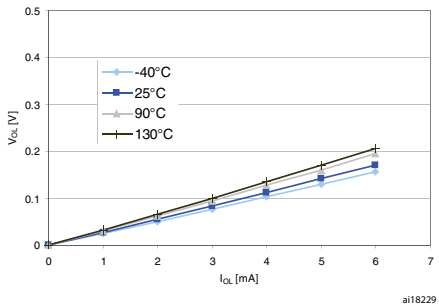



**Figure 33. Typical $V_{DD}$ - $V_{OH}$ @ $V_{DD}$ = 3.0 V (high sink ports)**

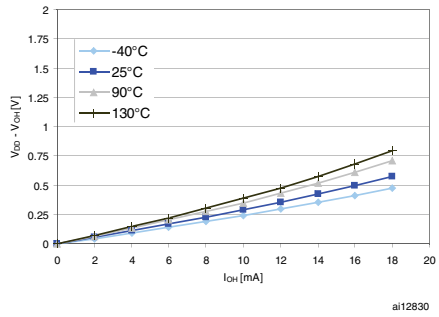



**Figure 34. Typical $V_{DD}$ - $V_{OH}$ @ $V_{DD}$ = 1.8 V (high sink ports)**

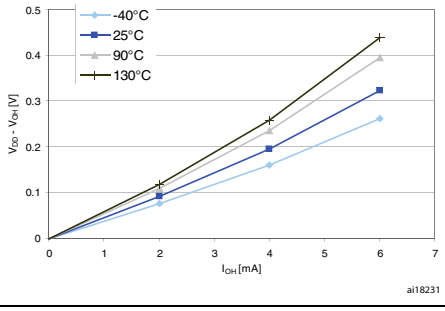
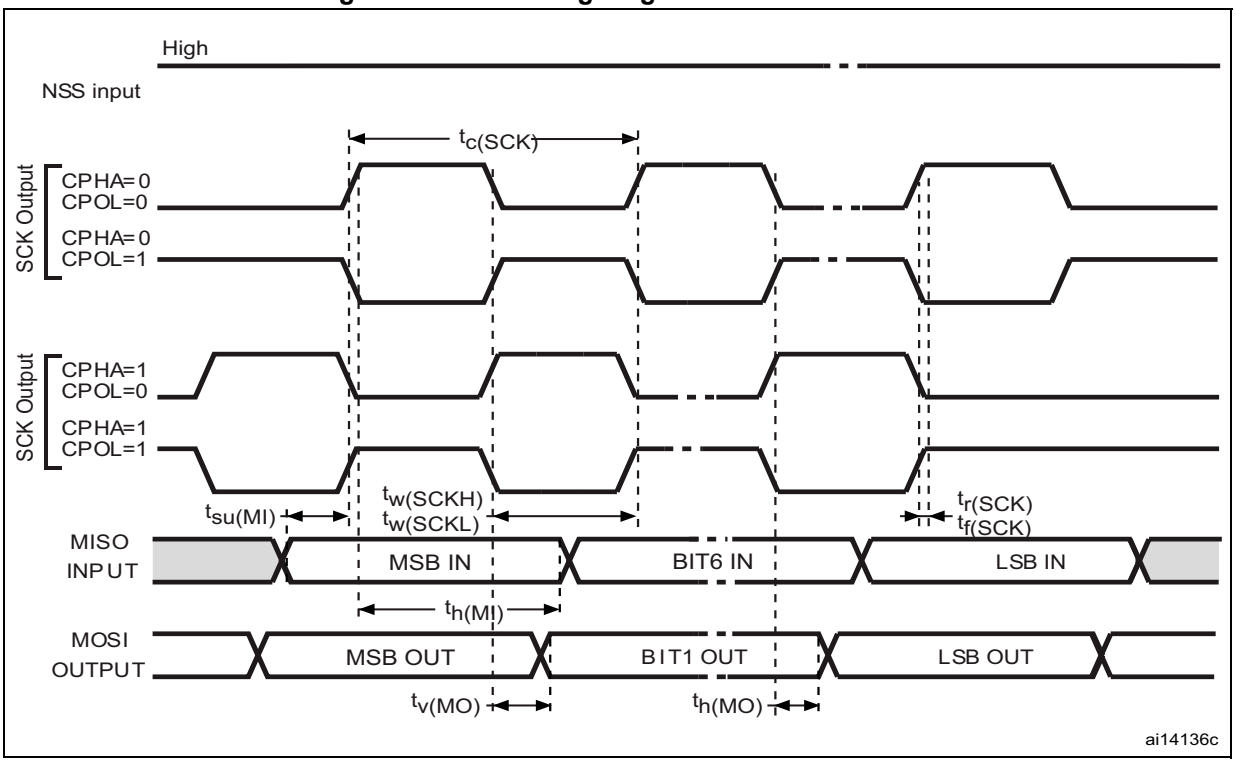


**Figure 40. SPI1 timing diagram - master mode(1)**




1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

### 9.3.10 Embedded reference voltage

In the following table, data are based on characterization results, not tested in production, unless otherwise specified.

**Table 49. Reference voltage characteristics**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{REFINT}$ | Internal reference voltage consumption | - | - | 1.4 | - | µA |
| $T_{S\_VREFINT}$(1)(2) | ADC sampling time when reading the internal reference voltage | - | - | 5 | 10 | µs |
| $I_{BUF}$(1) | Internal reference voltage buffer consumption (used for ADC) | - | - | 13.5 | 25 | µA |
| $V_{REFINT\ out}$ | Reference voltage output | - | 1.202 (3) | 1.224 | 1.242 (3) | V |
| $I_{LPBUF}$(1) | Internal reference voltage low-power buffer consumption (used for comparators or output) | - | - | 730 | 1200 | nA |
| $I_{REFOUT}$(1)(4) | Buffer output current | - | - | - | 1 | µA |
| $C_{REFOUT}$ | Reference voltage output load | - | - | - | 50 | pF |
| $t_{VREFINT}$(1) | Internal reference voltage startup time | - | - | 2 | 3 | ms |
| $t_{BUFEN}$(1)(2) | Internal reference voltage buffer startup time once enabled | - | - | - | 10 | µs |
| $ACC_{VREFINT}$(5) | Accuracy of $V_{REFINT}$ stored in the VREFINT_Factory_CONV byte | - | - | - | ± 5 | mV |
| $STAB_{VREFINT}$ | Stability of $V_{REFINT}$ over temperature | -40 °C ≤$T_A$ ≤ 125 °C | - | 20 | 50 | ppm/°C |
| | Stability of $V_{REFINT}$ over temperature | 0 °C ≤$T_A$ ≤ 50 °C | - | - | 20 | ppm/°C |
| $STAB_{VREFINT}$ | Stability of $V_{REFINT}$ after 1000 hours | - | - | - | TBD | ppm |

1. Guaranteed by design.
2. Defined when ADC output reaches its final value ±1/2LSB
3. Tested in production at $V_{DD}$ = 3 V ±10 mV.
4. To guarantee less than 1% $V_{REFOUT}$ deviation
5. Measured at $V_{DD}$ = 3 V ±10 mV. This value takes into account $V_{DD}$ accuracy and ADC conversion accuracy.

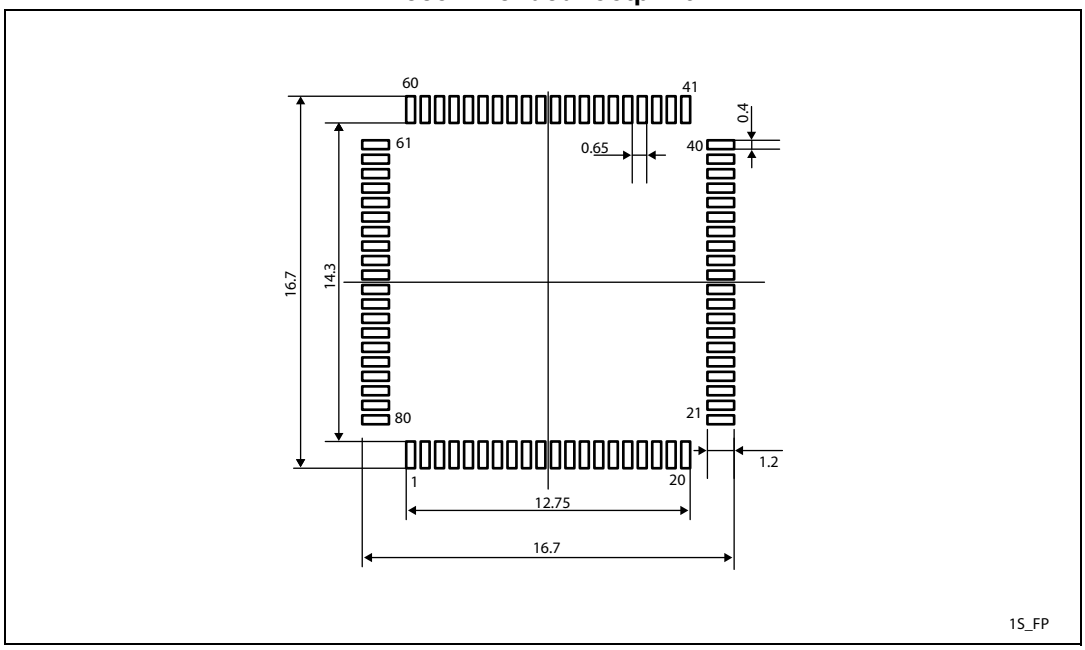
### 9.3.14 12-bit ADC1 characteristics

In the following table, data are guaranteed by design, not tested in production.

**Table 56. ADC1 characteristics**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Analog supply voltage | - | 1.8 | - | 3.6 | V |
| $V_{REF+}$ | Reference supply voltage | 2.4 V ≤$V_{DDA}$≤ 3.6 V | 2.4 | - | $V_{DDA}$ | V |
| | | 1.8 V≤$V_{DDA}$≤ 2.4 V | $V_{DDA}$ | | | V |
| $V_{REF-}$ | Lower reference voltage | - | $V_{SSA}$ | | | V |
| $I_{VDDA}$ | Current on the $V_{DDA}$ input pin | - | - | 1000 | 1450 | µA |
| $I_{VREF+}$ | Current on the $V_{REF+}$ input pin | - | - | 400 | 700 (peak)(1) | µA |
| | | - | - | | 450 (average)(1) | µA |
| $V_{AIN}$ | Conversion voltage range | - | 0(2) | - | $V_{REF+}$ | |
| $T_A$ | Temperature range | - | -40 | - | 125 | °C |
| $R_{AIN}$ | External resistance on $V_{AIN}$ | on PF0/1/2/3 fast channels | - | - | 50(3) | kΩ |
| | | on all other channels | - | - | | |
| $C_{ADC}$ | Internal sample and hold capacitor | on PF0/1/2/3 fast channels | - | 16 | - | pF |
| | | on all other channels | - | | - | |
| $f_{ADC}$ | ADC sampling clock frequency | 2.4 V≤$V_{DDA}$≤3.6 V without zooming | 0.320 | - | 16 | MHz |
| | | 1.8 V≤$V_{DDA}$≤2.4 V with zooming | 0.320 | - | 8 | MHz |
| $f_{CONV}$ | 12-bit conversion rate | $V_{AIN}$ on PF0/1/2/3 fast channels | - | - | 1(3)(4) | MHz |
| | | $V_{AIN}$ on all other channels | - | - | 760(3)(4) | kHz |
| $f_{TRIG}$ | External trigger frequency | - | - | - | $t_{conv}$ | $1/f_{ADC}$ |
| $t_{LAT}$ | External trigger latency | - | - | - | 3.5 | $1/f_{SYSCLK}$ |

**Figure 47. LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package recommended footprint**




1. Dimensions are expressed in millimeters.

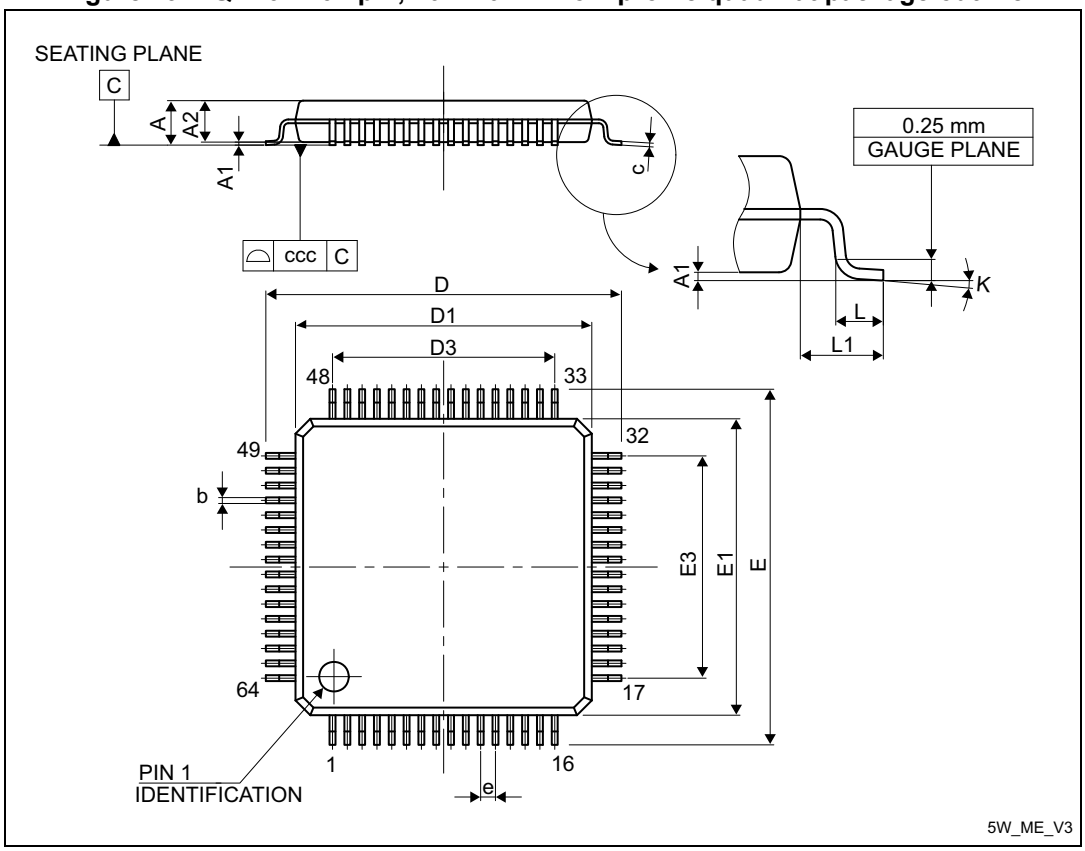
## Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

## 10.2 LQFP64 package information

**Figure 49. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline**




1. Drawing is not to scale.

**Table 66. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | - | 12.000 | - | - | 0.4724 | - |
| D1 | - | 10.000 | - | - | 0.3937 | - |
| D3 | - | 7.500 | - | - | 0.2953 | - |
| E | - | 12.000 | - | - | 0.4724 | - |
| E1 | - | 10.000 | - | - | 0.3937 | - |

# 12 Revision history

Table 69. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 22-Apr-2015 | 1 | Initial release. |
| 27-Jul-2015 | 2 | Updated the document confidentiality level to “Public”.<br>No other changes in the content. |
| 19-Aug-2015 | 3 | Changed datasheet status to “production data”.<br>Added LQFP64 and LQFP80 packages together with the corresponding part numbers. |
| 18-Oct-2016 | 4 | – Updated *Table 5: High-density STM8AL3xE8x pin description*: pin name changed from PC3/USART1_TX/LCD_SEG23(3)/ADC1_IN5/COMP_IN3M/COMP2_INM/COMP1_INP to PC3/USART1_TX/LCD_SEG23(3)/ADC1_IN5/COMP2_INM/COMP1_INP.<br>– Added footnote to *Table 68: STM8AL31E8x STM8AL3LE8x ordering information scheme*.<br>– Updated *Section : Device marking on page 122*, *Section : Device marking on page 126*, *Section : Device marking on page 130*<br>– Updated *Section 9.2: Absolute maximum ratings*<br>– Updated *Figure 12: Power supply thresholds*. |
| 5-Dec-2016 | 5 | – Updated *Table 5: High-density STM8AL3xE8x pin description*: two pin names changed from PI0/RTC_TAMP1/[SPI2_NSS]/[TIM3_CH3 to PI0/RTC_TAMP1/[SPI2_NSS]/[TIM3_CH1 and from PF2/ADC1_IN26/[SPI2_SCK]/[USART3_SCK] to PF2/ADC1_IN26/[SPI1_SCK]/[USART3_SCK] |