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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	68
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 28x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8al31e8atay

Contents

Table 4. Legend/abbreviation

Type	I= input, O = output, S = power supply	
Level	FT: Five-volt tolerant	
	Output	HS = high sink/source (20 mA)
Port and control configuration	Input	float = floating, wpu = weak pull-up
	Output	T = true open drain, OD = open drain, PP = push pull
Reset state	Bold X (pin state after reset release). Unless otherwise specified, the pin state is the same during the reset phase (i.e. “under reset”) and after internal reset release (i.e. at reset state).	

Table 5. High-density STM8AL3xE8x pin description

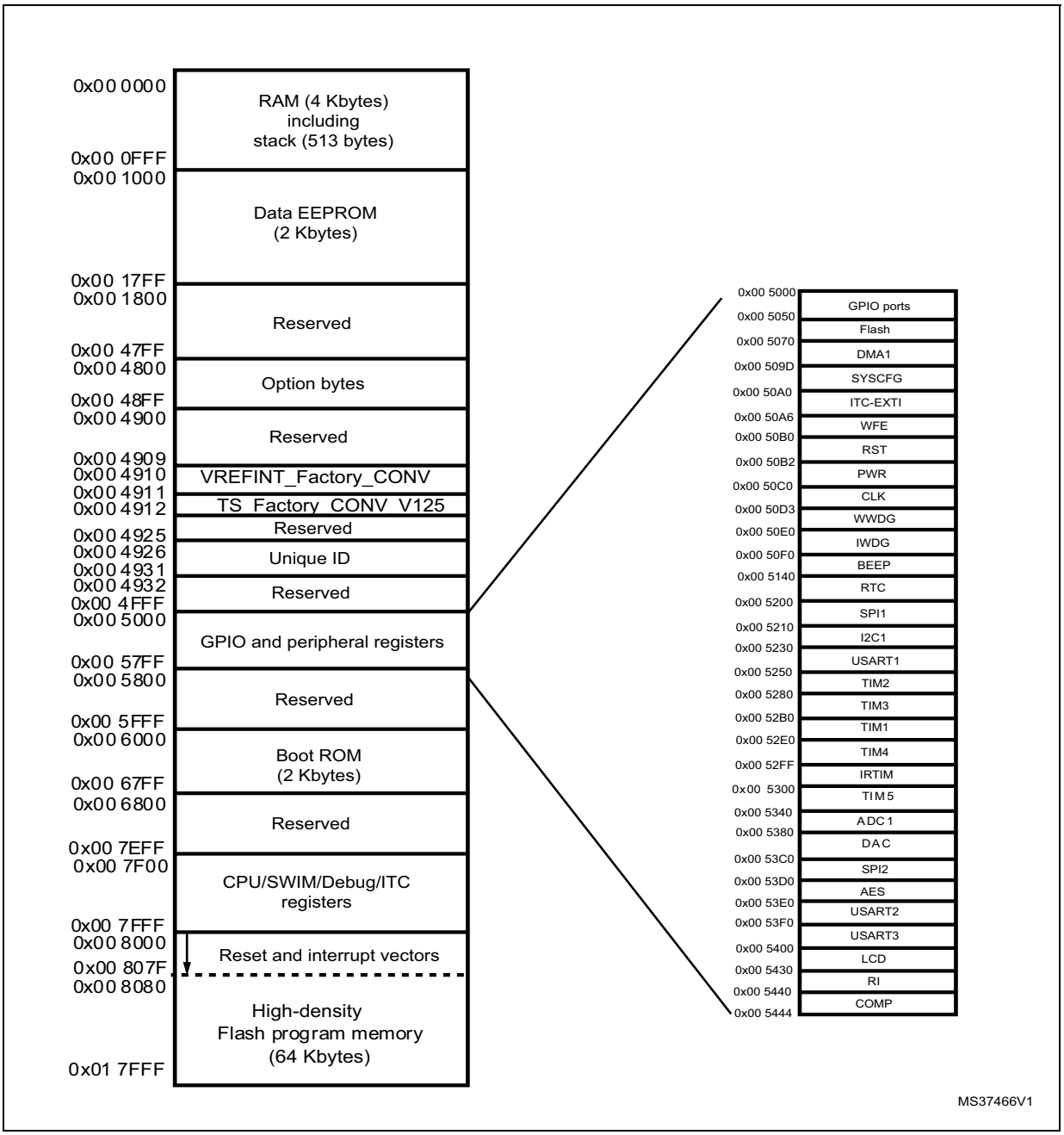
Pin number			Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP80	LQFP64	LQFP48				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
1	-	-	PH0/LCD SEG 36 (3)	I/O	FT(5)	**X**	X	X	HS	X	X	**Port H0**	LCD segment 36
2	-	-	PH1/LCD SEG 37 (3)	I/O	FT(5)	**X**	X	X	HS	X	X	**Port H1**	LCD segment 37
3	-	-	PH2/LCD SEG 38 (3)	I/O	FT(5)	**X**	X	X	HS	X	X	**Port H2**	LCD segment 38
4	-	-	PH3/LCD SEG 39 (3)	I/O	FT(5)	**X**	X	X	HS	X	X	**Port H3**	LCD segment 39
6	2	2	NRST/PA1(1)	I/O	-	-	**X**	-	HS	X	X	**Reset**	PA1
7	3	3	PA2/OSC_IN/ *[USART1_TX](2)/ [SPI1_MISO]* (2)	I/O	-	**X**	X	X	HS	X	X	**Port A2**	HSE oscillator input / *[USART1 transmit] / [SPI1 master in- slave out] /*
8	4	4	PA3/OSC_OUT/*[USART1 _RX](2)/[SPI1_MOSI](2)*	I/O	-	**X**	X	X	HS	X	X	**Port A3**	HSE oscillator output / *[USART1 receive]/ [SPI1 master out/slave in]/*
9	5	5	PA4/TIM2_BKIN/ *[TIM2_ETR](2)* LCD_COM0(3)/ADC1_IN2 COMP1_INP	I/O	FT(5)	**X**	X	X	HS	X	X	**Port A4**	Timer 2 - break input / */[Timer 2 - trigger] /* LCD COM 0 / ADC1 input 2/Comparator 1 positive input
10	6	6	PA5/TIM3_BKIN/ *[TIM3_ETR](2)/* LCD_COM1(3)/ADC1_IN1/ COMP1_INP	I/O	FT(5)	**X**	X	X	HS	X	X	**Port A5**	Timer 3 - break input / *[Timer 3 - trigger] /* LCD_COM 1 / ADC1 input 1/Comparator 1 positive input
11	7	7	PA6/ADC1_TRIG/ LCD_COM2(3)/ADC1_IN0/ COMP1_INP	I/O	FT(5)	**X**	X	X	HS	X	X	**Port A6**	ADC1 - trigger / LCD_COM2 / ADC1 input 0/Comparator 1 positive input

5 Memory and register map

5.1 Memory mapping

The memory map is shown in *Figure 9*.

Figure 9. Memory map



1. Refer to *Table 9* for an overview of hardware register mapping, to *Table 8* for details on I/O port hardware registers, and to *Table 10* for information on CPU/SWIM/debug module controller registers.

Table 8. I/O port hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 500F	Port D	PD_ODR	Port D data output latch register	0x00
0x00 5010		PD_IDR	Port D input pin value register	0xXX
0x00 5011		PD_DDR	Port D data direction register	0x00
0x00 5012		PD_CR1	Port D control register 1	0x00
0x00 5013		PD_CR2	Port D control register 2	0x00
0x00 5014	Port E	PE_ODR	Port E data output latch register	0x00
0x00 5015		PE_IDR	Port E input pin value register	0xXX
0x00 5016		PE_DDR	Port E data direction register	0x00
0x00 5017		PE_CR1	Port E control register 1	0x00
0x00 5018		PE_CR2	Port E control register 2	0x00
0x00 5019	Port F	PF_ODR	Port F data output latch register	0x00
0x00 501A		PF_IDR	Port F input pin value register	0xXX
0x00 501B		PF_DDR	Port F data direction register	0x00
0x00 501C		PF_CR1	Port F control register 1	0x00
0x00 501D		PF_CR2	Port F control register 2	0x00
0x00 501E	Port G	PG_ODR	Port F data output latch register	0x00
0x00 501F		PG_IDR	Port G input pin value register	0xXX
0x00 5020		PG_DDR	Port G data direction register	0x00
0x00 5021		PG_CR1	Port G control register 1	0x00
0x00 5022		PG_CR2	Port G control register 2	0x00
0x00 5023	Port H	PH_ODR	Port H data output latch register	0x00
0x00 5024		PH_IDR	Port H input pin value register	0xXX
0x00 5025		PH_DDR	Port H data direction register	0x00
0x00 5026		PH_CR1	Port H control register 1	0x00
0x00 5027		PH_CR2	Port H control register 2	0x00
0x00 5028	Port I	PI_ODR	Port I data output latch register	0x00
0x00 5029		PI_IDR	Port I input pin value register	0xXX
0x00 502A		PI_DDR	Port I data direction register	0x00
0x00 502B		PI_CR1	Port I control register 1	0x00
0x00 502C		PI_CR2	Port I control register 2	0x00

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 516A	RTC	RTC_CALRH	Calibration register high	0x00(1)
0x00 516B		RTC_CALRL	Calibration register low	0x00(1)
0x00 516C		RTC_TCR1	Tamper control register 1	0x00(1)
0x00 516D		RTC_TCR2	Tamper control register 2	0x00(1)
0x00 516E to 0x00 518A	Reserved area			
0x00 5190	CSSLSE	CSSLSE_CSR	CSS on LSE control and status register	0x00(1)
0x00 519A to 0x00 51FF	Reserved area			
0x00 5200	SPI1	SPI1_CR1	SPI1 control register 1	0x00
0x00 5201		SPI1_CR2	SPI1 control register 2	0x00
0x00 5202		SPI1_ICR	SPI1 interrupt control register	0x00
0x00 5203		SPI1_SR	SPI1 status register	0x02
0x00 5204		SPI1_DR	SPI1 data register	0x00
0x00 5205		SPI1_CRCPR	SPI1 CRC polynomial register	0x07
0x00 5206		SPI1_RXCRCR	SPI1 Rx CRC register	0x00
0x00 5207		SPI1_TXCRCR	SPI1 Tx CRC register	0x00
0x00 5208 to 0x00 520F	Reserved area (8 byte)			
0x00 5210	I2C1	I2C1_CR1	I2C1 control register 1	0x00
0x00 5211		I2C1_CR2	I2C1 control register 2	0x00
0x00 5212		I2C1_FREQR	I2C1 frequency register	0x00
0x00 5213		I2C1_OARL	I2C1 own address register low	0x00
0x00 5214		I2C1_OARH	I2C1 own address register high	0x00
0x00 5215		I2C1_OARH	I2C1 own address register for dual mode	0x00
0x00 5216		I2C1_DR	I2C1 data register	0x00
0x00 5217		I2C1_SR1	I2C1 status register 1	0x00
0x00 5218		I2C1_SR2	I2C1 status register 2	0x00
0x00 5219		I2C1_SR3	I2C1 status register 3	0x0X
0x00 521A		I2C1_ITR	I2C1 interrupt control register	0x00
0x00 521B		I2C1_CCRL	I2C1 clock control register low	0x00
0x00 521C		I2C1_CCRH	I2C1 clock control register high	0x00
0x00 521D		I2C1_TRISER	I2C1 TRISE register	0x02
0x00 521E		I2C1_PECR	I2C1 packet error checking register	0x00

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 52B0	TIM1	TIM1_CR1	TIM1 control register 1	0x00
0x00 52B1		TIM1_CR2	TIM1 control register 2	0x00
0x00 52B2		TIM1_SMCR	TIM1 Slave mode control register	0x00
0x00 52B3		TIM1_ETR	TIM1 external trigger register	0x00
0x00 52B4		TIM1_DER	TIM1 DMA1 request enable register	0x00
0x00 52B5		TIM1_IER	TIM1 Interrupt enable register	0x00
0x00 52B6		TIM1_SR1	TIM1 status register 1	0x00
0x00 52B7		TIM1_SR2	TIM1 status register 2	0x00
0x00 52B8		TIM1_EGR	TIM1 event generation register	0x00
0x00 52B9		TIM1_CCMR1	TIM1 Capture/Compare mode register 1	0x00
0x00 52BA		TIM1_CCMR2	TIM1 Capture/Compare mode register 2	0x00
0x00 52BB		TIM1_CCMR3	TIM1 Capture/Compare mode register 3	0x00
0x00 52BC		TIM1_CCMR4	TIM1 Capture/Compare mode register 4	0x00
0x00 52BD		TIM1_CCER1	TIM1 Capture/Compare enable register 1	0x00
0x00 52BE		TIM1_CCER2	TIM1 Capture/Compare enable register 2	0x00
0x00 52BF		TIM1_CNTRH	TIM1 counter high	0x00
0x00 52C0		TIM1_CNTRL	TIM1 counter low	0x00
0x00 52C1		TIM1_PSCRH	TIM1 prescaler register high	0x00
0x00 52C2		TIM1_PSCRL	TIM1 prescaler register low	0x00
0x00 52C3		TIM1_ARRH	TIM1 Auto-reload register high	0xFF
0x00 52C4		TIM1_ARRL	TIM1 Auto-reload register low	0xFF
0x00 52C5		TIM1_RCR	TIM1 Repetition counter register	0x00
0x00 52C6		TIM1_CCR1H	TIM1 Capture/Compare register 1 high	0x00
0x00 52C7		TIM1_CCR1L	TIM1 Capture/Compare register 1 low	0x00
0x00 52C8		TIM1_CCR2H	TIM1 Capture/Compare register 2 high	0x00
0x00 52C9		TIM1_CCR2L	TIM1 Capture/Compare register 2 low	0x00
0x00 52CA		TIM1_CCR3H	TIM1 Capture/Compare register 3 high	0x00
0x00 52CB		TIM1_CCR3L	TIM1 Capture/Compare register 3 low	0x00
0x00 52CC		TIM1_CCR4H	TIM1 Capture/Compare register 4 high	0x00
0x00 52CD		TIM1_CCR4L	TIM1 Capture/Compare register 4 low	0x00
0x00 52CE		TIM1_BKR	TIM1 break register	0x00
0x00 52CF		TIM1_DTR	TIM1 dead-time register	0x00
0x00 52D0		TIM1_OISR	TIM1 output idle state register	0x00
0x00 52D1		TIM1_DCR1	DMA1 control register 1	0x00

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 52D2	TIM1	TIM1_DCR2	TIM1 DMA1 control register 2	0x00
0x00 52D3		TIM1_DMA1R	TIM1 DMA1 address for burst mode	0x00
0x00 52D4 to 0x00 52DF	Reserved area (12 byte)			
0x00 52E0	TIM4	TIM4_CR1	TIM4 control register 1	0x00
0x00 52E1		TIM4_CR2	TIM4 control register 2	0x00
0x00 52E2		TIM4_SMCR	TIM4 Slave mode control register	0x00
0x00 52E3		TIM4_DER	TIM4 DMA1 request enable register	0x00
0x00 52E4		TIM4_IER	TIM4 Interrupt enable register	0x00
0x00 52E5		TIM4_SR1	TIM4 status register 1	0x00
0x00 52E6		TIM4_EGR	TIM4 Event generation register	0x00
0x00 52E7		TIM4_CNTR	TIM4 counter	0x00
0x00 52E8		TIM4_PSCR	TIM4 prescaler register	0x00
0x00 52E9		TIM4_ARR	TIM4 Auto-reload register	0x00
0x00 52EA to 0x00 52FE	Reserved area (21 byte)			
0x00 52FF	IRTIM	IR_CR	Infrared control register	0x00
0x00 5300	TIM5	TIM5_CR1	TIM5 control register 1	0x00
0x00 5301		TIM5_CR2	TIM5 control register 2	0x00
0x00 5302		TIM5_SMCR	TIM5 Slave mode control register	0x00
0x00 5303		TIM5_ETR	TIM5 external trigger register	0x00
0x00 5304		TIM5_DER	TIM5 DMA1 request enable register	0x00
0x00 5305		TIM5_IER	TIM5 interrupt enable register	0x00
0x00 5306		TIM5_SR1	TIM5 status register 1	0x00
0x00 5307		TIM5_SR2	TIM5 status register 2	0x00
0x00 5308		TIM5_EGR	TIM5 event generation register	0x00
0x00 5309		TIM5_CCMR1	TIM5 Capture/Compare mode register 1	0x00
0x00 530A		TIM5_CCMR2	TIM5 Capture/Compare mode register 2	0x00
0x00 530B		TIM5_CCER1	TIM5 Capture/Compare enable register 1	0x00
0x00 530C		TIM5_CNTRH	TIM5 counter high	0x00
0x00 530D		TIM5_CNTRL	TIM5 counter low	0x00
0x00 530E		TIM5_PSCR	TIM5 prescaler register	0x00
0x00 530F		TIM5_ARRH	TIM5 Auto-reload register high	0xFF

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5386 to 0x00 5387	Reserved area (2 byte)			
0x00 5388	DAC	DAC_CH1RDHRH	DAC channel 1 right aligned data holding register high	0x00
0x00 5389		DAC_CH1RDHRL	DAC channel 1 right aligned data holding register low	0x00
0x00 538A to 0x00 538B	Reserved area (2 byte)			
0x00 538C	DAC	DAC_CH1LDHRH	DAC channel 1 left aligned data holding register high	0x00
0x00 538D		DAC_CH1LDHRL	DAC channel 1 left aligned data holding register low	0x00
0x00 538E to 0x00 538F	Reserved area (2 byte)			
0x00 5390	DAC	DAC_CH1DHR8	DAC channel 1 8-bit data holding register	0x00
0x00 5391 to 0x00 5393	Reserved area (3 byte)			
0x00 5394	DAC	DAC_CH2RDHRH	DAC channel 2 right aligned data holding register high	0x00
0x00 5395		DAC_CH2RDHRL	DAC channel 2 right aligned data holding register low	0x00
0x00 5396 to 0x00 5397	Reserved area (2 byte)			
0x00 5398	DAC	DAC_CH2LDHRH	DAC channel 2 left aligned data holding register high	0x00
0x00 5399		DAC_CH2LDHRL	DAC channel 2 left aligned data holding register low	0x00
0x00 539A to 0x00 539B	Reserved area (2 byte)			
0x00 539C	DAC	DAC_CH2DHR8	DAC channel 2 8-bit data holding register	0x00
0x00 539D to 0x00 539F	Reserved area (3 byte)			
0x00 53A0	DAC	DAC_DCH1RDHRH	DAC channel 1 right aligned data holding register high	0x00
0x00 53A1		DAC_DCH1RDHRL	DAC channel 1 right aligned data holding register low	0x00
0x00 53A2 to 0x00 53AB	Reserved area (3 byte)			

Table 10. CPU/SWIM/debug module/interrupt controller registers (continued)

Address	Block	Register label	Register name	Reset status
0x00 7F90	DM	DM_BK1RE	DM breakpoint 1 register extended byte	0xFF
0x00 7F91		DM_BK1RH	DM breakpoint 1 register high byte	0xFF
0x00 7F92		DM_BK1RL	DM breakpoint 1 register low byte	0xFF
0x00 7F93		DM_BK2RE	DM breakpoint 2 register extended byte	0xFF
0x00 7F94		DM_BK2RH	DM breakpoint 2 register high byte	0xFF
0x00 7F95		DM_BK2RL	DM breakpoint 2 register low byte	0xFF
0x00 7F96		DM_CR1	DM Debug module control register 1	0x00
0x00 7F97		DM_CR2	DM Debug module control register 2	0x00
0x00 7F98		DM_CSR1	DM Debug module control/status register 1	0x10
0x00 7F99		DM_CSR2	DM Debug module control/status register 2	0x00
0x00 7F9A		DM_ENFCTR	DM enable function register	0xFF
0x00 7F9B to 0x00 7F9F	Reserved area (5 byte)			

1. Accessible by debug module only

Table 11. Interrupt mapping (continued)

IRQ No.	Source block	Description	Wakeup from Halt mode	Wakeup from Active-halt mode	Wakeup from Wait (WFI mode)	Wakeup from Wait (WFE mode)(1)	Vector address
19	TIM2/ USART2	TIM2 update /overflow/trigger/break/ USART2 transmission complete/transmit data register empty interrupt	-	-	Yes	Yes(3)	0x00 8054
20	TIM2/ USART2	Capture/Compare/USART 2 interrupt	-	-	Yes	Yes(3)	0x00 8058
21	TIM3/ USART3	TIM3 Update /Overflow/Trigger/Break/ USART3 transmission complete/transmit data register empty interrupt	-	-	Yes	Yes(3)	0x00 805C
22	TIM3/ USART3	TIM3 Capture/Compare/ USART3 Receive register data full/overrun/idle line detected/parity error/ interrupt	-	-	Yes	Yes(3)	0x00 8060
23	TIM1	Update /overflow/trigger/ COM	-	-	-	Yes(3)	0x00 8064
24	TIM1	Capture/Compare	-	-	-	Yes(3)	0x00 8068
25	TIM4	Update/overflow/trigger	-	-	Yes	Yes(3)	0x00 806C
26	SPI1	End of Transfer	Yes	Yes	Yes	Yes(3)	0x00 8070
27	USART 1/ TIM5	USART1 transmission complete/transmit data register empty/ TIM5 update/overflow/ trigger/break	-	-	Yes	Yes(3)	0x00 8074
28	USART 1/ TIM5	USART1 Receive register data full/overrun/idle line detected/parity error/ TIM5 capture/compare	-	-	Yes	Yes(3)	0x00 8078
29	I^2C1/SPI2	I^2C1 interrupt(5)/ SPI2	Yes	Yes	Yes	Yes(3)	0x00 807C

1. The Low-power wait mode is entered when executing a WFE instruction in Low-power run mode.
2. The TLI interrupt is the logic OR between TIM2 overflow interrupt, and TIM4 overflow interrupts.
3. In WFE mode, this interrupt is served if it has been previously enabled. After processing the interrupt, the processor goes back to WFE mode. When this interrupt is configured as a wakeup event, the CPU wakes up and resumes processing.
4. The interrupt from PVD is logically OR-ed with Port E and F interrupts. Register EXTI_CONF allows to select between Port E and Port F interrupt. See more details about the external interrupt port select register (EXTI_CONF) in the STM8L051/L052 Value Line, STM8L151/L152, STM8L162, STM8AL31, STM8AL3L MCU lines reference manual (RM0031).
5. The device is woken up from Halt or Active-halt mode only when the address received matches the interface address.

7 Option byte

Option byte contain configurations for device hardware features as well as the memory protection of the device. They are stored in a dedicated memory block.

All option byte can be modified in ICP mode (with SWIM) by accessing the EEPROM address. See *Table 12* for details on option byte addresses.

The option byte can also be modified 'on the fly' by the application in IAP mode, except for the ROP, UBC and PCODESIZE values which are only taken into account when they are modified in ICP mode (with the SWIM).

Refer to the STM8AL31E8x/STM8AL3LE8x Flash programming manual (PM0054) and STM8 SWIM and Debug Manual (UM0470) for information on SWIM programming procedures.

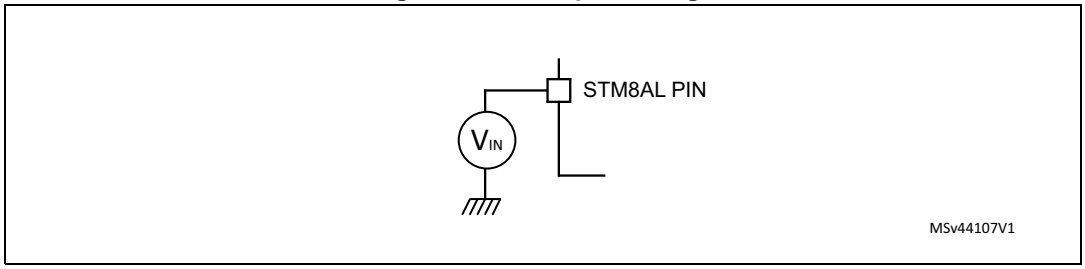
Table 12. Option byte addresses

Address	Option name	Option byte No.	Option bits								Factory default setting
			7	6	5	4	3	2	1	0	
00 4800	Read-out protection (ROP)	OPT0	ROP[7:0]								0xAA
00 4802	UBC (User Boot code size)	OPT1	UBC[7:0]								0x00
00 4807	PCODESIZE	OPT2	PCODE[7:0]								0x00
00 4808	Independent watchdog option	OPT3 [3:0]	Reserved				WWDG _HALT	WWDG _HW	IWDG _HALT	IWDG _HW	0x00
00 4809	Number of stabilization clock cycles for HSE and LSE oscillators	OPT4	Reserved				LSECNT[1:0]		HSECNT[1:0]		0x00
00 480A	Brownout reset (BOR)	OPT5 [3:0]	Reserved				BOR_TH			BOR_ ON	0x01
00 480B	Bootloader option byte (OPTBL)	OPTBL [15:0]	OPTBL[15:0]								0x00
00 480C											0x00

9.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 11*.

Figure 11. Pin input voltage



9.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 15: Voltage characteristics*, *Table 16: Current characteristics* and *Table 17: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only, and a functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods of time may affect the device's reliability.

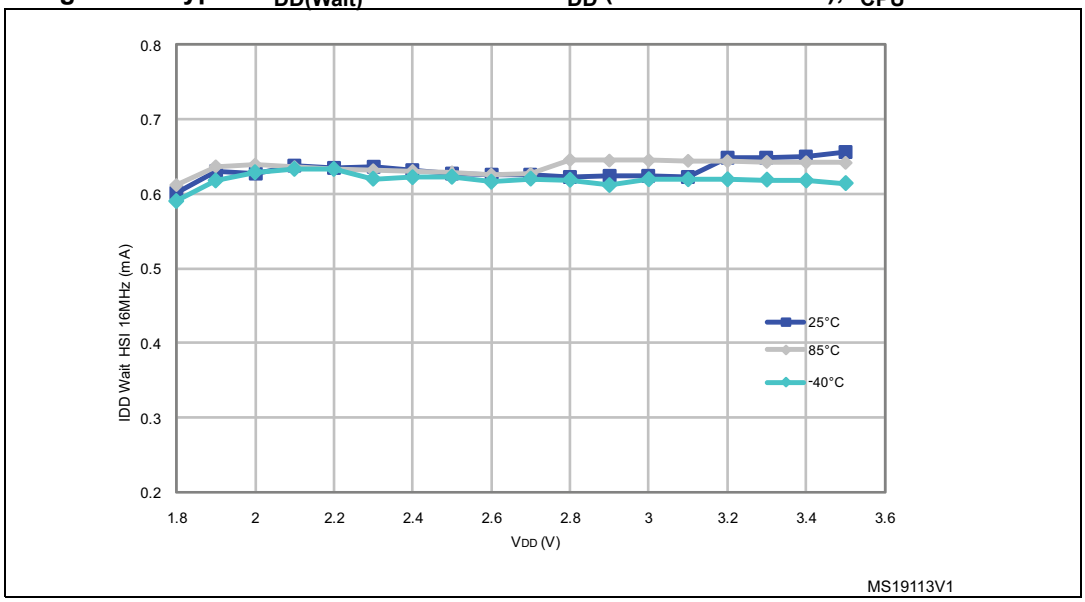
The device's mission profile (application conditions) is compliant with the JEDEC JESD47 qualification standard, its extended mission profiles are available on demand.

Table 15. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}- V_{SS}	External supply voltage (including V_{DDA})(1)	- 0.3	4.0	V
V_{IN}(2)	Input voltage on true open-drain pins (PC0 and PC1)	V_{SS} - 0.3	V_{DD} + 4.0	
	Input voltage on five-volt tolerant (FT) pins		V_{DD} + 4.0	
	Input voltage on any other pin		4.0	
V_{ESD}	Electrostatic discharge voltage	see *Absolute maximum ratings (electrical sensitivity) on page 118*		

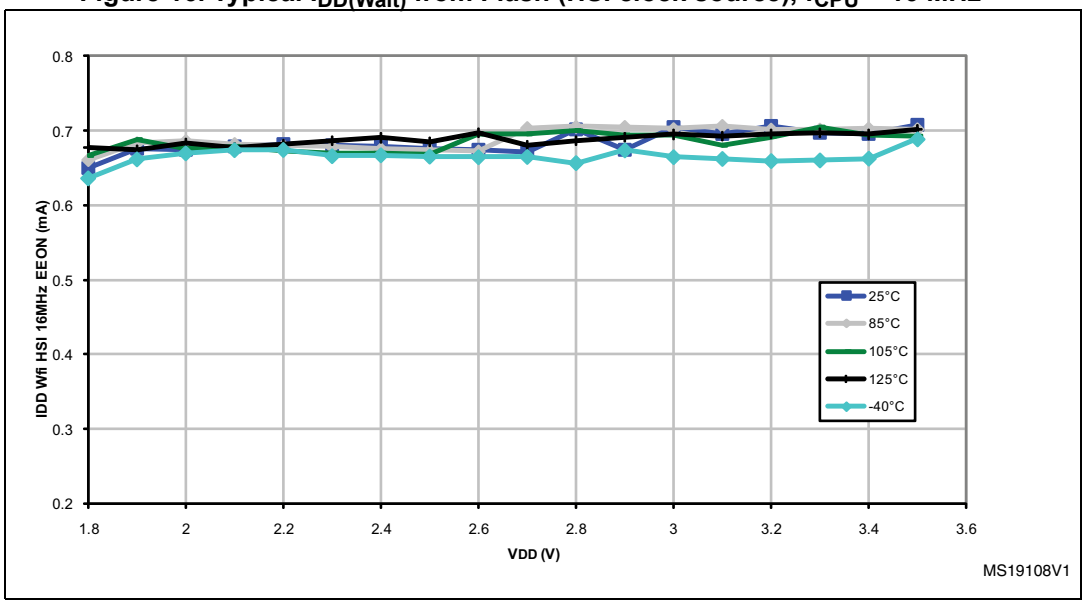
1. All power (V_{DD1}, V_{DD2}, V_{DD3}, V_{DD4}, V_{DDA}) and ground (V_{SS1}, V_{SS2}, V_{SS3}, V_{SS4}, V_{SSA}) pins must always be connected to the external power supply.
2. V_{IN} maximum must always be respected. Refer to *Table 16.* for maximum allowed injected current values.

Figure 15. Typical $I_{DD(Wait)}$ from RAM vs. V_{DD} (HSI clock source), f_{CPU} = 16 MHz(1)



1. Typical current consumption measured with code executed from RAM.

Figure 16. Typical $I_{DD(Wait)}$ from Flash (HSI clock source), f_{CPU} = 16 MHz(1)



1. Typical current consumption measured with code executed from Flash.

Table 28. Peripheral current consumption (continued)

Symbol	Parameter		Typ. V_{DD} = 3.0 V	Unit
$I_{DD(TIM1)}$	TIM1 supply current(1)		10	µA/MHz
$I_{DD(TIM2)}$	TIM2 supply current (4)		7	
$I_{DD(TIM3)}$	TIM3 supply current (1)		7	
$I_{DD(TIM5)}$	TIM5 supply current (1)		7	
$I_{DD(TIM4)}$	TIM4 timer supply current (1)		3	
$I_{DD(USART1)}$	USART1 supply current (5)		5	
$I_{DD(USART2)}$	USART2 supply current (6)		5	
$I_{DD(USART3)}$	USART3 supply current (7)		5	
$I_{DD(SPI1)}$	SPI1 supply current (4)		3	
$I_{DD(SPI2)}$	SPI2 supply current (4)		3	
$I_{DD(I2C1)}$	I^2C1 supply current (4)		4	
$I_{DD(DMA1)}$	DMA1 supply current		3	
$I_{DD(AES)}$	AES supply current		4	
$I_{DD(WWDG)}$	WWDG supply current		1	
$I_{DD(ALL)}$	Peripherals ON(8)		67	
$I_{DD(ADC1)}$	ADC1 supply current(9)		1500	µA
$I_{DD(DAC)}$	DAC supply current(10)		370	
$I_{DD(COMP1)}$	Comparator 1 supply current(11)		0.160	
$I_{DD(COMP2)}$	Comparator 2 supply current(11)	Slow mode	2	
		Fast mode	5	
$I_{DD(PVD/BOR)}$	Power voltage detector and brownout Reset unit supply current (12)		2.6	
$I_{DD(BOR)}$	Brownout Reset unit supply current (12)		2.4	
$I_{DD(IDWDG)}$	Independent watchdog supply current	including LSI supply current	0.45	
		excluding LSI supply current	0.05	

1. Data based on a differential I_{DD} measurement between all peripherals OFF and a timer counter running at 16 MHz. The CPU is in Wait mode in both cases. No IC/OC programmed, no I/O pins toggling. Not tested in production.
2. Data based on a differential I_{DD} measurement between the on-chip peripheral in reset configuration and not clocked and the on-chip peripheral when clocked and not kept under reset. The CPU is in Wait mode in both cases. No I/O pins toggling. Not tested in production.
3. Peripherals listed above the $I_{DD(ALL)}$ parameter ON: TIM1, TIM2, TIM3, TIM4, TIM5, USART1, USART2, USART3, SPI1, SPI2, I2C1, DMA1, WWDG.
4. Data based on a differential I_{DD} measurement between all peripherals OFF and a timer counter running at 16 MHz. The CPU is in Wait mode in both cases. No IC/OC programmed, no I/O pins toggling. Not tested in production.

9.3.8 Communication interfaces

SPI1 - Serial peripheral interface

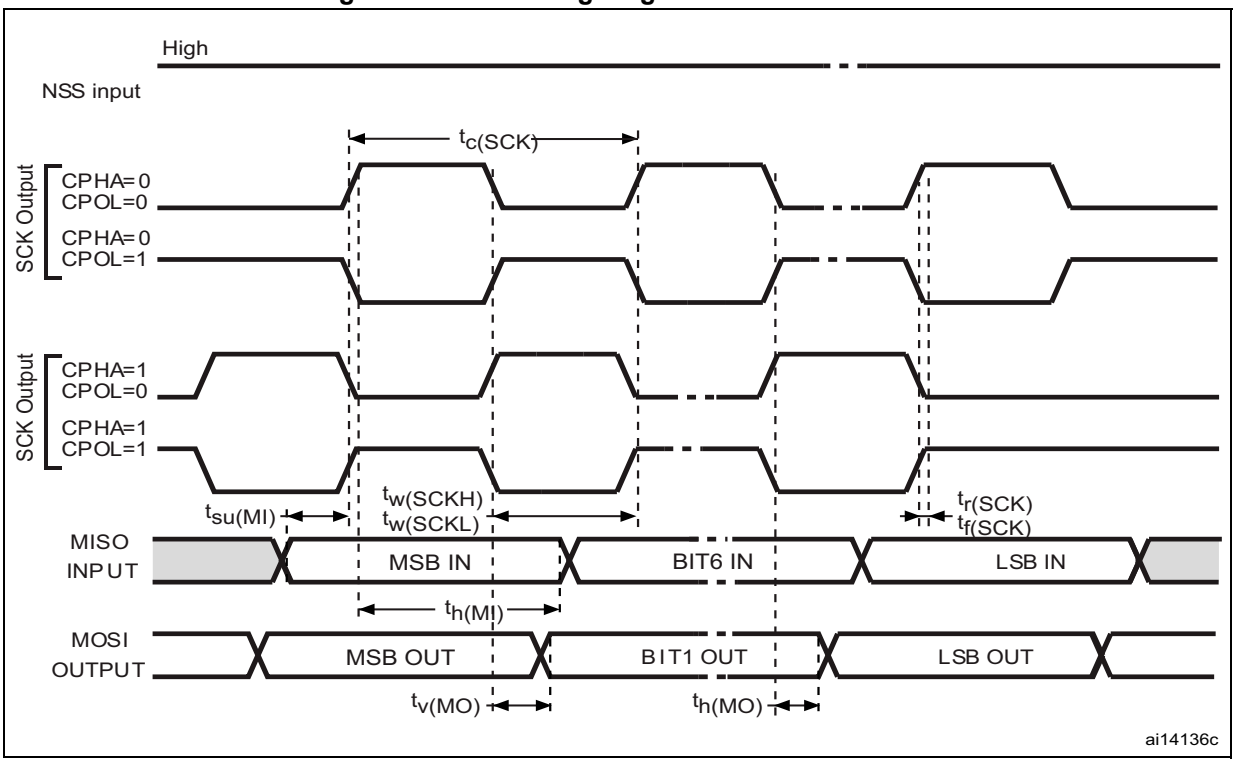
Unless otherwise specified, the parameters given in *Table 46* are derived from tests performed under ambient temperature, f_{SYSCLK} frequency and V_{DD} supply voltage conditions summarized in *Section 9.3.1*. Refer to I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 46. SPI1 characteristics

Symbol	Parameter	Conditions(1)	Min.	Max.	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI1 clock frequency	Master mode	0	8	MHz
		Slave mode	0	8	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI1 clock rise and fall time	Capacitive load: C = 30 pF	-	30	ns
$t_{su(NSS)}$(2)	NSS setup time	Slave mode	4 x $1/f_{SYSCLK}$	-	
$t_{h(NSS)}$(2)	NSS hold time	Slave mode	80	-	
$t_{w(SCKH)}$(2) $t_{w(SCKL)}$(2)	SCK high and low time	Master mode, f_{MASTER} = 8 MHz, f_{SCK}= 4 MHz	105	145	
$t_{su(MI)}$(2) $t_{su(SI)}$(2)	Data input setup time	Master mode	30	-	
		Slave mode	3	-	
$t_{h(MI)}$(2) $t_{h(SI)}$(2)	Data input hold time	Master mode	15	-	
		Slave mode	0	-	
$t_{a(SO)}$(2)(3)	Data output access time	Slave mode	-	3x $1/f_{SYSCLK}$	
$t_{dis(SO)}$(2)(4)	Data output disable time	Slave mode	30	-	
$t_{v(SO)}$(2)	Data output valid time	Slave mode (after enable edge)	-	60	
$t_{v(MO)}$(2)	Data output valid time	Master mode (after enable edge)	-	20	
$t_{h(SO)}$(2)	Data output hold time	Slave mode (after enable edge)	15	-	
$t_{h(MO)}$(2)		Master mode (after enable edge)	1	-	

1. Parameters are given by selecting 10 MHz I/O output frequency.
2. Guaranteed by characterization results or by design.
3. Min. time is for the minimum time to drive the output and max. time is for the maximum time to validate the data.
4. Min. time is for the minimum time to invalidate the output and max. time is for the maximum time to put the data in Hi-Z.

Figure 40. SPI1 timing diagram - master mode(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

9.3.9 LCD controller (STM8AL3LE8x only)

In the following table, data are guaranteed by design, not tested in production.

Table 48. LCD characteristics

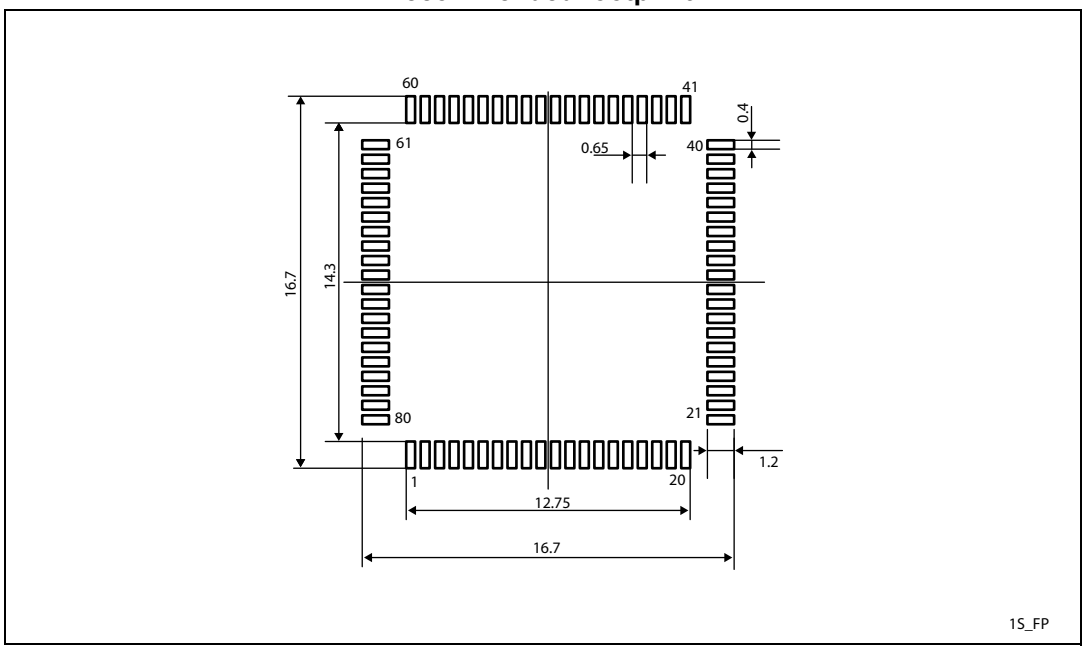
Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{LCD}	LCD external voltage	-	-	3.6	V
V_{LCD0}	LCD internal reference voltage 0	-	2.6	-	
V_{LCD1}	LCD internal reference voltage 1	-	2.7	-	
V_{LCD2}	LCD internal reference voltage 2	-	2.8	-	
V_{LCD3}	LCD internal reference voltage 3	-	3.0	-	
V_{LCD4}	LCD internal reference voltage 4	-	3.1	-	
V_{LCD5}	LCD internal reference voltage 5	-	3.2	-	
V_{LCD6}	LCD internal reference voltage 6	-	3.4	-	
V_{LCD7}	LCD internal reference voltage 7	-	3.5	-	
C_{EXT}	V_{LCD} external capacitance	0.1	1	2	µF
I_{DD}	Supply current(1) at V_{DD} = 1.8 V	-	3	-	µA
	Supply current(1) at V_{DD} = 3 V	-	3	-	
R_{HN}(2)	High value resistive network (low drive)	-	6.6	-	MΩ
R_{LN}(3)	Low value resistive network (high drive)	-	240	-	kΩ
V_{33}	Segment/Common higher level voltage	-	-	V_{LCDx}	V
V_{34}	Segment/Common 3/4 level voltage	-	$3/4V_{LCDx}$	-	
V_{23}	Segment/Common 2/3 level voltage	-	$2/3V_{LCDx}$	-	
V_{12}	Segment/Common 1/2 level voltage	-	$1/2V_{LCDx}$	-	
V_{13}	Segment/Common 1/3 level voltage	-	$1/3V_{LCDx}$	-	
V_{14}	Segment/Common 1/4 level voltage	-	$1/4V_{LCDx}$	-	
V_0	Segment/Common lowest level voltage	0	-	-	

1. LCD enabled with 3 V internal booster (LCD_CR1 = 0x08), 1/4 duty, 1/3 bias, division ratio= 64, all pixels active, no LCD connected.
2. R_{HN} is the total high value resistive network.
3. R_{LN} is the total low value resistive network.

VLCD external capacitor (STM8AL3LE8x only)

The application achieves a stabilized LCD reference voltage when connecting an external capacitor C_{EXT} to the V_{LCD} pin. C_{EXT} is specified in *Table 48*.

Figure 47. LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

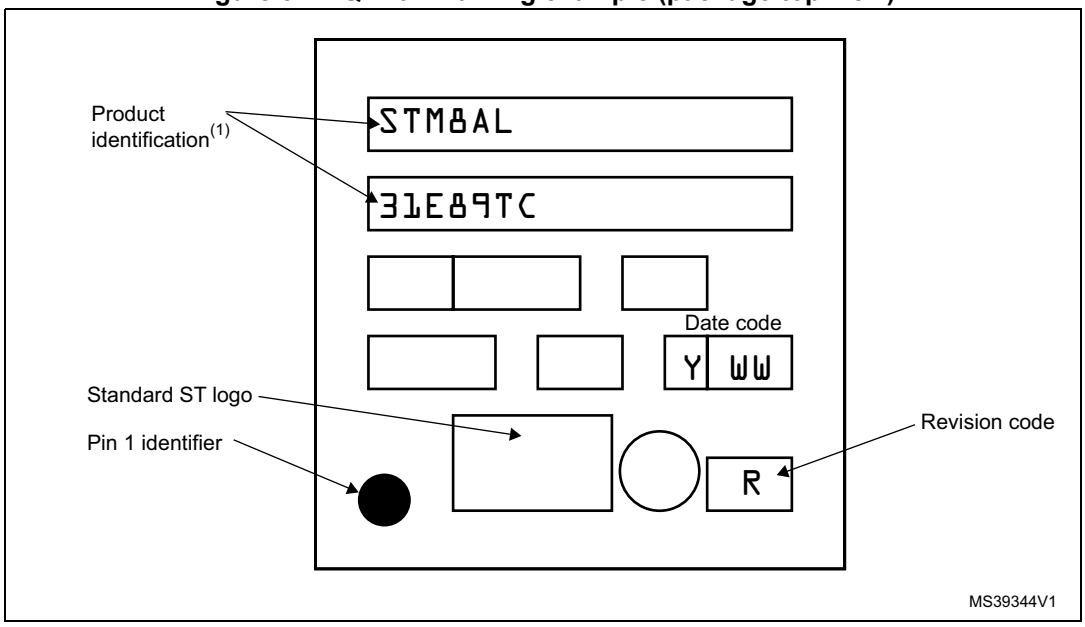
Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 51. LQFP64 marking example (package top view)



1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted to run a qualification activity prior to any decision to use these engineering samples.

12 Revision history

Table 69. Document revision history

Date	Revision	Changes
22-Apr-2015	1	Initial release.
27-Jul-2015	2	Updated the document confidentiality level to “Public”. No other changes in the content.
19-Aug-2015	3	Changed datasheet status to “production data”. Added LQFP64 and LQFP80 packages together with the corresponding part numbers.
18-Oct-2016	4	– Updated *Table 5: High-density STM8AL3xE8x pin description*: pin name changed from PC3/USART1_TX/LCD_SEG23(3)/ADC1_IN5/COMP_IN3M/COMP2_INM/COMP1_INP to PC3/USART1_TX/LCD_SEG23(3)/ADC1_IN5/COMP2_INM/COMP1_INP. – Added footnote to *Table 68: STM8AL31E8x STM8AL3LE8x ordering information scheme*. – Updated *Section : Device marking on page 122*, *Section : Device marking on page 126*, *Section : Device marking on page 130* – Updated *Section 9.2: Absolute maximum ratings* – Updated *Figure 12: Power supply thresholds*.
5-Dec-2016	5	– Updated *Table 5: High-density STM8AL3xE8x pin description*: two pin names changed from PI0/RTC_TAMP1/[SPI2_NSS]/[TIM3_CH3 to PI0/RTC_TAMP1/[SPI2_NSS]/[TIM3_CH1 and from PF2/ADC1_IN26/[SPI2_SCK]/[USART3_SCK] to PF2/ADC1_IN26/[SPI1_SCK]/[USART3_SCK]