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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	41
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 25x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8al3l88tay

3.9 Analog-to-digital converter

- 12-bit analog-to-digital converter (ADC1) with 28 channels (including 4 fast channel), temperature sensor and internal reference voltage
- Conversion time down to 1 µs with f_{SYSCLK}= 16 MHz
- Programmable resolution
- Programmable sampling time
- Single and continuous mode of conversion
- Scan capability: automatic conversion performed on a selected group of analog inputs
- Analog watchdog: interrupt generation when the converted voltage is outside the programmed threshold
- Triggered by timer

Note: ADC1 can be served by DMA1.

3.10 Digital-to-analog converter

- 12-bit DAC with 2 buffered outputs (two digital signals are converted into two analog voltage signal outputs)
- Synchronized update capability using timers
- DMA capability for each channel
- External triggers for conversion
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channels with independent or simultaneous conversions
- Input reference voltage V_{REF+} for better resolution

Note: DAC can be served by DMA1.

3.11 Ultra-low-power comparators

The high-density STM8AL3xE8x devices embed two comparators (COMP1 and COMP2) sharing the same current bias and voltage reference. The voltage reference is an internal or external (coming from an I/O).

- One comparator with fixed threshold (COMP1).
- One comparator rail to rail with fast or slow mode (COMP2). The threshold is one of the following:
  - DAC output
  - External I/O
  - Internal reference voltage or internal reference voltage submultiple (1/4, 1/2, 3/4)

The two comparators are usable together to offer a window function. They wake up from Halt mode.

Bootloader

A bootloader is available to reprogram the Flash memory using the USART1, USART2, USART3 (USARTs in asynchronous mode), SPI1 or SPI2 interfaces.

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 516A	RTC	RTC_CALRH	Calibration register high	0x00(1)
0x00 516B		RTC_CALRL	Calibration register low	0x00(1)
0x00 516C		RTC_TCR1	Tamper control register 1	0x00(1)
0x00 516D		RTC_TCR2	Tamper control register 2	0x00(1)
0x00 516E to 0x00 518A	Reserved area			
0x00 5190	CSSLSE	CSSLSE_CSR	CSS on LSE control and status register	0x00(1)
0x00 519A to 0x00 51FF	Reserved area			
0x00 5200	SPI1	SPI1_CR1	SPI1 control register 1	0x00
0x00 5201		SPI1_CR2	SPI1 control register 2	0x00
0x00 5202		SPI1_ICR	SPI1 interrupt control register	0x00
0x00 5203		SPI1_SR	SPI1 status register	0x02
0x00 5204		SPI1_DR	SPI1 data register	0x00
0x00 5205		SPI1_CRCPR	SPI1 CRC polynomial register	0x07
0x00 5206		SPI1_RXCRCR	SPI1 Rx CRC register	0x00
0x00 5207		SPI1_TXCRCR	SPI1 Tx CRC register	0x00
0x00 5208 to 0x00 520F	Reserved area (8 byte)			
0x00 5210	I2C1	I2C1_CR1	I2C1 control register 1	0x00
0x00 5211		I2C1_CR2	I2C1 control register 2	0x00
0x00 5212		I2C1_FREQR	I2C1 frequency register	0x00
0x00 5213		I2C1_OARL	I2C1 own address register low	0x00
0x00 5214		I2C1_OARH	I2C1 own address register high	0x00
0x00 5215		I2C1_OARH	I2C1 own address register for dual mode	0x00
0x00 5216		I2C1_DR	I2C1 data register	0x00
0x00 5217		I2C1_SR1	I2C1 status register 1	0x00
0x00 5218		I2C1_SR2	I2C1 status register 2	0x00
0x00 5219		I2C1_SR3	I2C1 status register 3	0x0X
0x00 521A		I2C1_ITR	I2C1 interrupt control register	0x00
0x00 521B		I2C1_CCRL	I2C1 clock control register low	0x00
0x00 521C		I2C1_CCRH	I2C1 clock control register high	0x00
0x00 521D		I2C1_TRISER	I2C1 TRISE register	0x02
0x00 521E		I2C1_PECR	I2C1 packet error checking register	0x00

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5262	TIM2	TIM2_CCR1L	TIM2 capture/compare register 1 low	0x00
0x00 5263		TIM2_CCR2H	TIM2 capture/compare register 2 high	0x00
0x00 5264		TIM2_CCR2L	TIM2 capture/compare register 2 low	0x00
0x00 5265		TIM2_BKR	TIM2 break register	0x00
0x00 5266		TIM2_OISR	TIM2 output idle state register	0x00
0x00 5267 to 0x00 527F	Reserved area (25 byte)			
0x00 5280	TIM3	TIM3_CR1	TIM3 control register 1	0x00
0x00 5281		TIM3_CR2	TIM3 control register 2	0x00
0x00 5282		TIM3_SMCR	TIM3 Slave mode control register	0x00
0x00 5283		TIM3_ETR	TIM3 external trigger register	0x00
0x00 5284		TIM3_DER	TIM3 DMA1 request enable register	0x00
0x00 5285		TIM3_IER	TIM3 interrupt enable register	0x00
0x00 5286		TIM3_SR1	TIM3 status register 1	0x00
0x00 5287		TIM3_SR2	TIM3 status register 2	0x00
0x00 5288		TIM3_EGR	TIM3 event generation register	0x00
0x00 5289		TIM3_CCMR1	TIM3 Capture/Compare mode register 1	0x00
0x00 528A		TIM3_CCMR2	TIM3 Capture/Compare mode register 2	0x00
0x00 528B		TIM3_CCER1	TIM3 Capture/Compare enable register 1	0x00
0x00 528C		TIM3_CNTRH	TIM3 counter high	0x00
0x00 528D		TIM3_CNTRL	TIM3 counter low	0x00
0x00 528E		TIM3_PSCR	TIM3 prescaler register	0x00
0x00 528F		TIM3_ARRH	TIM3 Auto-reload register high	0xFF
0x00 5290		TIM3_ARRL	TIM3 Auto-reload register low	0xFF
0x00 5291		TIM3_CCR1H	TIM3 Capture/Compare register 1 high	0x00
0x00 5292		TIM3_CCR1L	TIM3 Capture/Compare register 1 low	0x00
0x00 5293		TIM3_CCR2H	TIM3 Capture/Compare register 2 high	0x00
0x00 5294		TIM3_CCR2L	TIM3 Capture/Compare register 2 low	0x00
0x00 5295		TIM3_BKR	TIM3 break register	0x00
0x00 5296		TIM3_OISR	TIM3 output idle state register	0x00
0x00 5297 to 0x00 52AF	Reserved area (25 byte)			

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5422 to 0x00 542E	Reserved area			
0x00 542F	LCD	LCD_CR4	LCD control register 4	0x00
0x00 5430	RI	Reserved area (1 byte)		0x00
0x00 5431		RI_ICR1	Timer input capture routing register 1	0x00
0x00 5432		RI_ICR2	Timer input capture routing register 2	0x00
0x00 5433		RI_IOIR1	I/O input register 1	0xXX
0x00 5434		RI_IOIR2	I/O input register 2	0xXX
0x00 5435		RI_IOIR3	I/O input register 3	0xXX
0x00 5436		RI_IOCMR1	I/O control mode register 1	0x00
0x00 5437		RI_IOCMR2	I/O control mode register 2	0x00
0x00 5438		RI_IOCMR3	I/O control mode register 3	0x00
0x00 5439		RI_IOSR1	I/O switch register 1	0x00
0x00 543A		RI_IOSR2	I/O switch register 2	0x00
0x00 543B		RI_IOSR3	I/O switch register 3	0x00
0x00 543C		RI_IOGCR	I/O group control register	0x3F
0x00 543D		RI_ASCR1	Analog switch register 1	0x00
0x00 543E		RI_ASCR2	Analog switch register 2	0x00
0x00 543F		RI_RCR	Resistor control register 1	0x00
0x00 5440	COMP1/ COMP2	COMP_CSR1	Comparator control and status register 1	0x00
0x00 5441		COMP_CSR2	Comparator control and status register 2	0x00
0x00 5442		COMP_CSR3	Comparator control and status register 3	0x00
0x00 5443		COMP_CSR4	Comparator control and status register 4	0x00
0x00 5444		COMP_CSR5	Comparator control and status register 5	0x00

1. These registers are not impacted by a system reset. They are reset at power-on.

Table 10. CPU/SWIM/debug module/interrupt controller registers

Address	Block	Register label	Register name	Reset status
0x00 7F00	CPU(1)	A	Accumulator	0x00
0x00 7F01		PCE	Program counter extended	0x00
0x00 7F02		PCH	Program counter high	0x00
0x00 7F03		PCL	Program counter low	0x00
0x00 7F04		XH	X index register high	0x00
0x00 7F05		XL	X index register low	0x00
0x00 7F06		YH	Y index register high	0x00
0x00 7F07		YL	Y index register low	0x00
0x00 7F08		SPH	Stack pointer high	0x03
0x00 7F09		SPL	Stack pointer low	0xFF
0x00 7F0A		CCR	Condition code register	0x28
0x00 7F0B to 0x00 7F5F	Reserved area (85 byte)			
0x00 7F60	CPU	CFG_GCR	Global configuration register	0x00
0x00 7F70	ITC-SPR	ITC_SPR1	Interrupt Software priority register 1	0xFF
0x00 7F71		ITC_SPR2	Interrupt Software priority register 2	0xFF
0x00 7F72		ITC_SPR3	Interrupt Software priority register 3	0xFF
0x00 7F73		ITC_SPR4	Interrupt Software priority register 4	0xFF
0x00 7F74		ITC_SPR5	Interrupt Software priority register 5	0xFF
0x00 7F75		ITC_SPR6	Interrupt Software priority register 6	0xFF
0x00 7F76		ITC_SPR7	Interrupt Software priority register 7	0xFF
0x00 7F77		ITC_SPR8	Interrupt Software priority register 8	0xFF
0x00 7F78 to 0x00 7F79	Reserved area (2 byte)			
0x00 7F80	SWIM	SWIM_CSR	SWIM control status register	0x00
0x00 7F81 to 0x00 7F8F	Reserved area (15 byte)			

6 Interrupt vector mapping

Note: Slope control of all GPIO pins can be programmed except true open drain pins and by default is limited to 2 MHz.

Table 11. Interrupt mapping

IRQ No.	Source block	Description	Wakeup from Halt mode	Wakeup from Active-halt mode	Wakeup from Wait (WFI mode)	Wakeup from Wait (WFE mode)(1)	Vector address
	RESET	Reset	Yes	Yes	Yes	Yes	0x00 8000
	TRAP	Software interrupt	-	-	-	-	0x00 8004
0	TLI(2)	External Top level Interrupt	-	-	-	-	0x00 8008
1	FLASH	EOP/WR_PG_DIS	-	-	Yes	Yes(3)	0x00 800C
2	DMA1 0/1	DMA1 channels 0/1	-	-	Yes	Yes(3)	0x00 8010
3	DMA1 2/3	DMA1 channels 2/3	-	-	Yes	Yes(3)	0x00 8014
4	RTC/LSE_ CSS	RTC alarm interrupt/LSE CSS interrupt	Yes	Yes	Yes	Yes	0x00 8018
5	EXTI E/F/PVD(4)	PortE/F interrupt/PVD interrupt	Yes	Yes	Yes	Yes(3)	0x00 801C
6	EXTIB/G	External interrupt port B/G	Yes	Yes	Yes	Yes(3)	0x00 8020
7	EXTID/H	External interrupt port D/H	Yes	Yes	Yes	Yes(3)	0x00 8024
8	EXTI0	External interrupt 0	Yes	Yes	Yes	Yes(3)	0x00 8028
9	EXTI1	External interrupt 1	Yes	Yes	Yes	Yes(3)	0x00 802C
10	EXTI2	External interrupt 2	Yes	Yes	Yes	Yes(3)	0x00 8030
11	EXTI3	External interrupt 3	Yes	Yes	Yes	Yes(3)	0x00 8034
12	EXTI4	External interrupt 4	Yes	Yes	Yes	Yes(3)	0x00 8038
13	EXTI5	External interrupt 5	Yes	Yes	Yes	Yes(3)	0x00 803C
14	EXTI6	External interrupt 6	Yes	Yes	Yes	Yes(3)	0x00 8040
15	EXTI7	External interrupt 7	Yes	Yes	Yes	Yes(3)	0x00 8044
16	LCD/AES	LCD interrupt/AES interrupt	-	-	Yes	Yes	0x00 8048
17	CLK/ TIM1/ DAC	System clock switch/CSS interrupt/TIM1 break/DAC	-	-	Yes	Yes	0x00 804C
18	COMP1/ COMP2 ADC1	Comparator 1 and 2 interrupt/ADC1	Yes	Yes	Yes	Yes(3)	0x00 8050

8 Unique ID

STM8 devices feature a 96-bit unique device identifier which provides a reference number that is unique for any device and in any context. The 96 bits of the identifier are never altered by the user.

The unique device identifier is read in single byte and may then be concatenated using a custom algorithm.

The unique device identifier is ideally suited:

- For use as serial numbers
- For use as security keys to increase the code security in the program memory while using and combining this unique ID with software cryptographic primitives and protocols before programming the internal memory.
- To activate secure boot processes

Table 14. Unique ID registers (96 bits)

Address	Content description	Unique ID bits							
		7	6	5	4	3	2	1	0
0x4926	X co-ordinate on the wafer	U_ID[7:0]							
0x4927		U_ID[15:8]							
0x4928	Y co-ordinate on the wafer	U_ID[23:16]							
0x4929		U_ID[31:24]							
0x492A	Wafer number	U_ID[39:32]							
0x492B	Lot number	U_ID[47:40]							
0x492C		U_ID[55:48]							
0x492D		U_ID[63:56]							
0x492E		U_ID[71:64]							
0x492F		U_ID[79:72]							
0x4930		U_ID[87:80]							
0x4931		U_ID[95:88]							

In the following table, data are based on characterization results, unless otherwise specified.

Table 25. Total current consumption and timing in Active-halt mode at V_{DD} = 1.65 V to 3.6 V

Symbol	Parameter	Conditions(1)			Typ.	Max.(2)	Unit
$I_{DD(AH)}$	Supply current in Active-halt mode	LSI RC (at 38 kHz)	LCD OFF(3)	T_A = -40 °C to 25 °C	0.90	2.10	µA
				T_A = 85 °C	1.50	3.40	
				T_A = 125 °C	5.10	12.00	
			LCD ON (static duty/ external V_{LCD}) (4)	T_A = -40 °C to 25 °C	1.40	3.10	
				T_A = 85 °C	1.90	4.30	
				T_A = 125 °C	5.50	13.00	
			LCD ON (1/4 duty/ external V_{LCD}) (5)	T_A = -40 °C to 25 °C	1.90	4.30	
				T_A = 85 °C	2.40	5.40	
				T_A = 125 °C	6.00	15.00	
			LCD ON (1/4 duty/ internal V_{LCD}) (6)	T_A = -40 °C to 25 °C	3.90	8.75	
				T_A = 85 °C	4.50	10.20	
				T_A = 125 °C	6.80	16.30	
$I_{DD(AH)}$	Supply current in Active-halt mode	LSE external clock (32.768 kHz) (7)	LCD OFF(8)	T_A = -40 °C to 25 °C	0.50	1.20	µA
				T_A = 85 °C	0.90	2.10	
				T_A = 125 °C	4.80	11.00	
			LCD ON (static duty/ external V_{LCD}) (4)	T_A = -40 °C to 25 °C	0.85	1.90	
				T_A = 85 °C	1.30	3.20	
				T_A = 125 °C	5.00	12.00	
			LCD ON (1/4 duty/ external V_{LCD}) (5)	T_A = -40 °C to 25 °C	1.50	2.50	
				T_A = 85 °C	1.80	4.20	
				T_A = 125 °C	5.70	14.00	
			LCD ON (1/4 duty/ internal V_{LCD}) (6)	T_A = -40 °C to 25 °C	3.40	7.60	
				T_A = 85 °C	3.90	9.20	
				T_A = 125 °C	6.30	15.20	
$I_{DD(WUFAH)}$	Supply current during wakeup time from Active-halt mode (using HSI)	-	-	-	2.40	-	mA

In the following table, data are based on characterization results, unless otherwise specified.

Table 27. Total current consumption and timing in Halt mode at V_{DD} = 1.65 to 3.6 V

Symbol	Parameter	Condition(1)	Typ.	Max.	Unit
$I_{DD(Halt)}$	Supply current in Halt mode (ultra-low-power ULP bit =1 in the PWR_CSR2 register)	T_A = -40 °C to 25 °C	0.4	0.9(2)	µA
		T_A = 85 °C	0.9	2.8(3)	
		T_A = 125 °C	4.4	13(3)	
$I_{DD(WUHalt)}$	Supply current during wakeup time from Halt mode (using HSI)	-	2.4	-	mA
$t_{WU\_HSI(Halt)}$ (4)(5)	Wakeup time from Halt to Run mode (using HSI)	-	4.7	7(2)	µs
$t_{WU\_LSI(Halt)}$ (4)(5)	Wakeup time from Halt mode to Run mode (using LSI)	-	150	-	

1. T_A = -40 to 125 °C, no floating I/O, unless otherwise specified.
2. Guaranteed by characterization results.
3. Tested at 85 °C for temperature range A or 125°C for temperature range C.
4. ULP=0 or ULP=1 and FWU=1 in the PWR_CSR2 register.
5. Wakeup time until start of interrupt vector fetch. The first word of interrupt routine is fetched 4 CPU cycles after t_{WU}.

Figure 20. Typical $I_{DD(Halt)}$ vs. V_{DD} (internal reference voltage OFF)

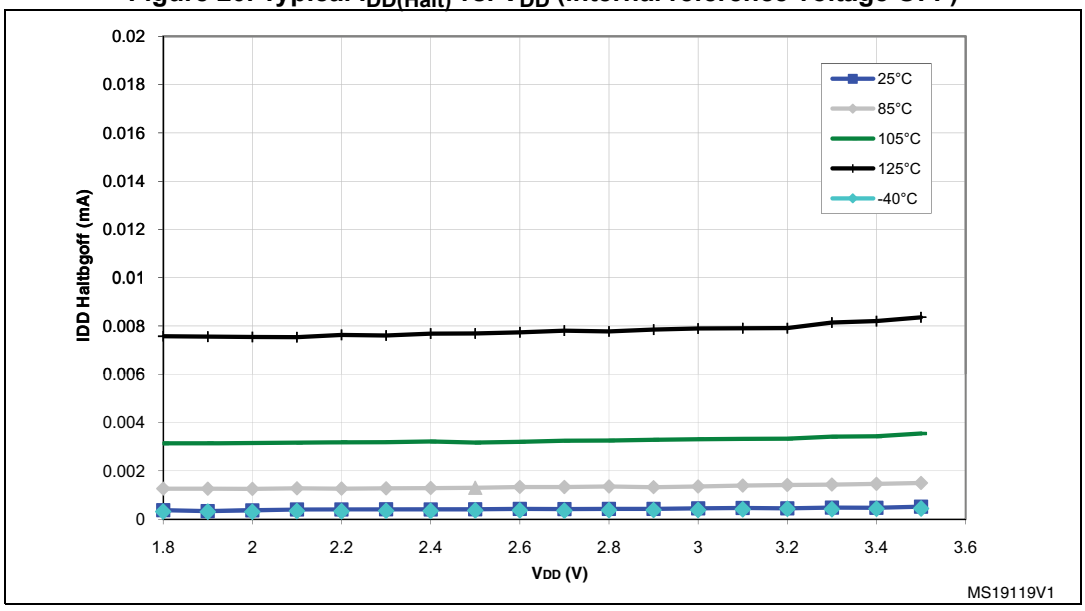


Table 34. HSI oscillator characteristics

Symbol	Parameter	Conditions(1)	Min.	Typ.	Max.	Unit
f_{HSI}	Frequency	V_{DD} = 3.0 V	-	16	-	MHz
ACC_{HSI}	HSI oscillator user trimming accuracy	Trimmed by the application for any V_{DD} and T_A conditions	-1	-	1	%
	HSI oscillator accuracy (factory calibrated)	V_{DD} ≤1.8 V≤ V_{DD} ≤ 3.6 V -40 °C ≤T_A ≤ 125 °C	-5	-	5	
TRIM	HSI user trimming step(2)	Trimming code ≠ multiple of 16	-	0.4	0.7(2)	%
		Trimming code = multiple of 16	-	-	± 1.5(2)	
$t_{su(HSI)}$	HSI oscillator setup time (wakeup time)	-	-	3.7	6 (3)	µs
$I_{DD(HSI)}$	HSI oscillator power consumption	-	-	100	140(3)	µA

1. V_{DD} = 3.0 V, T_A = -40 to 125 °C unless otherwise specified.
2. The trimming step differs depending on the trimming code. It is usually negative on the codes which are multiples of 16 (0x00, 0x10, 0x20, 0x30...0xE0). Refer to the AN3101 “STM8L15x internal RC oscillator calibration” application note for more details.
3. Guaranteed by design.

Figure 23. Typical HSI frequency vs. V_{DD}

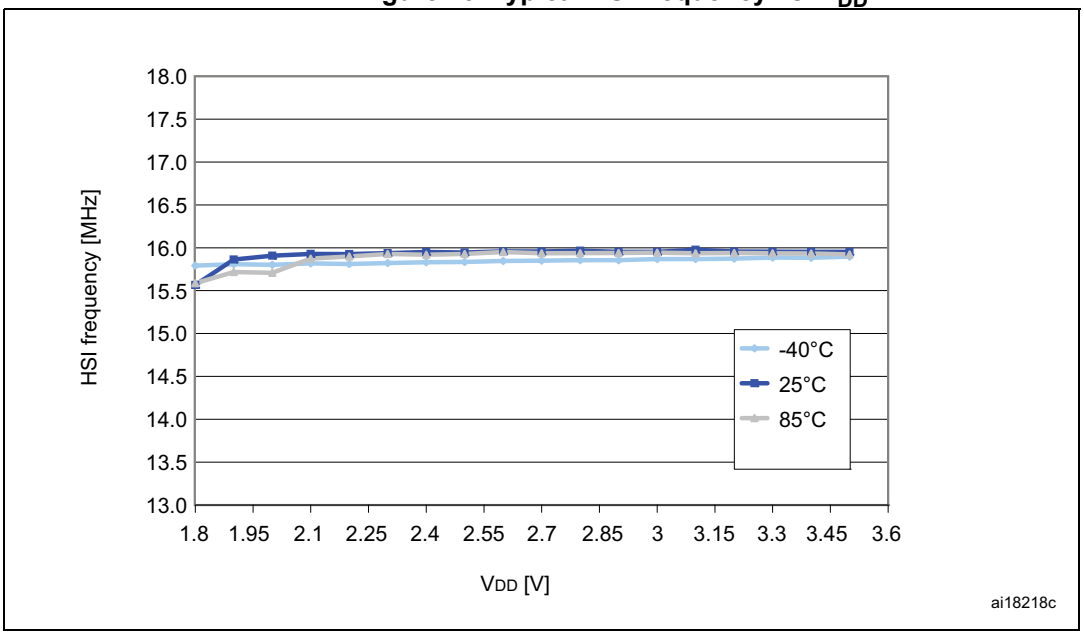


Figure 25. Typical V_{IL} and V_{IH} vs. V_{DD} (standard I/Os)

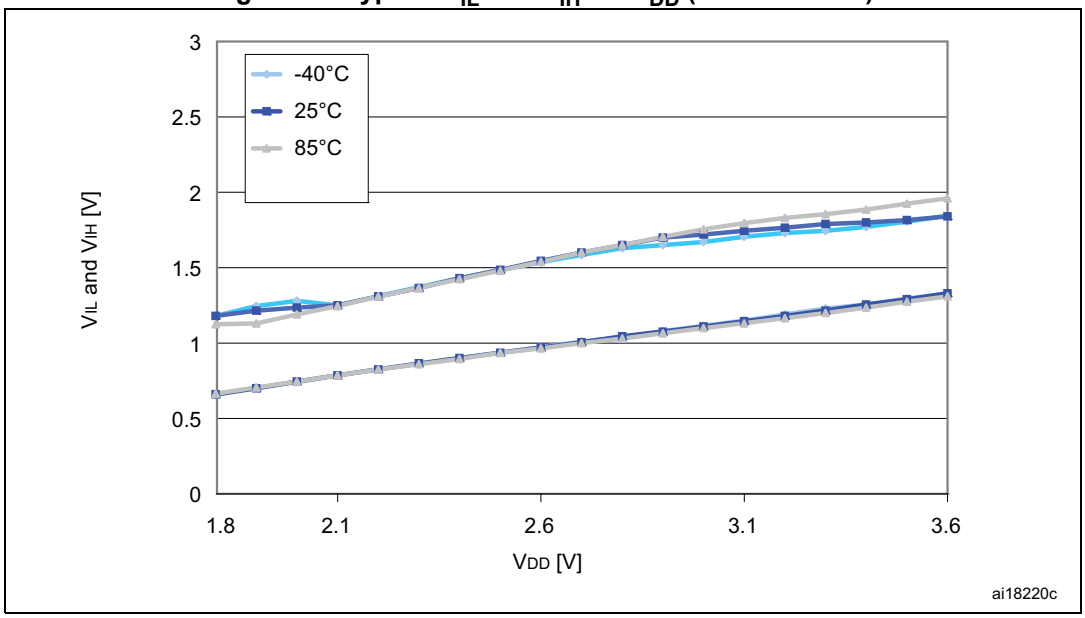
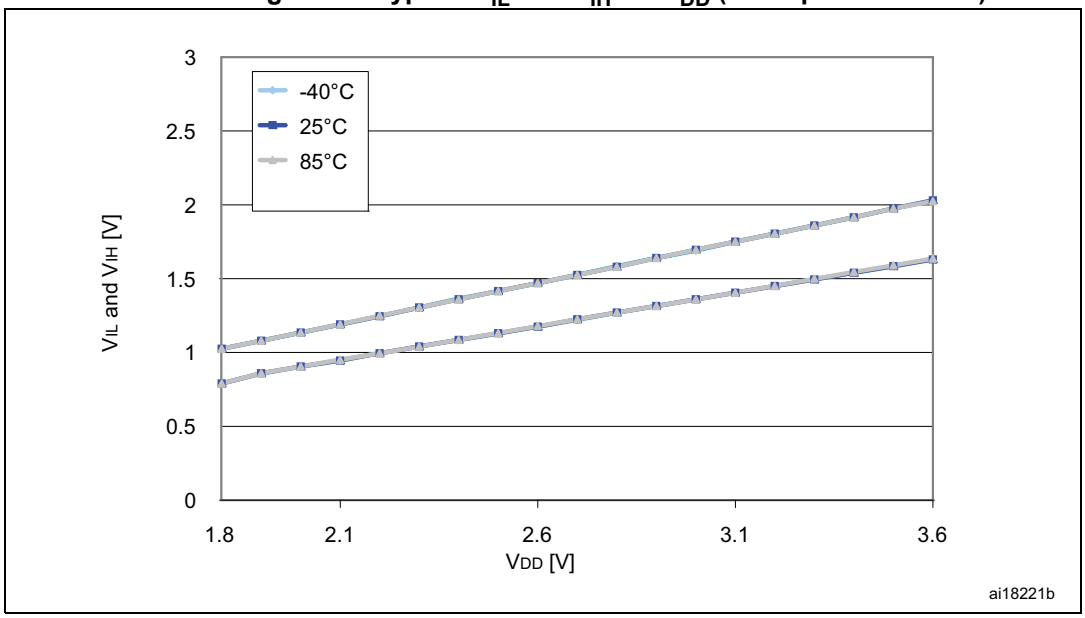


Figure 26. Typical V_{IL} and V_{IH} vs. V_{DD} (true open drain I/Os)



In the following table, data are based on characterization results, not tested in production.

Table 54. DAC accuracy

Symbol	Parameter	Conditions	Typ.	Max.(1)	Unit
DNL	Differential non linearity(2)	R_L ≥5 kΩ, C_L≤50 pF DACOUT buffer ON(3)	1.5	3	12-bit LSB
		No load DACOUT buffer OFF	1.5	3	
INL	Integral non linearity(4)	R_L ≥5 kΩ, C_L≤ 50 pF DACOUT buffer ON(3)	2	4	
		No load DACOUT buffer OFF	2	4	
Offset	Offset error(5)	R_L ≥5 kΩ, C_L≤ 50 pF DACOUT buffer ON(3)	±10	±25	
		No load DACOUT buffer OFF	±5	±8	
Offset1	Offset error at Code 1 (6)	DACOUT buffer OFF	±1.5	±5	
Gain error	Gain error(7)	R_L ≥5 kΩ, C_L≤ 50 pF DACOUT buffer ON(3)	+0.1/-0.2	+0.2/-0.5	%
		No load DACOUT buffer OFF	+0/-0.2	+0/-0.4	
TUE	Total unadjusted error	R_L ≥5 kΩ, C_L≤ 50 pF DACOUT buffer ON(3)	12	30	12-bit LSB
		No load -DACOUT buffer OFF	8	12	

1. Not tested in production.
2. Difference between two consecutive codes - 1 LSB.
3. In 48-pin package devices the DAC2 output buffer must be kept off and no load must be applied on the DAC_OUT2 output.
4. Difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023.
5. Difference between the value measured at Code (0x800) and the ideal value = V_{REF+}/2.
6. Difference between the value measured at Code (0x001) and the ideal value.
7. Difference between the ideal slope of the transfer function and the measured slope computed from Code 0x000 and 0xFFF when buffer is ON, and from Code giving 0.2 V and (V_{DDA} -0.2) V when buffer is OFF.

Table 56. ADC1 characteristics (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_S	Sampling time	V_{AIN} PF0/1/2/3 fast channels V_{DDA} < 2.4 V	0.43(3)(4)	-	-	µs
		V_{AIN} PF0/1/2/3 fast channels 2.4 V ≤V_{DDA}≤ 3.6 V	0.22(3)(4)	-	-	
		V_{AIN} on slow channels V_{DDA} < 2.4 V	0.86(3)(4)	-	-	
		V_{AIN} on slow channels 2.4 V ≤V_{DDA}≤ 3.6 V	0.41(3)(4)	-	-	
t_{conv}	12-bit conversion time	-	12000000 / f_{ADC} + t_S			
		16 MHz	1(3)	-	-	
t_{WKUP}	Wakeup time from OFF state	-	-	-	3	
t_{IDLE}(5)	Time before a new conversion	-	-	-	∞	s
$t_{VREFINT}$	Internal reference voltage startup time	-	-	-	refer to *Table 49*	ms

1. The current consumption through V_{REF} is composed of two parameters:
   - one constant (max 300 µA)
   - one variable (max 400 µA), only during sampling time + 2 first conversion pulses.
   So, peak consumption is 300+400 = 700 µA and average consumption is 300 + [(4 sampling + 2) /16] x 400 = 450 µA at 1Msps
2. V_{REF-} must be tied to ground.
3. Minimum sampling and conversion time is reached for maximum R_{AIN}= 0.5 kΩ.
4. Value obtained for continuous conversion on fast channel.
5. In the RM0031, t_{IDLE} defines the time between 2 conversions, or between ADC ON and the first conversion. t_{IDLE} is not relevant for this device.

Table 59. ADC1 accuracy with $V_{DDA} = V_{REF}^{+} = 1.8$ V to 2.4 V (continued)

Symbol	Parameter	Typ.	Max.(1)	Unit
Offset	Offset error	2	3	LSB
Gain	Gain error	2	3	LSB

1. Guaranteed by characterization results.

Figure 42. ADC1 accuracy characteristics

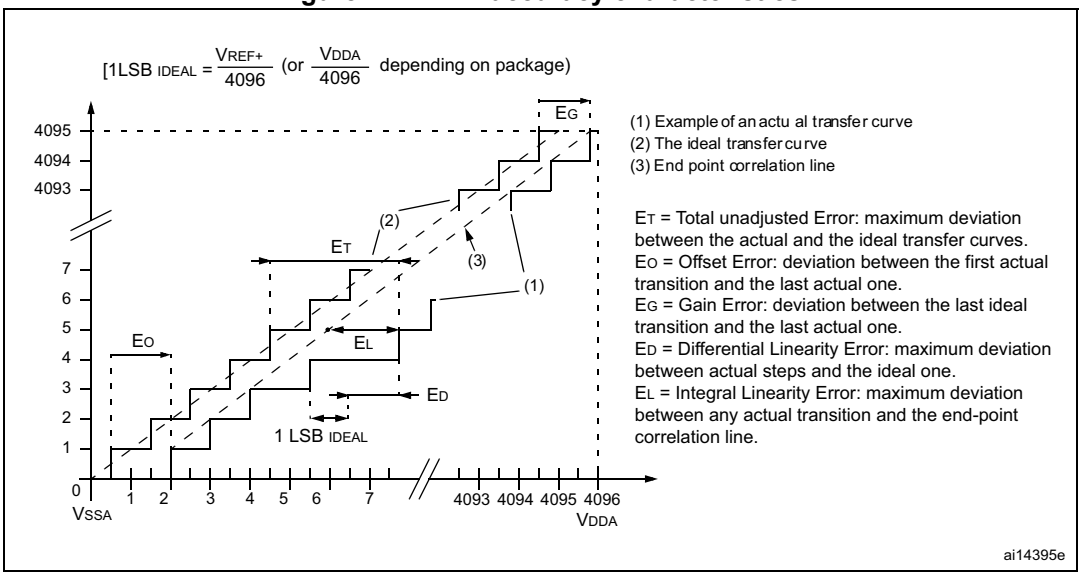
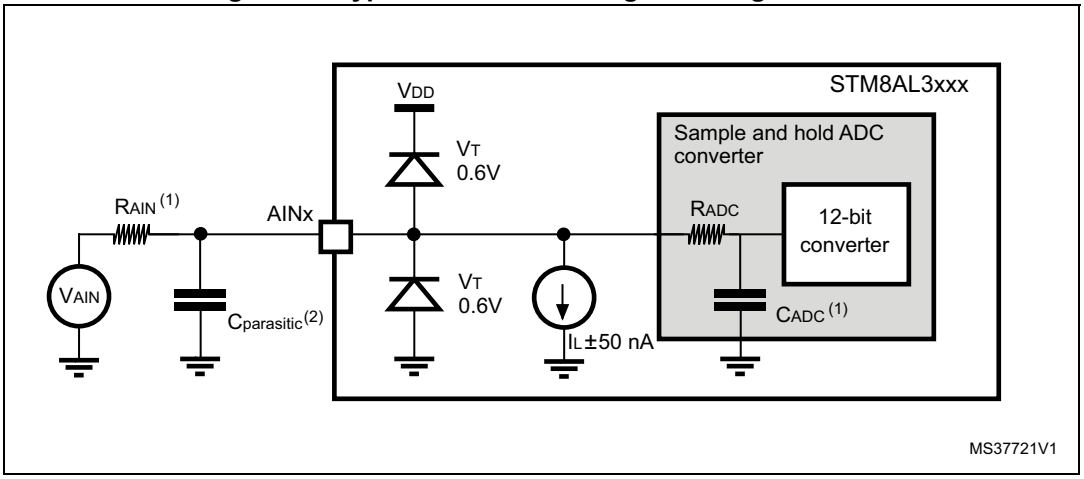


Figure 43. Typical connection diagram using the ADC



1. Refer to *Table 56* for the values of R_{AIN} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 44* or *Figure 45*, depending on whether V_{REF+} is connected to V_{DDA} or not. Good quality ceramic 10 nF capacitors should be used. They should be placed as close as possible to the chip.

Electromagnetic interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm IEC61967-2 which specifies the board and the loading of each pin.

Table 61. EMI data (1)

Symbol	Parameter	Conditions	Monitored frequency band	Max vs.	Unit
				16 MHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = +25 °C, LQFP80 conforming to IEC61967-2	0.1 MHz to 30 MHz	10	dBµV
			30 MHz to 130 MHz	4	
			130 MHz to 1 GHz	1	
			EMI Level	1.5	-

1. Guaranteed by characterization results.

Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic discharge (ESD)

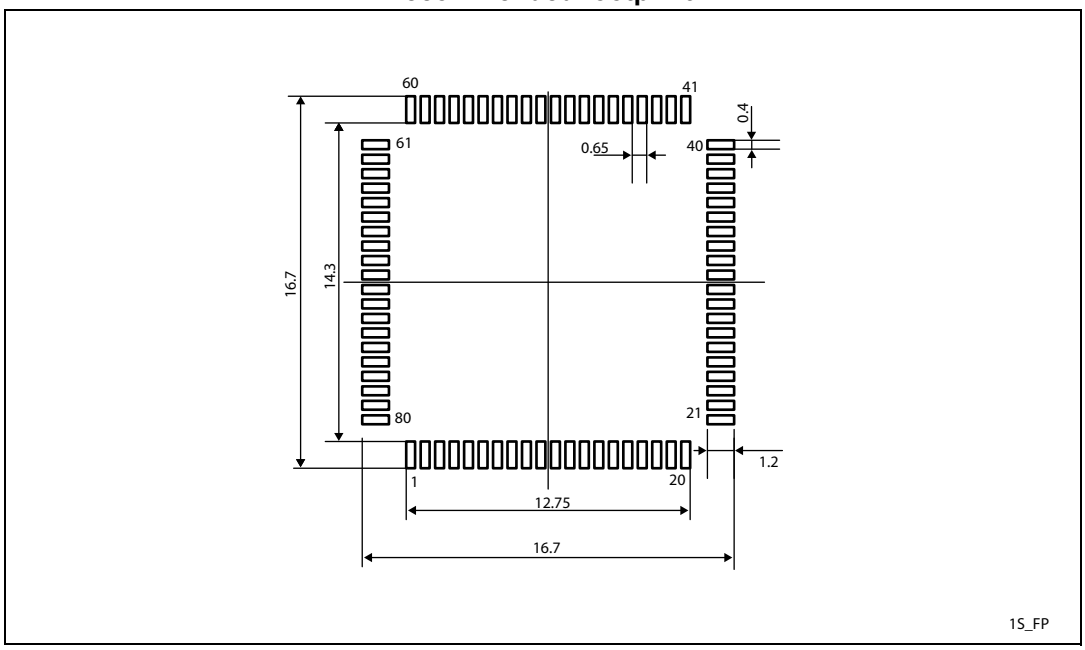
Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). Two models are simulated: human body model and charge device model. This test conforms to the ANSI/ESDA/JEDEC JS-001, JESD22-A115 and ANSI/ESD S5.3.1.

Table 62. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value (1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = 25 °C, conforming to ANSI/ESDA/ JEDEC JS-001	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = 25 °C, conforming to ANSI/ESD S5.3.1	C4B	500	
$V_{ESD(MM)}$	Electrostatic discharge voltage (machine model)	T_A = 25 °C, conforming to JESD22-A115	M2	200	

1. Guaranteed by characterization results.

Figure 47. LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package recommended footprint



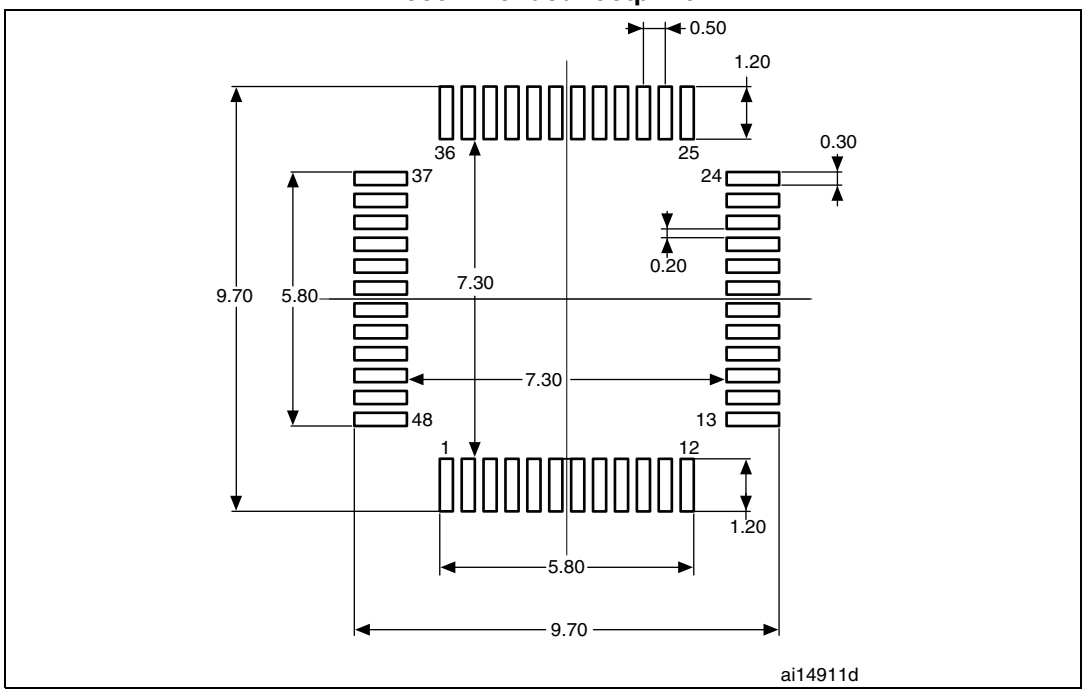
1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 53. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

11 Ordering information

Table 68. STM8AL31E8x STM8AL3LE8x ordering information scheme

Example: STM8 AL 31 E 8 8 T C Y

Device family

STM8 microcontroller

Product type

AL = automotive low-power(1)

Device subfamily

31: standard devices

3L: devices with LCD

AES encryption hardware accelerator

E = AES encryption hardware accelerator

Program memory size

8 = 64 Kbytes of Flash memory

Pin count

A = 80 pins

9 = 64 pins

8 = 48 pins

Package

T = LQFP

Temperature range

C = -40 to 125 °C

A = -40 to 85 °C

Packing

Y = tray

X = Tape and reel compliant with EIA 481-C

1. Qualified and characterized according to AECQ100 and Q003 or equivalent, advanced screening according to AEC Q001 and Q002 or equivalent.

For a list of available options (e.g. memory size, package) and orderable part numbers or for further information on any aspect of this device, please go to *www.st.com* or contact the nearest ST sales office.

12 Revision history

Table 69. Document revision history

Date	Revision	Changes
22-Apr-2015	1	Initial release.
27-Jul-2015	2	Updated the document confidentiality level to “Public”. No other changes in the content.
19-Aug-2015	3	Changed datasheet status to “production data”. Added LQFP64 and LQFP80 packages together with the corresponding part numbers.
18-Oct-2016	4	– Updated *Table 5: High-density STM8AL3xE8x pin description*: pin name changed from PC3/USART1_TX/LCD_SEG23(3)/ADC1_IN5/COMP_IN3M/COMP2_INM/COMP1_INP to PC3/USART1_TX/LCD_SEG23(3)/ADC1_IN5/COMP2_INM/COMP1_INP. – Added footnote to *Table 68: STM8AL31E8x STM8AL3LE8x ordering information scheme*. – Updated *Section : Device marking on page 122*, *Section : Device marking on page 126*, *Section : Device marking on page 130* – Updated *Section 9.2: Absolute maximum ratings* – Updated *Figure 12: Power supply thresholds*.
5-Dec-2016	5	– Updated *Table 5: High-density STM8AL3xE8x pin description*: two pin names changed from PI0/RTC_TAMP1/[SPI2_NSS]/[TIM3_CH3 to PI0/RTC_TAMP1/[SPI2_NSS]/[TIM3_CH1 and from PF2/ADC1_IN26/[SPI2_SCK]/[USART3_SCK] to PF2/ADC1_IN26/[SPI1_SCK]/[USART3_SCK]