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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

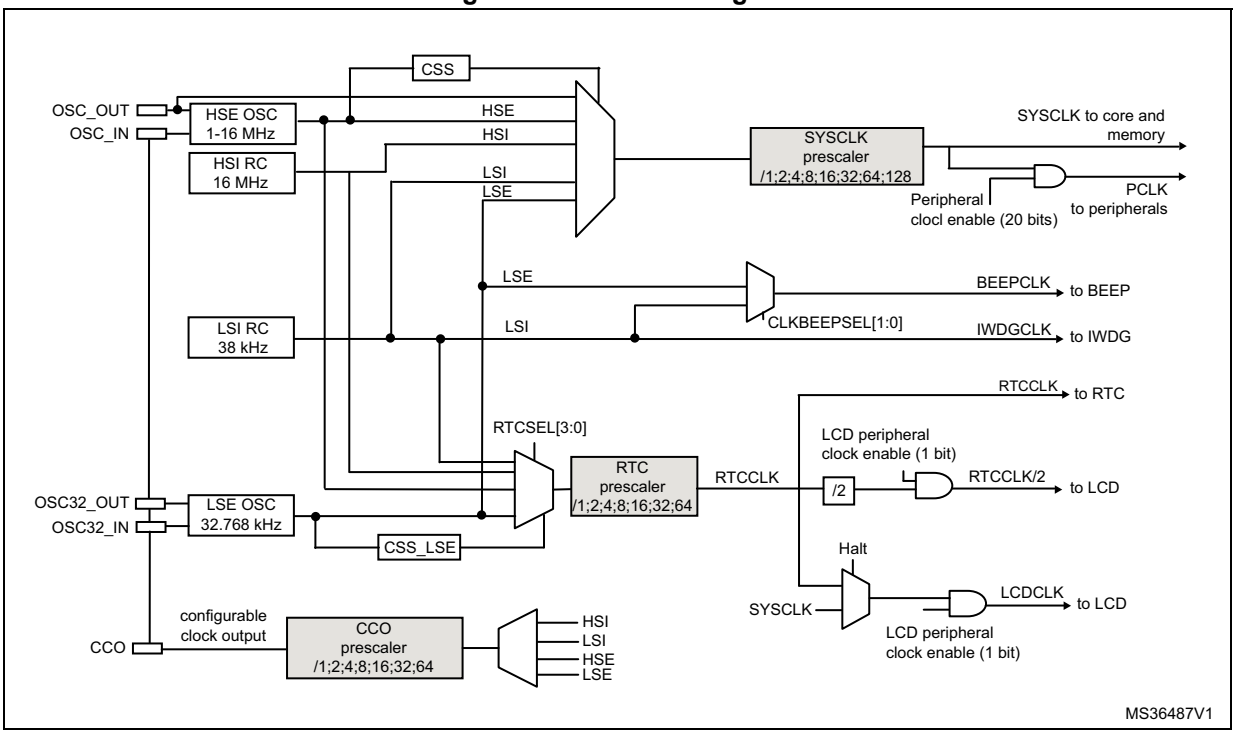
Details	
Product Status	Not For New Designs
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	41
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 25x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8al3le88tay

Table 1. Device summary

Reference	Part number
STM8AL31E8x	STM8AL31E88, STM8AL31E89, STM8AL31E8A
STM8AL3LE8x	STM8AL3LE88, STM8AL3LE89, STM8AL3LE8A

Contents

Figure 2. Clock tree diagram



1. The HSE clock source is either an external crystal/ceramic resonator or an external source (HSE bypass). Refer to Section HSE clock in STM8L051/L052 Value Line, STM8L151/L152, STM8L162, STM8AL31, STM8AL3L MCU lines reference manual (RM0031).
2. The LSE clock source is either an external crystal/ceramic resonator or a external source (LSE bypass). Refer to Section LSE clock in STM8L051/L052 Value Line, STM8L151/L152, STM8L162, STM8AL31, STM8AL3L MCU lines reference manual (RM0031).

3.5 Low-power real-time clock

The real-time clock (RTC) is an independent binary coded decimal (BCD) timer/counter.

Six byte locations contain the second, minute, hour (12/24 hour), week day, date, month, year, in BCD (binary coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day months are made automatically. The subsecond field is also readable in binary format.

The calendar is adjustable from 1 to 32767 RTC clock pulses. This allows to make a synchronization to a master clock.

The RTC offers a digital calibration which allows an accuracy of +/-0.5ppm.

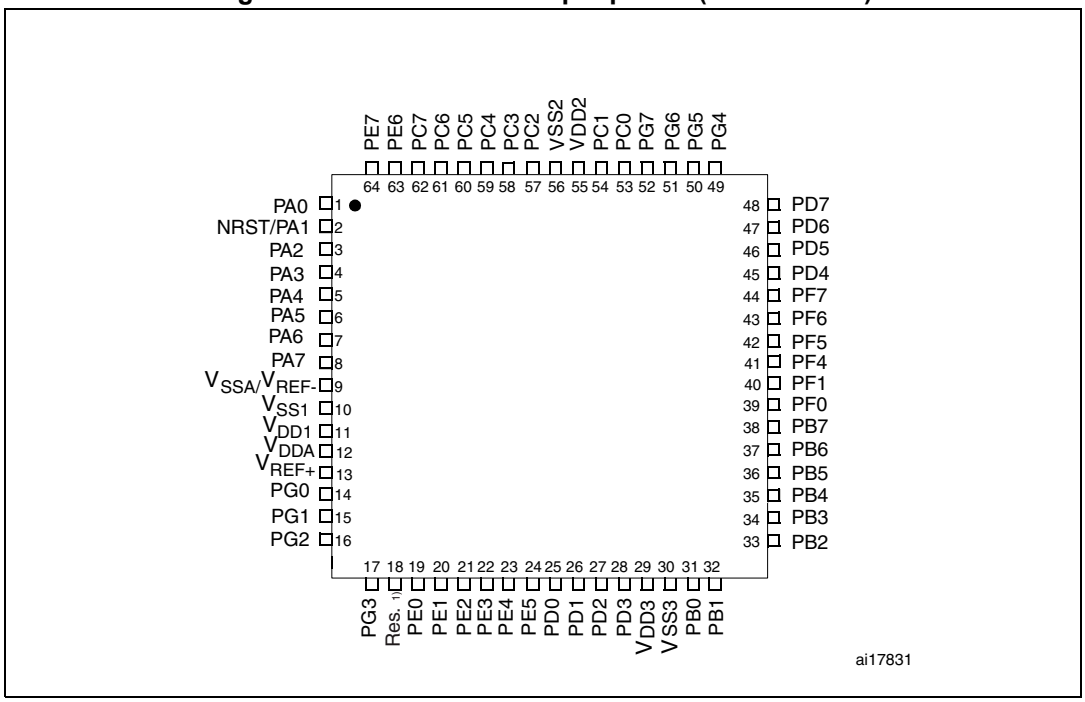
It provides a programmable alarm and programmable periodic interrupts with wakeup from Halt capability.

- Periodic wakeup time using the 32.768 kHz LSE with the lowest resolution (of 61 µs) is from min. 122 µs to max. 3.9 s. With a different resolution, the wakeup time reaches 36 hours
- Periodic alarms based on the calendar are generated from LSE period to every year

A clock security system detects a failure on LSE, and provides an interrupt with wakeup capability. The RTC clock automatically switches to LSI in case of LSE failure.

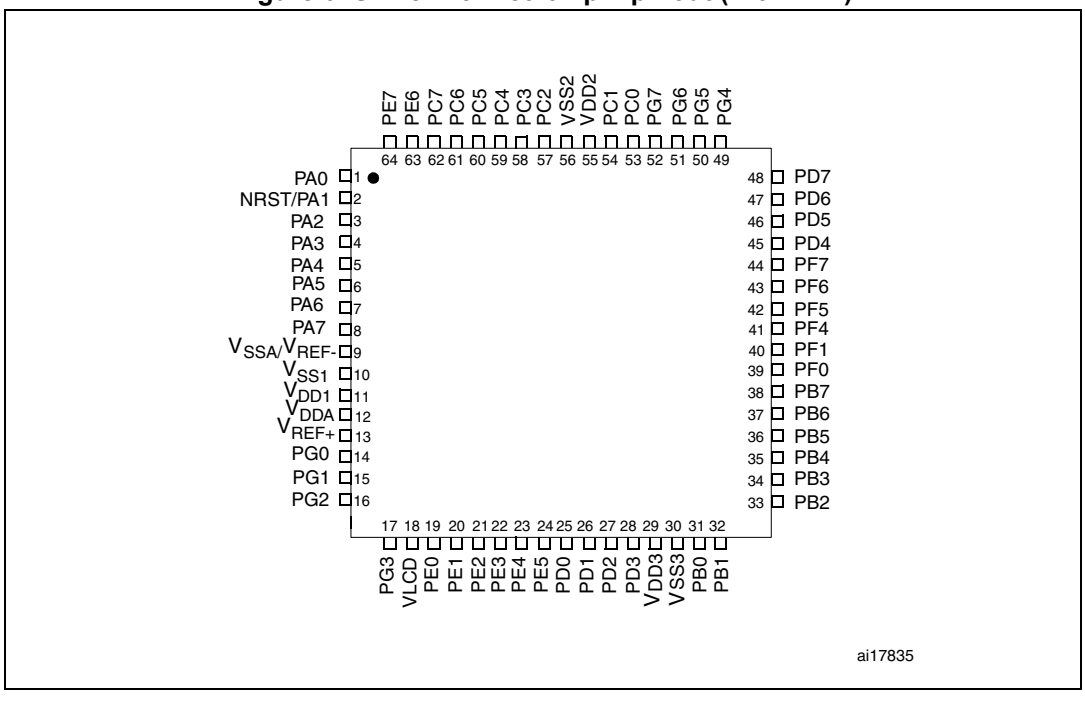
The RTC also provides 3 anti-tamper detection pins. This detection embeds a programmable filter and wakes-up the MCU.

Figure 5. STM8AL31E89 64-pin pinout (without LCD)



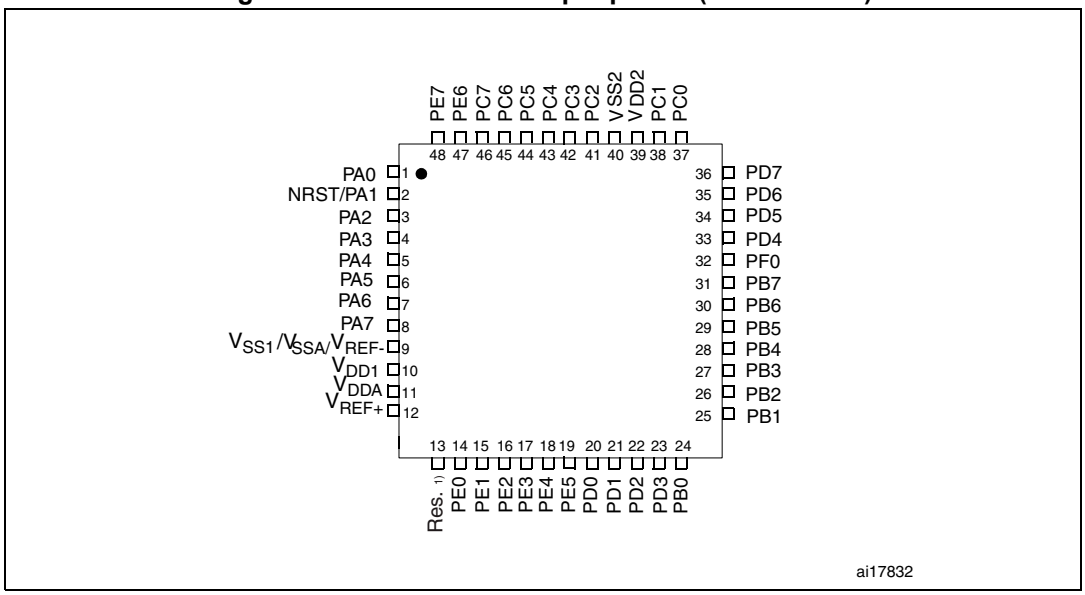
1. Pin 18 is reserved and must be tied to V_{DD}.
2. The above figure shows the package top view.

Figure 6. STM8AL3LE89 64-pin pinout (with LCD)



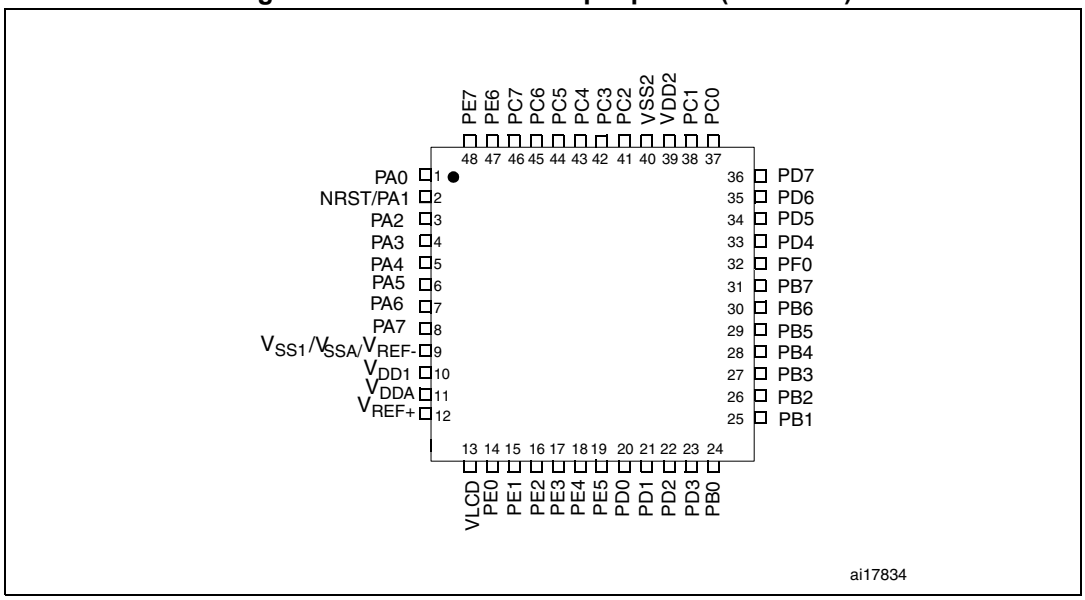
1. The above figure shows the package top view.

Figure 7. STM8AL31E88 48-pin pinout (without LCD)



1. Pin 13 is reserved and must be tied to V_{DD}.
2. The above figure shows the package top view.

Figure 8. STM8AL3LE88 48-pin pinout (with LCD)



1. The above figure shows the package top view.

Table 4. Legend/abbreviation

Type	I= input, O = output, S = power supply	
Level	FT: Five-volt tolerant	
	Output	HS = high sink/source (20 mA)
Port and control configuration	Input	float = floating, wpu = weak pull-up
	Output	T = true open drain, OD = open drain, PP = push pull
Reset state	Bold X (pin state after reset release). Unless otherwise specified, the pin state is the same during the reset phase (i.e. “under reset”) and after internal reset release (i.e. at reset state).	

Table 5. High-density STM8AL3xE8x pin description

Pin number			Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP80	LQFP64	LQFP48				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
1	-	-	PH0/LCD SEG 36 (3)	I/O	FT(5)	**X**	X	X	HS	X	X	**Port H0**	LCD segment 36
2	-	-	PH1/LCD SEG 37 (3)	I/O	FT(5)	**X**	X	X	HS	X	X	**Port H1**	LCD segment 37
3	-	-	PH2/LCD SEG 38 (3)	I/O	FT(5)	**X**	X	X	HS	X	X	**Port H2**	LCD segment 38
4	-	-	PH3/LCD SEG 39 (3)	I/O	FT(5)	**X**	X	X	HS	X	X	**Port H3**	LCD segment 39
6	2	2	NRST/PA1(1)	I/O	-	-	**X**	-	HS	X	X	**Reset**	PA1
7	3	3	PA2/OSC_IN/ *[USART1_TX](2)/ [SPI1_MISO]* (2)	I/O	-	**X**	X	X	HS	X	X	**Port A2**	HSE oscillator input / *[USART1 transmit] / [SPI1 master in- slave out] /*
8	4	4	PA3/OSC_OUT/*[USART1 _RX](2)/[SPI1_MOSI](2)*	I/O	-	**X**	X	X	HS	X	X	**Port A3**	HSE oscillator output / *[USART1 receive]/ [SPI1 master out/slave in]/*
9	5	5	PA4/TIM2_BKIN/ *[TIM2_ETR](2)* LCD_COM0(3)/ADC1_IN2 COMP1_INP	I/O	FT(5)	**X**	X	X	HS	X	X	**Port A4**	Timer 2 - break input / */[Timer 2 - trigger] /* LCD COM 0 / ADC1 input 2/Comparator 1 positive input
10	6	6	PA5/TIM3_BKIN/ *[TIM3_ETR](2)/* LCD_COM1(3)/ADC1_IN1/ COMP1_INP	I/O	FT(5)	**X**	X	X	HS	X	X	**Port A5**	Timer 3 - break input / *[Timer 3 - trigger] /* LCD_COM 1 / ADC1 input 1/Comparator 1 positive input
11	7	7	PA6/ADC1_TRIG/ LCD_COM2(3)/ADC1_IN0/ COMP1_INP	I/O	FT(5)	**X**	X	X	HS	X	X	**Port A6**	ADC1 - trigger / LCD_COM2 / ADC1 input 0/Comparator 1 positive input

Table 5. High-density STM8AL3xE8x pin description (continued)

Pin number			Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP80	LQFP64	LQFP48				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
64	52	-	PG7/LCD_SEG35/ SPI2_MISO	I/O	FT(5)	**X**	X	X	HS	X	X	**Port G7**	LCD segment 35 / SPI2 master in- slave out
23	-	-	PE0/LCD_SEG1(3)/ TIM5_CH2	I/O	FT(5)	**X**	X	X	HS	X	X	**Port E0**	LCD segment 1 /Timer 5 channel 2
-	19	14	PE0/LCD_SEG1(3)/ TIM5_CH2/RTC_TAMP1	I/O	FT(5)	**X**	X	X	HS	X	X	**Port E0**	LCD segment 1 /Timer 5 channel 2 / RTC tamper 1
24	-	-	PE1/TIM1_CH2N /LCD_SEG2(3)	I/O	FT(5)	**X**	X	X	HS	X	X	**Port E1**	Timer 1 - inverted channel 2 / LCD segment 2
-	20	15	PE1/TIM1_CH2N /LCD_SEG2(3)/ RTC_TAMP2	I/O	FT(5)	**X**	X	X	HS	X	X	**Port E1**	Timer 1 - inverted channel 2 / LCD segment 2 / RTC tamper 2
25	-	-	PE2/TIM1_CH3N /LCD_SEG3(3)	I/O	FT(5)	**X**	X	X	HS	X	X	**Port E2**	Timer 1 - inverted channel 3 / LCD segment 3
-	21	16	PE2/TIM1_CH3N /LCD_SEG3(3)/ RTC_TAMP3	I/O	FT(5)	**X**	X	X	HS	X	X	**Port E2**	Timer 1 - inverted channel 3 / LCD segment 3 / RTC tamper 3
26	-	-	PE3/LCD_SEG4(3)	I/O	FT(5)	**X**	X	X	HS	X	X	**Port E3**	LCD segment 4
-	22	17	PE3/LCD_SEG4(3)/ USART2_RX	I/O	FT(5)	**X**	X	X	HS	X	X	**Port E3**	LCD segment 4/ USART2 receive
27	-	-	PE4/LCD_SEG5(3)/ DAC_TRIG1	I/O	FT(5)	**X**	X	X	HS	X	X	**Port E4**	LCD segment 5/ DAC 1 trigger
-	23	18	PE4/LCD_SEG5(3)/ DAC_TRIG2/USART2_TX	I/O	FT(5)	**X**	X	X	HS	X	X	**Port E4**	LCD segment 5/ DAC 2 trigger/ USART2 transmit
28	-	-	PE5/LCD_SEG6(3)/ ADC1_IN23/COMP1_INP/ COMP2_INP	I/O	FT(5)	**X**	X	X	HS	X	X	**Port E5**	LCD segment 6 / ADC1_IN23/Comparator 1 positive input/Comparator 2 positive input
-	24	19	PE5/LCD_SEG6(3)/ ADC1_IN23/COMP1_INP/ COMP2_INP/ USART2_CK	I/O	FT(5)	**X**	X	X	HS	X	X	**Port E5**	LCD segment 6 / ADC1_IN23/ Comparator 1 positive input/ Comparator 2 positive input/USART2 synchronous clock
-	-	47	PE6/LCD_SEG26(3)/ PVD_IN/TIM5_BKIN/ USART3_TX	I/O	FT(5)	**X**	X	X	HS	X	X	**Port E6**	LCD segment 26 /PVD_IN /TIM5 break input / USART3 transmit

Table 5. High-density STM8AL3xE8x pin description (continued)

Pin number			Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP80	LQFP64	LQFP48				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
53	41	-	PF4/LCD_COM4	I/O	FT(5)	**X**	X	X	HS	X	X	**Port F4**	LCD COM4
54	42	-	PF5/LCD_COM5	I/O	FT(5)	**X**	X	X	HS	X	X	**Port F5**	LCD COM5
55	43	-	PF6/LCD_COM6	I/O	FT(5)	**X**	X	X	HS	X	X	**Port F6**	LCD COM6
56	44	-	PF7/LCD_COM7	I/O	FT(5)	**X**	X	X	HS	X	X	**Port F7**	LCD COM7
22	18	13	VLCD(7)	S	-	**-**	-	-	-	-	-	LCD booster external capacitor	
15	11	10	V_{DD1}	S	-	**-**	-	-	-	-	-	Digital power supply	
14	10	-	V_{SS1}	-	-	**-**	-	-	-	-	-	I/O ground	
16	12	11	V_{DDA}	S	-	**-**	-	-	-	-	-	Analog supply voltage	
17	13	12	V_{REF+}/V_{REF+_DAC}	S	-	**-**	-	-	-	-	-	ADC1 and DAC1/2 positive voltage reference	
18	14	-	PG0/LCD SEG 28(3)/USART3_RX/ *[TIM2_BKIN]*	I/O	FT(5)	**X**	X	X	HS	X	X	**Port G0**	LCD segment 28/ USART3 receive / *[Timer 2 - break input]*
19	15	-	PG1/LCD SEG 29(3)/USART3_TX/ *[TIM3_BKIN]*	I/O	FT(5)	**X**	X	X	HS	X	X	**Port G1**	LCD segment 29/ USART3 transmit / *[Timer 3 -break input]*
20	16	-	PG2/LCD_SEG 30(3)/ USART3_CK	I/O	FT(5)	**X**	X	X	HS	X	X	**Port G2**	LCD segment 30/ USART 3 synchronous clock
21	17	-	PG3/LCD SEG 31 (3)/ *[TIM3_ETR]*	I/O	FT(5)	**X**	X	X	HS	X	X	**Port G3**	LCD segment 31/ *[Timer 3 - trigger]*
33	-	-	PH4/USART2_RX	I/O	FT(5)	**X**	X	X	HS	X	X	**Port H4**	USART2 receive
34	-	-	PH5/USART2_TX	I/O	FT(5)	**X**	X	X	HS	X	X	**Port H5**	USART2 transmit
35	-	-	PH6/USART2_CK/ TIM5_CH1	I/O	FT(5)	**X**	X	X	HS	X	X	**Port H6**	USART2 synchronous clock/ Timer 5 - channel 1
36	-	-	PH7/TIM5_CH2	I/O	FT(5)	**X**	X	X	HS	X	X	**Port H7**	Timer 5 - channel 2
-	-	9	$V_{SS}/V_{SSA}/V_{REF-}$	S	-	-	-	-	-	-	-	I/O ground / Analog ground voltage / ADC1 negative voltage reference	
13	9	-	V_{SSA}/V_{REF-}	S	-	-	-	-	-	-	-	Analog ground voltage / ADC1 negative voltage reference	
37	29	-	V_{DD3}	S	-	-	-	-	-	-	-	IOs supply voltage	
38	30	-	V_{SS3}	S	-	-	-	-	-	-	-	IOs ground voltage	

Table 8. I/O port hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 500F	Port D	PD_ODR	Port D data output latch register	0x00
0x00 5010		PD_IDR	Port D input pin value register	0xXX
0x00 5011		PD_DDR	Port D data direction register	0x00
0x00 5012		PD_CR1	Port D control register 1	0x00
0x00 5013		PD_CR2	Port D control register 2	0x00
0x00 5014	Port E	PE_ODR	Port E data output latch register	0x00
0x00 5015		PE_IDR	Port E input pin value register	0xXX
0x00 5016		PE_DDR	Port E data direction register	0x00
0x00 5017		PE_CR1	Port E control register 1	0x00
0x00 5018		PE_CR2	Port E control register 2	0x00
0x00 5019	Port F	PF_ODR	Port F data output latch register	0x00
0x00 501A		PF_IDR	Port F input pin value register	0xXX
0x00 501B		PF_DDR	Port F data direction register	0x00
0x00 501C		PF_CR1	Port F control register 1	0x00
0x00 501D		PF_CR2	Port F control register 2	0x00
0x00 501E	Port G	PG_ODR	Port F data output latch register	0x00
0x00 501F		PG_IDR	Port G input pin value register	0xXX
0x00 5020		PG_DDR	Port G data direction register	0x00
0x00 5021		PG_CR1	Port G control register 1	0x00
0x00 5022		PG_CR2	Port G control register 2	0x00
0x00 5023	Port H	PH_ODR	Port H data output latch register	0x00
0x00 5024		PH_IDR	Port H input pin value register	0xXX
0x00 5025		PH_DDR	Port H data direction register	0x00
0x00 5026		PH_CR1	Port H control register 1	0x00
0x00 5027		PH_CR2	Port H control register 2	0x00
0x00 5028	Port I	PI_ODR	Port I data output latch register	0x00
0x00 5029		PI_IDR	Port I input pin value register	0xXX
0x00 502A		PI_DDR	Port I data direction register	0x00
0x00 502B		PI_CR1	Port I control register 1	0x00
0x00 502C		PI_CR2	Port I control register 2	0x00

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 509D	SYSCFG	SYSCFG_RMPCR3	Remapping register 3	0x00
0x00 509E		SYSCFG_RMPCR1	Remapping register 1	0x00
0x00 509F		SYSCFG_RMPCR2	Remapping register 2	0x00
0x00 50A0	ITC - EXTI	EXTI_CR1	External interrupt control register 1	0x00
0x00 50A1		EXTI_CR2	External interrupt control register 2	0x00
0x00 50A2		EXTI_CR3	External interrupt control register 3	0x00
0x00 50A3		EXTI_SR1	External interrupt status register 1	0x00
0x00 50A4		EXTI_SR2	External interrupt status register 2	0x00
0x00 50A5		EXTI_CONF1	External interrupt port select register 1	0x00
0x00 50A6	WFE	WFE_CR1	WFE control register 1	0x00
0x00 50A7		WFE_CR2	WFE control register 2	0x00
0x00 50A8		WFE_CR3	WFE control register 3	0x00
0x00 50A9		WFE_CR4	WFE control register 4	0x00
0x00 50AA	ITC - EXTI	EXTI_CR4	External interrupt control register 4	0x00
0x00 50AB		EXTI_CONF2	External interrupt port select register 2	0x00
0x00 50A9 to 0x00 50AF	Reserved area (7 byte)			
0x00 50B0	RST	RST_CR	Reset control register	0x00
0x00 50B1		RST_SR	Reset status register	0x01
0x00 50B2	PWR	PWR_CSR1	Power control and status register 1	0x00
0x00 50B3		PWR_CSR2	Power control and status register 2	0x00
0x00 50B4 to 0x00 50BF	Reserved area (12 byte)			
0x00 50C0	CLK	CLK_CKDIVR	Clock master divider register	0x03
0x00 50C1		CLK_CRTCR	Clock RTC register	0x00(1)
0x00 50C2		CLK_ICKCR	Internal clock control register	0x11
0x00 50C3		CLK_PCKENR1	Peripheral clock gating register 1	0x00
0x00 50C4		CLK_PCKENR2	Peripheral clock gating register 2	0x00
0x00 50C5		CLK_CCOR	Configurable clock control register	0x00
0x00 50C6		CLK_ECKCR	External clock control register	0x00
0x00 50C7		CLK_SCSR	System clock status register	0x01
0x00 50C8		CLK_SWR	System clock switch register	0x01
0x00 50C9		CLK_SWCR	Clock switch control register	0xX0

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 521F to 0x00 522F	Reserved area (17 byte)			
0x00 5230	USART1	USART1_SR	USART1 status register	0xC0
0x00 5231		USART1_DR	USART1 data register	0xXX
0x00 5232		USART1_BRR1	USART1 baud rate register 1	0x00
0x00 5233		USART1_BRR2	USART1 baud rate register 2	0x00
0x00 5234		USART1_CR1	USART1 control register 1	0x00
0x00 5235		USART1_CR2	USART1 control register 2	0x00
0x00 5236		USART1_CR3	USART1 control register 3	0x00
0x00 5237		USART1_CR4	USART1 control register 4	0x00
0x00 5238		USART1_CR5	USART1 control register 5	0x00
0x00 5239		USART1_GTR	USART1 guard time register	0x00
0x00 523A		USART1_PSCR	USART1 prescaler register	0x00
0x00 523B to 0x00 524F	Reserved area (21 byte)			
0x00 5250	TIM2	TIM2_CR1	TIM2 control register 1	0x00
0x00 5251		TIM2_CR2	TIM2 control register 2	0x00
0x00 5252		TIM2_SMCR	TIM2 Slave mode control register	0x00
0x00 5253		TIM2_ETR	TIM2 external trigger register	0x00
0x00 5254		TIM2_DER	TIM2 DMA1 request enable register	0x00
0x00 5255		TIM2_IER	TIM2 interrupt enable register	0x00
0x00 5256		TIM2_SR1	TIM2 status register 1	0x00
0x00 5257		TIM2_SR2	TIM2 status register 2	0x00
0x00 5258		TIM2_EGR	TIM2 event generation register	0x00
0x00 5259		TIM2_CCMR1	TIM2 capture/compare mode register 1	0x00
0x00 525A		TIM2_CCMR2	TIM2 capture/compare mode register 2	0x00
0x00 525B		TIM2_CCER1	TIM2 capture/compare enable register 1	0x00
0x00 525C		TIM2_CNTRH	TIM2 counter high	0x00
0x00 525D		TIM2_CNTRL	TIM2 counter low	0x00
0x00 525E		TIM2_PSCR	TIM2 prescaler register	0x00
0x00 525F		TIM2_ARRH	TIM2 auto-reload register high	0xFF
0x00 5260		TIM2_ARRL	TIM2 auto-reload register low	0xFF
0x00 5261		TIM2_CCR1H	TIM2 capture/compare register 1 high	0x00

Table 10. CPU/SWIM/debug module/interrupt controller registers (continued)

Address	Block	Register label	Register name	Reset status
0x00 7F90	DM	DM_BK1RE	DM breakpoint 1 register extended byte	0xFF
0x00 7F91		DM_BK1RH	DM breakpoint 1 register high byte	0xFF
0x00 7F92		DM_BK1RL	DM breakpoint 1 register low byte	0xFF
0x00 7F93		DM_BK2RE	DM breakpoint 2 register extended byte	0xFF
0x00 7F94		DM_BK2RH	DM breakpoint 2 register high byte	0xFF
0x00 7F95		DM_BK2RL	DM breakpoint 2 register low byte	0xFF
0x00 7F96		DM_CR1	DM Debug module control register 1	0x00
0x00 7F97		DM_CR2	DM Debug module control register 2	0x00
0x00 7F98		DM_CSR1	DM Debug module control/status register 1	0x10
0x00 7F99		DM_CSR2	DM Debug module control/status register 2	0x00
0x00 7F9A		DM_ENFCTR	DM enable function register	0xFF
0x00 7F9B to 0x00 7F9F	Reserved area (5 byte)			

1. Accessible by debug module only

Table 23. Total current consumption and timing in low-power run mode at V_{DD} = 1.65 V to 3.6 V

Symbol	Parameter	Conditions(1)			Typ.	Max.	Unit
$I_{DD(LPR)}$	Supply current in low-power run mode	LSI RC osc. (at 38 kHz)	all peripherals OFF	T_A = -40 °C to 25 °C	5.10	6.50(2)	µA
				T_A = 85 °C	6.80	11.00(3)	
				T_A = 125 °C	13.40	20.00(3)	
		LSE (4) external clock (32.768 kHz)		T_A = -40 °C to 25 °C	5.25	5.60(2)	
				T_A = 85 °C	5.85	6.30(2)	
				T_A = 125 °C	14.00	16.50(2)	

1. No floating I/Os
2. Guaranteed by characterization results.
3. Tested at 85°C for temperature range A or 125°C for temperature range C.
4. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ LSE}$) must be added. Refer to *Table 33*

Figure 17. Typical $I_{DD(LPR)}$ vs. V_{DD} (LSI clock source), all peripherals OFF

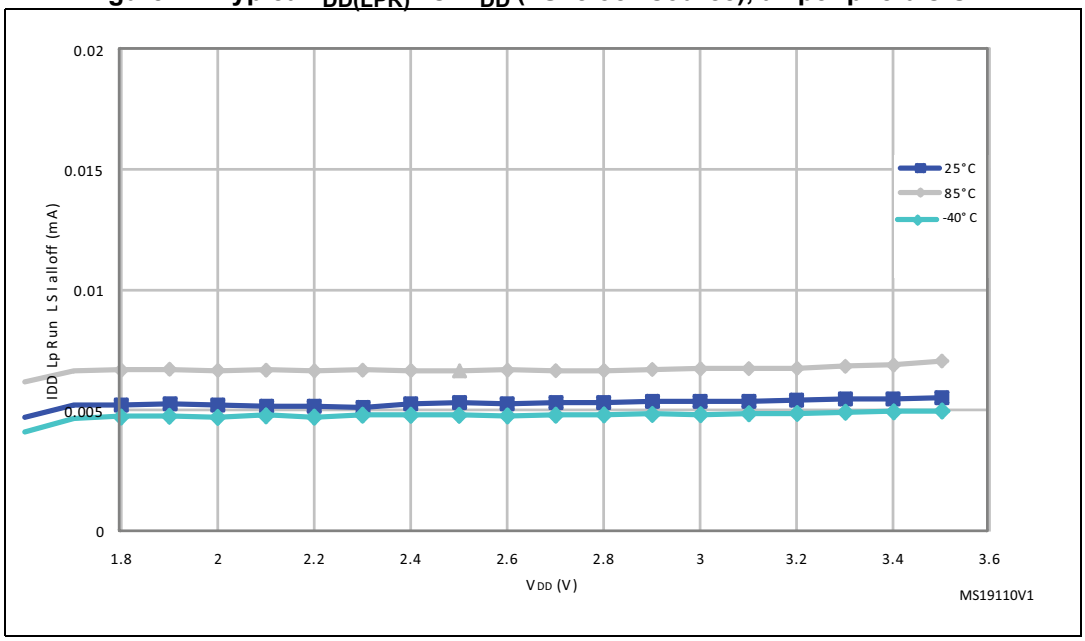


Figure 19. Typical $I_{DD(AH)}$ vs. V_{DD} (LSI clock source)

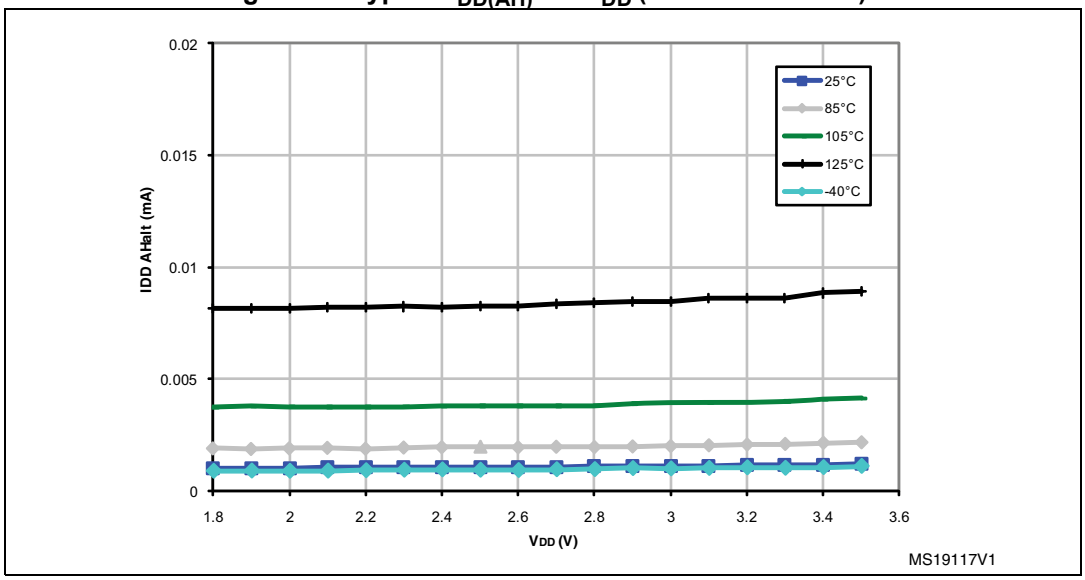


Figure 25. Typical V_{IL} and V_{IH} vs. V_{DD} (standard I/Os)

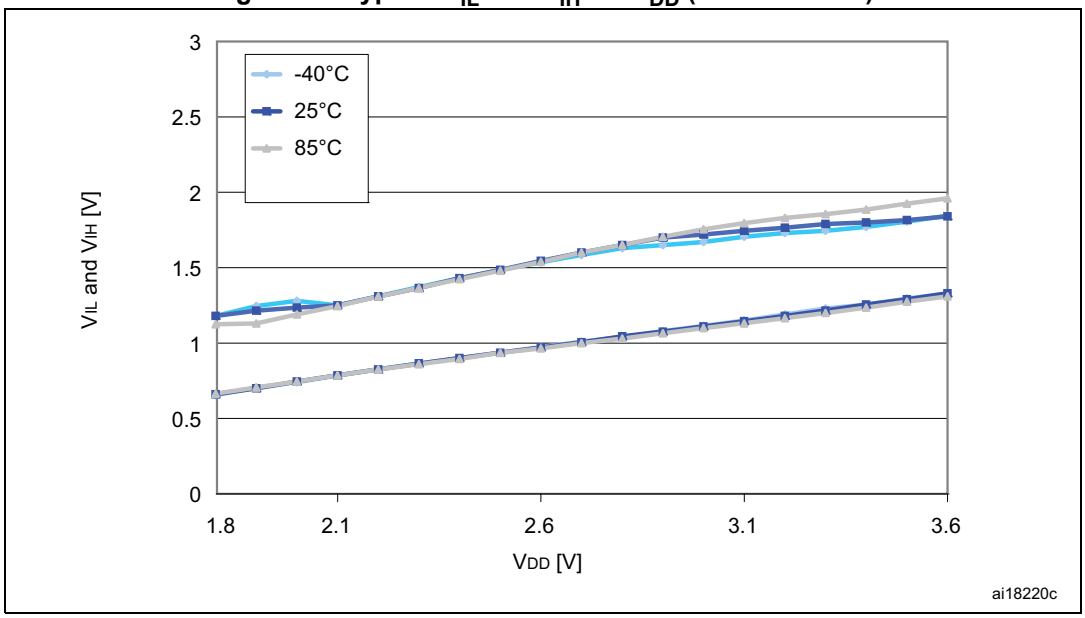
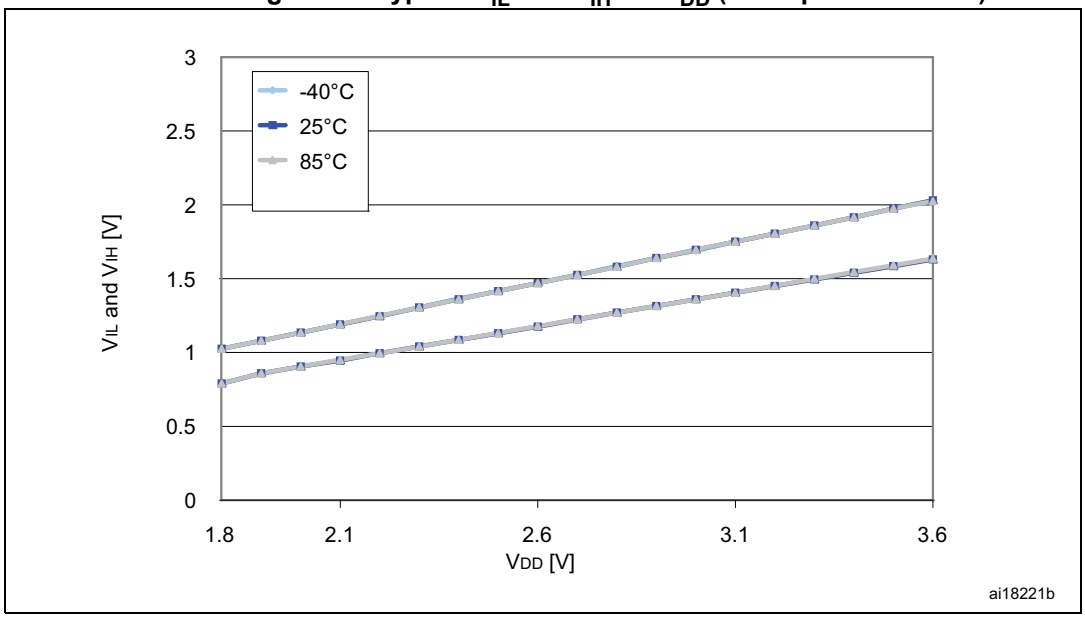


Figure 26. Typical V_{IL} and V_{IH} vs. V_{DD} (true open drain I/Os)



I²C - Inter IC control interface

Subject to general operating conditions for V_{DD}, f_{SYSCLK}, and T_A unless otherwise specified.

The STM8AL I²C interface (I2C1) meets the requirements of the Standard I²C communication protocol described in the following table with the restriction mentioned below:

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (SDA and SCL).

Table 47. I2C characteristics

Symbol	Parameter	Standard mode I²C		Fast mode I²C(1)		Unit
		Min.(2)	Max. (2)	Min. (2)	Max. (2)	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0	-	0	900	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	-	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	START condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated START condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	STOP condition setup time	4.0	-	0.6	-	
$t_{w(STO:STA)}$	STOP to START condition time (bus free)	4.7	-	1.3	-	
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. f_{SYSCLK} must be at least equal to 8 MHz to achieve max fast I²C speed (400 kHz).
2. Data based on standard I²C protocol requirement, not tested in production.

Note: For speeds around 200 kHz, the achieved speed has a ±5% tolerance.
For other speed ranges, the achieved speed has a ±2% tolerance.
The above variations depend on the accuracy of the external components used.

In the following table, data are based on characterization results, not tested in production.

Table 54. DAC accuracy

Symbol	Parameter	Conditions	Typ.	Max.(1)	Unit
DNL	Differential non linearity(2)	R_L ≥5 kΩ, C_L≤50 pF DACOUT buffer ON(3)	1.5	3	12-bit LSB
		No load DACOUT buffer OFF	1.5	3	
INL	Integral non linearity(4)	R_L ≥5 kΩ, C_L≤ 50 pF DACOUT buffer ON(3)	2	4	
		No load DACOUT buffer OFF	2	4	
Offset	Offset error(5)	R_L ≥5 kΩ, C_L≤ 50 pF DACOUT buffer ON(3)	±10	±25	
		No load DACOUT buffer OFF	±5	±8	
Offset1	Offset error at Code 1 (6)	DACOUT buffer OFF	±1.5	±5	
Gain error	Gain error(7)	R_L ≥5 kΩ, C_L≤ 50 pF DACOUT buffer ON(3)	+0.1/-0.2	+0.2/-0.5	%
		No load DACOUT buffer OFF	+0/-0.2	+0/-0.4	
TUE	Total unadjusted error	R_L ≥5 kΩ, C_L≤ 50 pF DACOUT buffer ON(3)	12	30	12-bit LSB
		No load -DACOUT buffer OFF	8	12	

1. Not tested in production.
2. Difference between two consecutive codes - 1 LSB.
3. In 48-pin package devices the DAC2 output buffer must be kept off and no load must be applied on the DAC_OUT2 output.
4. Difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023.
5. Difference between the value measured at Code (0x800) and the ideal value = V_{REF+}/2.
6. Difference between the value measured at Code (0x001) and the ideal value.
7. Difference between the ideal slope of the transfer function and the measured slope computed from Code 0x000 and 0xFFF when buffer is ON, and from Code giving 0.2 V and (V_{DDA} -0.2) V when buffer is OFF.

9.3.14 12-bit ADC1 characteristics

In the following table, data are guaranteed by design, not tested in production.

Table 56. ADC1 characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	Analog supply voltage	-	1.8	-	3.6	V
V_{REF+}	Reference supply voltage	2.4 V ≤V_{DDA}≤ 3.6 V	2.4	-	V_{DDA}	V
		1.8 V≤V_{DDA}≤ 2.4 V	V_{DDA}			V
V_{REF-}	Lower reference voltage	-	V_{SSA}			V
I_{VDDA}	Current on the V_{DDA} input pin	-	-	1000	1450	µA
I_{VREF+}	Current on the V_{REF+} input pin	-	-	400	700 (peak)(1)	µA
		-	-		450 (average)(1)	µA
V_{AIN}	Conversion voltage range	-	0(2)	-	V_{REF+}	
T_A	Temperature range	-	-40	-	125	°C
R_{AIN}	External resistance on V_{AIN}	on PF0/1/2/3 fast channels	-	-	50(3)	kΩ
		on all other channels	-	-		
C_{ADC}	Internal sample and hold capacitor	on PF0/1/2/3 fast channels	-	16	-	pF
		on all other channels	-		-	
f_{ADC}	ADC sampling clock frequency	2.4 V≤V_{DDA}≤3.6 V without zooming	0.320	-	16	MHz
		1.8 V≤V_{DDA}≤2.4 V with zooming	0.320	-	8	MHz
f_{CONV}	12-bit conversion rate	V_{AIN} on PF0/1/2/3 fast channels	-	-	1(3)(4)	MHz
		V_{AIN} on all other channels	-	-	760(3)(4)	kHz
f_{TRIG}	External trigger frequency	-	-	-	t_{conv}	$1/f_{ADC}$
t_{LAT}	External trigger latency	-	-	-	3.5	$1/f_{SYSCLK}$

Electromagnetic interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm IEC61967-2 which specifies the board and the loading of each pin.

Table 61. EMI data (1)

Symbol	Parameter	Conditions	Monitored frequency band	Max vs.	Unit
				16 MHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = +25 °C, LQFP80 conforming to IEC61967-2	0.1 MHz to 30 MHz	10	dBµV
			30 MHz to 130 MHz	4	
			130 MHz to 1 GHz	1	
			EMI Level	1.5	-

1. Guaranteed by characterization results.

Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic discharge (ESD)

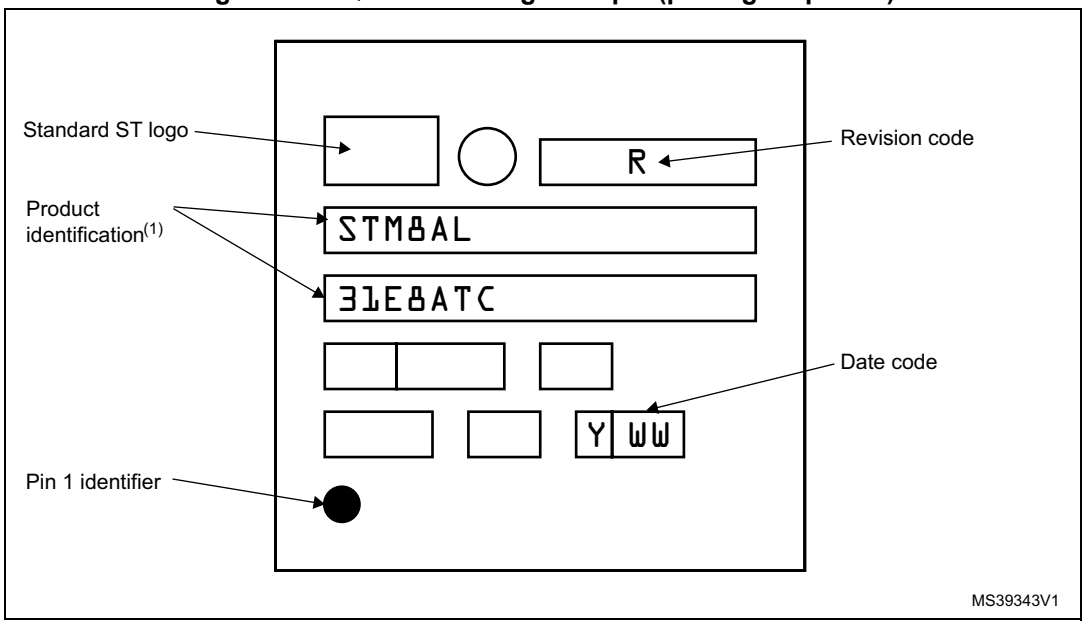
Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). Two models are simulated: human body model and charge device model. This test conforms to the ANSI/ESDA/JEDEC JS-001, JESD22-A115 and ANSI/ESD S5.3.1.

Table 62. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value (1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = 25 °C, conforming to ANSI/ESDA/ JEDEC JS-001	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = 25 °C, conforming to ANSI/ESD S5.3.1	C4B	500	
$V_{ESD(MM)}$	Electrostatic discharge voltage (machine model)	T_A = 25 °C, conforming to JESD22-A115	M2	200	

1. Guaranteed by characterization results.

Figure 48. LQFP80 marking example (package top view)



1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted to run a qualification activity prior to any decision to use these engineering samples.