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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	68
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 28x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8al3le8atay

Table 1. Device summary

Reference	Part number
STM8AL31E8x	STM8AL31E88, STM8AL31E89, STM8AL31E8A
STM8AL3LE8x	STM8AL3LE88, STM8AL3LE89, STM8AL3LE8A

List of figures

3.2 Central processing unit STM8

3.2.1 Advanced STM8 Core

The 8-bit STM8 core is designed for code efficiency and performance with an Harvard architecture and a 3-stage pipeline.

It contains 6 internal registers which are directly addressable in each execution context, 20 addressing modes including indexed indirect and relative addressing, and 80 instructions.

Architecture and registers

- Harvard architecture
- 3-stage pipeline
- 32-bit wide program memory bus - single cycle fetching most instructions
- X and Y 16-bit index registers - enabling indexed addressing modes with or without offset and read-modify-write type data manipulations
- 8-bit accumulator
- 24-bit program counter - 16 Mbyte linear memory space
- 16-bit stack pointer - access to a 64 Kbyte level stack
- 8-bit condition code register - 7 condition flags for the result of the last instruction

Addressing

- 20 addressing modes
- Indexed indirect addressing mode for lookup tables located anywhere in the address space
- Stack pointer relative addressing mode for local variables and parameter passing

Instruction set

- 80 instructions with 2-byte average instruction size
- Standard data movement and logic/arithmetic functions
- 8-bit by 8-bit multiplication
- 16-bit by 8-bit and 16-bit by 16-bit division
- Bit manipulation
- Data transfer between stack and accumulator (push/pop) with direct stack access
- Data transfer using the X and Y registers or direct memory-to-memory transfers

3.2.2 Interrupt controller

The high-density STM8AL3xE8x devices feature a nested vectored interrupt controller:

- Nested interrupts with 3 software priority levels
- 32 interrupt vectors with hardware priority
- Up to 40 external interrupt sources on 11 vectors
- Trap and reset interrupts

3.6 LCD (Liquid crystal display)

The LCD is only available on STM8AL3LE8x devices.

The liquid crystal display drives up to 8 common terminals and up to 40 segment terminals to drive up to 320 pixels. This LCD is configurable to drive up to 4 common and 44 segments (up to 176 pixels).

- Internal step-up converter to guarantee contrast control whatever V_{DD}.
- Static 1/2, 1/3, 1/4, 1/8 duty supported.
- Static 1/2, 1/3, 1/4 bias supported.
- Phase inversion to reduce power consumption and EMI.
- Up to 8 pixels programmable to blink.
- The LCD controller operating in Halt mode.

Note: Unnecessary segments and common pins can be used as general I/O pins.

3.7 Memories

The high-density STM8AL3xE8x devices have the following main features:

- 4 Kbytes of RAM
- The non-volatile memory is divided into three arrays:
  - 64 Kbytes of medium-density embedded Flash program memory
  - 2 Kbytes of Data EEPROM
  - Option byte.

The memory supports the read-while-write (RWW): it is possible to execute the code from the program matrix while programming/erasing the data matrix.

The option byte protects part of the Flash program memory from write and readout piracy.

3.8 DMA

A 4-channel direct memory access controller (DMA1) offers a memory-to-memory and peripherals-from/to-memory transfer capability. The 4 channels are shared between the following IPs with DMA capability: ADC1, DAC1,DAC2, AES, I2C1, SPI1, SPI2, USART1, USART2, USART3, and the 5 Timers.

3.17.3 USART

The USART interfaces (USART1, USART2 and USART3) allow full duplex, asynchronous communications with external devices requiring an industry standard NRZ asynchronous serial data format. It offers a very wide range of baud rates.

- 1 Mbit/s full duplex SCI
- SPI1 emulation
- High precision baud rate generator
- Smartcard emulation
- IrDA SIR encoder decoder
- Single wire half duplex mode

Note: USART1, USART2 and USART3 can be served by the DMA1 Controller.

USART interfaces are used to implement LIN slave communication, with LIN Break detection on the framing error flag (FE in USART_SR register) with a value of 0 in the USART data register (USART_DR).

3.18 Infrared (IR) interface

The high-density STM8AL3xE8x devices contain an infrared interface which is used with an IR LED for remote control functions. Two timer output compare channels are used to generate the infrared remote control signals.

3.19 Development support

Development tools

Development tools for the STM8 microcontrollers include:

- The STice emulation system offering tracing and code profiling
- The STVD high-level language debugger including C compiler, assembler and integrated development environment
- The STVP Flash programming software

The STM8 also comes with starter kits, evaluation boards and low-cost in-circuit debugging/programming tools.

Single wire data interface (SWIM) and debug module

The debug module with its single wire data interface (SWIM) permits non-intrusive real-time in-circuit debugging and fast memory programming.

The Single wire interface is used for direct access to the debugging module and memory programming. The interface is activated in all device operation modes.

The non-intrusive debugging module features a performance close to a full-featured emulator. Beside memory and peripherals, CPU operation is also monitored in real-time by means of shadow registers.

Table 5. High-density STM8AL3xE8x pin description (continued)

Pin number			Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP80	LQFP64	LQFP48				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
64	52	-	PG7/LCD_SEG35/ SPI2_MISO	I/O	FT(5)	**X**	X	X	HS	X	X	**Port G7**	LCD segment 35 / SPI2 master in- slave out
23	-	-	PE0/LCD_SEG1(3)/ TIM5_CH2	I/O	FT(5)	**X**	X	X	HS	X	X	**Port E0**	LCD segment 1 /Timer 5 channel 2
-	19	14	PE0/LCD_SEG1(3)/ TIM5_CH2/RTC_TAMP1	I/O	FT(5)	**X**	X	X	HS	X	X	**Port E0**	LCD segment 1 /Timer 5 channel 2 / RTC tamper 1
24	-	-	PE1/TIM1_CH2N /LCD_SEG2(3)	I/O	FT(5)	**X**	X	X	HS	X	X	**Port E1**	Timer 1 - inverted channel 2 / LCD segment 2
-	20	15	PE1/TIM1_CH2N /LCD_SEG2(3)/ RTC_TAMP2	I/O	FT(5)	**X**	X	X	HS	X	X	**Port E1**	Timer 1 - inverted channel 2 / LCD segment 2 / RTC tamper 2
25	-	-	PE2/TIM1_CH3N /LCD_SEG3(3)	I/O	FT(5)	**X**	X	X	HS	X	X	**Port E2**	Timer 1 - inverted channel 3 / LCD segment 3
-	21	16	PE2/TIM1_CH3N /LCD_SEG3(3)/ RTC_TAMP3	I/O	FT(5)	**X**	X	X	HS	X	X	**Port E2**	Timer 1 - inverted channel 3 / LCD segment 3 / RTC tamper 3
26	-	-	PE3/LCD_SEG4(3)	I/O	FT(5)	**X**	X	X	HS	X	X	**Port E3**	LCD segment 4
-	22	17	PE3/LCD_SEG4(3)/ USART2_RX	I/O	FT(5)	**X**	X	X	HS	X	X	**Port E3**	LCD segment 4/ USART2 receive
27	-	-	PE4/LCD_SEG5(3)/ DAC_TRIG1	I/O	FT(5)	**X**	X	X	HS	X	X	**Port E4**	LCD segment 5/ DAC 1 trigger
-	23	18	PE4/LCD_SEG5(3)/ DAC_TRIG2/USART2_TX	I/O	FT(5)	**X**	X	X	HS	X	X	**Port E4**	LCD segment 5/ DAC 2 trigger/ USART2 transmit
28	-	-	PE5/LCD_SEG6(3)/ ADC1_IN23/COMP1_INP/ COMP2_INP	I/O	FT(5)	**X**	X	X	HS	X	X	**Port E5**	LCD segment 6 / ADC1_IN23/Comparator 1 positive input/Comparator 2 positive input
-	24	19	PE5/LCD_SEG6(3)/ ADC1_IN23/COMP1_INP/ COMP2_INP/ USART2_CK	I/O	FT(5)	**X**	X	X	HS	X	X	**Port E5**	LCD segment 6 / ADC1_IN23/ Comparator 1 positive input/ Comparator 2 positive input/USART2 synchronous clock
-	-	47	PE6/LCD_SEG26(3)/ PVD_IN/TIM5_BKIN/ USART3_TX	I/O	FT(5)	**X**	X	X	HS	X	X	**Port E6**	LCD segment 26 /PVD_IN /TIM5 break input / USART3 transmit

Table 5. High-density STM8AL3xE8x pin description (continued)

Pin number			Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP80	LQFP64	LQFP48				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
5	1	1	PA0[8]/*[USART1_CK]*[2]/ SWIM/BEEP/IR_TIM [9]	I/O	-	X	**X**	X	HS	X	X	**Port A0**	*[USART1 synchronous clock]*[2] / SWIM input and output / Beep output / Infrared Timer output
68	56	40	V_{SS2}	S	-	**-**	-	-	-	-	-	IOs ground voltage	
67	55	39	V_{DD2}	S	-	**-**	-	-	-	-	-	IOs supply voltage	
48	-	-	V_{SS4}	S	-	**-**	-	-	-	-	-	IOs ground voltage	
47	-	-	V_{DD4}	S	-	**-**	-	-	-	-	-	IOs supply voltage	

1. At power-up, the PA1/NRST pin is a reset input pin with pull-up. To be used as a general purpose pin (PA1), it can be configured only as output open-drain or push-pull, not as a general purpose input. Refer to Section *Configuring NRST/PA1 pin as general purpose output* in STM8L051/L052 Value Line, STM8L151/L152, STM8L162, STM8AL31, STM8AL3L MCU lines reference manual (RM0031).
2. [ ] Alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).
3. Available onSTM8AL3LE8xdevices only.
4. A pull-up is applied to PB0 and PB4 during the reset phase. These two pins are input floating after reset release.
5. In the 5 V tolerant I/Os, the protection diode to V_{DD} is not implemented.
6. In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer, weak pull-up and protection diode to V_{DD} are not implemented).
7. Available on STM8AL3LE8x devices only. On STM8AL31E8x devices it is reserved and must be tied to V_{DD}.
8. The PA0 pin is in input pull-up during the reset phase and after reset release.
9. High Sink LED driver capability available on PA0.

Note: The slope control of all GPIO pins, except true open drain pins, are programmable. By default the slope control is limited to 2 MHz.

System configuration options

As shown in *Table 5: High-density STM8AL3xE8x pin description*, some alternate functions can be remapped on different I/O ports by programming one of the two remapping registers described in the "Routing interface (RI) and system configuration controller" section in STM8L051/L052 Value Line, STM8L151/L152, STM8L162, STM8AL31, STM8AL3L MCU lines reference manual (RM0031).

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 52D2	TIM1	TIM1_DCR2	TIM1 DMA1 control register 2	0x00
0x00 52D3		TIM1_DMA1R	TIM1 DMA1 address for burst mode	0x00
0x00 52D4 to 0x00 52DF	Reserved area (12 byte)			
0x00 52E0	TIM4	TIM4_CR1	TIM4 control register 1	0x00
0x00 52E1		TIM4_CR2	TIM4 control register 2	0x00
0x00 52E2		TIM4_SMCR	TIM4 Slave mode control register	0x00
0x00 52E3		TIM4_DER	TIM4 DMA1 request enable register	0x00
0x00 52E4		TIM4_IER	TIM4 Interrupt enable register	0x00
0x00 52E5		TIM4_SR1	TIM4 status register 1	0x00
0x00 52E6		TIM4_EGR	TIM4 Event generation register	0x00
0x00 52E7		TIM4_CNTR	TIM4 counter	0x00
0x00 52E8		TIM4_PSCR	TIM4 prescaler register	0x00
0x00 52E9		TIM4_ARR	TIM4 Auto-reload register	0x00
0x00 52EA to 0x00 52FE	Reserved area (21 byte)			
0x00 52FF	IRTIM	IR_CR	Infrared control register	0x00
0x00 5300	TIM5	TIM5_CR1	TIM5 control register 1	0x00
0x00 5301		TIM5_CR2	TIM5 control register 2	0x00
0x00 5302		TIM5_SMCR	TIM5 Slave mode control register	0x00
0x00 5303		TIM5_ETR	TIM5 external trigger register	0x00
0x00 5304		TIM5_DER	TIM5 DMA1 request enable register	0x00
0x00 5305		TIM5_IER	TIM5 interrupt enable register	0x00
0x00 5306		TIM5_SR1	TIM5 status register 1	0x00
0x00 5307		TIM5_SR2	TIM5 status register 2	0x00
0x00 5308		TIM5_EGR	TIM5 event generation register	0x00
0x00 5309		TIM5_CCMR1	TIM5 Capture/Compare mode register 1	0x00
0x00 530A		TIM5_CCMR2	TIM5 Capture/Compare mode register 2	0x00
0x00 530B		TIM5_CCER1	TIM5 Capture/Compare enable register 1	0x00
0x00 530C		TIM5_CNTRH	TIM5 counter high	0x00
0x00 530D		TIM5_CNTRL	TIM5 counter low	0x00
0x00 530E		TIM5_PSCR	TIM5 prescaler register	0x00
0x00 530F		TIM5_ARRH	TIM5 Auto-reload register high	0xFF

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 53AC	DAC	DAC_DORH	DAC data output register high	0x00
0x00 53AD		DAC_DORL	DAC data output register low	0x00
0x00 53A2		DAC_DCH2RDHRH	DAC channel 2 right aligned data holding register high	0x00
0x00 53A3		DAC_DCH2RDHRL	DAC channel 2 right aligned data holding register low	0x00
0x00 53A4		DAC_DCH1LDHRH	DAC channel 1left aligned data holding register high	0x00
0x00 53A5		DAC_DCH1LDHRL	DAC channel 1left aligned data holding register low	0x00
0x00 53A6		DAC_DCH2LDHRH	DAC channel 2 left aligned data holding register high	0x00
0x00 53A7		DAC_DCH2LDHRL	DAC channel 2 left aligned data holding register low	0x00
0x00 53A8		DAC_DCH1DHR8	DAC channel 1 8-bit mode data holding register	0x00
0x00 53A9		DAC_DCH2DHR8	DAC channel 2 8-bit mode data holding register	0x00
0x00 53AA to 0x00 53AB	Reserved area (2 byte)			
0x00 53AC	DAC	DAC_CH1DORH Reset value	DAC channel 1 data output register high	0x00
0x00 53AD		DAC_CH1DORL Reset value	DAC channel 1 data output register low	0x00
0x00 53AE to 0x00 53AF	Reserved area (2 byte)			
0x00 53B0	DAC	DAC_CH2DORH Reset value	DAC channel 2 data output register high	0x00
0x00 53B1		DAC_CH2DORL Reset value	DAC channel 2 data output register low	0x00
0x00 53B2 to 0x00 53BF	Reserved area			
0x00 53C0	SPI2	SPI2_CR1	SPI2 control register 1	0x00
0x00 53C1		SPI2_CR2	SPI2 control register 2	0x00
0x00 53C2		SPI2_ICR	SPI2 interrupt control register	0x00
0x00 53C3		SPI2_SR	SPI2 status register	0x02
0x00 53C4		SPI2_DR	SPI2 data register	0x00
0x00 53C5		SPI2_CRCPR	SPI2 CRC polynomial register	0x07
0x00 53C6		SPI2_RXCRCR	SPI2 Rx CRC register	0x00
0x00 53C7		SPI2_TXCRCR	SPI2 Tx CRC register	0x00

Table 10. CPU/SWIM/debug module/interrupt controller registers (continued)

Address	Block	Register label	Register name	Reset status
0x00 7F90	DM	DM_BK1RE	DM breakpoint 1 register extended byte	0xFF
0x00 7F91		DM_BK1RH	DM breakpoint 1 register high byte	0xFF
0x00 7F92		DM_BK1RL	DM breakpoint 1 register low byte	0xFF
0x00 7F93		DM_BK2RE	DM breakpoint 2 register extended byte	0xFF
0x00 7F94		DM_BK2RH	DM breakpoint 2 register high byte	0xFF
0x00 7F95		DM_BK2RL	DM breakpoint 2 register low byte	0xFF
0x00 7F96		DM_CR1	DM Debug module control register 1	0x00
0x00 7F97		DM_CR2	DM Debug module control register 2	0x00
0x00 7F98		DM_CSR1	DM Debug module control/status register 1	0x10
0x00 7F99		DM_CSR2	DM Debug module control/status register 2	0x00
0x00 7F9A		DM_ENFCTR	DM enable function register	0xFF
0x00 7F9B to 0x00 7F9F	Reserved area (5 byte)			

1. Accessible by debug module only

Table 25. Total current consumption and timing in Active-halt mode at V_{DD} = 1.65 V to 3.6 V (continued)

Symbol	Parameter	Conditions(1)			Typ.	Max.(2)	Unit
$t_{WU\_HSI(AH)}$(9)(10)	Wakeup time from Active-halt mode to Run mode (using HSI)	-	-	-	4.70	7.00	µs
$t_{WU\_LSI(AH)}$(9)(10)	Wakeup time from Active-halt mode to Run mode (using LSI)	-	-	-	150.0	-	µs

1. No floating I/O, unless otherwise specified.
2. Guaranteed by characterization results.
3. RTC enabled. Clock source = LSI
4. RTC enabled, LCD enabled with external V_{LCD} = 3 V, static duty, division ratio = 256, all pixels active, no LCD connected.
5. RTC enabled, LCD enabled with external V_{LCD}, 1/4 duty, 1/3 bias, division ratio = 64, all pixels active, no LCD connected.
6. LCD enabled with internal LCD booster V_{LCD} = 3 V, 1/4 duty, 1/3 bias, division ratio = 64, all pixels active, no LCD connected.
7. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ LSE}$) must be added. Refer to *Table 33*
8. RTC enabled. Clock source = LSE
9. Wakeup time until start of interrupt vector fetch.
   The first word of interrupt routine is fetched 4 CPU cycles after t_{WU}.
10. ULP=0 or ULP=1 and FWU=1 in the PWR_CSR2 register.

Table 26. Typical current consumption in Active-halt mode, RTC clocked by LSE external crystal

Symbol	Parameter	Condition(1)		Typ.	Unit
$I_{DD(AH)}$ (2)	Supply current in Active-halt mode	V_{DD} = 1.8 V	LSE	1.15	µA
			LSE/32(3)	1.05	
		V_{DD} = 3 V	LSE	1.30	
			LSE/32(3)	1.20	
		V_{DD} = 3.6 V	LSE	1.45	
			LSE/32(3)	1.35	

1. No floating I/O, unless otherwise specified.
2. Based on measurements on bench with 32.768 kHz external crystal oscillator.
3. RTC clock is LSE divided by 32.

Table 28. Peripheral current consumption (continued)

Symbol	Parameter		Typ. V_{DD} = 3.0 V	Unit
$I_{DD(TIM1)}$	TIM1 supply current(1)		10	µA/MHz
$I_{DD(TIM2)}$	TIM2 supply current (4)		7	
$I_{DD(TIM3)}$	TIM3 supply current (1)		7	
$I_{DD(TIM5)}$	TIM5 supply current (1)		7	
$I_{DD(TIM4)}$	TIM4 timer supply current (1)		3	
$I_{DD(USART1)}$	USART1 supply current (5)		5	
$I_{DD(USART2)}$	USART2 supply current (6)		5	
$I_{DD(USART3)}$	USART3 supply current (7)		5	
$I_{DD(SPI1)}$	SPI1 supply current (4)		3	
$I_{DD(SPI2)}$	SPI2 supply current (4)		3	
$I_{DD(I2C1)}$	I^2C1 supply current (4)		4	
$I_{DD(DMA1)}$	DMA1 supply current		3	
$I_{DD(AES)}$	AES supply current		4	
$I_{DD(WWDG)}$	WWDG supply current		1	
$I_{DD(ALL)}$	Peripherals ON(8)		67	
$I_{DD(ADC1)}$	ADC1 supply current(9)		1500	µA
$I_{DD(DAC)}$	DAC supply current(10)		370	
$I_{DD(COMP1)}$	Comparator 1 supply current(11)		0.160	
$I_{DD(COMP2)}$	Comparator 2 supply current(11)	Slow mode	2	
		Fast mode	5	
$I_{DD(PVD/BOR)}$	Power voltage detector and brownout Reset unit supply current (12)		2.6	
$I_{DD(BOR)}$	Brownout Reset unit supply current (12)		2.4	
$I_{DD(IDWDG)}$	Independent watchdog supply current	including LSI supply current	0.45	
		excluding LSI supply current	0.05	

1. Data based on a differential I_{DD} measurement between all peripherals OFF and a timer counter running at 16 MHz. The CPU is in Wait mode in both cases. No IC/OC programmed, no I/O pins toggling. Not tested in production.
2. Data based on a differential I_{DD} measurement between the on-chip peripheral in reset configuration and not clocked and the on-chip peripheral when clocked and not kept under reset. The CPU is in Wait mode in both cases. No I/O pins toggling. Not tested in production.
3. Peripherals listed above the $I_{DD(ALL)}$ parameter ON: TIM1, TIM2, TIM3, TIM4, TIM5, USART1, USART2, USART3, SPI1, SPI2, I2C1, DMA1, WWDG.
4. Data based on a differential I_{DD} measurement between all peripherals OFF and a timer counter running at 16 MHz. The CPU is in Wait mode in both cases. No IC/OC programmed, no I/O pins toggling. Not tested in production.

5. Data based on a differential I_{DD} measurement between the on-chip peripheral in reset configuration and not clocked and the on-chip peripheral when clocked and not kept under reset. The CPU is in Wait mode in both cases. No I/O pins toggling. Not tested in production.
6. Data based on a differential I_{DD} measurement between the on-chip peripheral in reset configuration and not clocked and the on-chip peripheral when clocked and not kept under reset. The CPU is in Wait mode in both cases. No I/O pins toggling. Not tested in production.
7. Data based on a differential I_{DD} measurement between the on-chip peripheral in reset configuration and not clocked and the on-chip peripheral when clocked and not kept under reset. The CPU is in Wait mode in both cases. No I/O pins toggling. Not tested in production.
8. Peripherals listed above the $I_{DD(ALL)}$ parameter ON: TIM1, TIM2, TIM3, TIM4, USART1, SPI1, I2C1, DMA1, WWDG.
9. Data based on a differential I_{DD} measurement between ADC in reset configuration and continuous ADC conversion.
10. Data based on a differential I_{DD} measurement between DAC in reset configuration and continuous DAC conversion of V_{DD} /2. Floating DAC output.
11. Data based on a differential I_{DD} measurement between COMP1 or COMP2 in reset configuration and COMP1 or COMP2 enabled with static inputs. Supply current of internal reference voltage excluded.
12. Including supply current of internal reference voltage.

Table 29. Current consumption under external reset

Symbol	Parameter	Conditions		Typ.	Unit
$I_{DD(RST)}$	Supply current under external reset (1)	PB1/PB3/PA5 pins are externally tied to V_{DD}	V_{DD} = 1.8 V	48	µA
			V_{DD} = 3 V	80	
			V_{DD} = 3.6 V	95	

1. All pins except PA0, PB0 and PB4 are floating under reset. PA0, PB0 and PB4 are configured with pull-up under reset. PB1, PB3 and PA5 must be tied externally under reset to avoid the consumption due to their schmitt trigger.

9.3.4 Clock and timing characteristics

HSE external clock (HSEBYP = 1 in CLK_ECKCR)

Subject to general operating conditions for V_{DD} and T_A.

Table 30. HSE external clock characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{HSE_ext} (1)	External clock source frequency	-	1	-	16	MHz
V_{HSEH}	OSC_IN input pin high-level voltage		0.7 x V_{DD}	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low-level voltage		V_{SS}	-	0.3 x V_{DD}	
$C_{in(HSE)}$ (1)	OSC_IN input capacitance	-	-	2.6	-	pF
I_{LEAK_HSE}	OSC_IN input leakage current	$V_{SS} < V_{IN} < V_{DD}$	-	-	±500	nA

1. Guaranteed by design.

Table 41. I/O static characteristics

Symbol	Parameter	Conditions[1]	Min.	Typ.	Max.	Unit
V_{IL}	Input low-level voltage	Input voltage on all pins	Vss-0.3	-	0.3 x V_{DD}	V
V_{IH}	Input high-level voltage	Input voltage on true open-drain pins (PC0 and PC1) with V_{DD} < 2 V	0.70 x V_{DD}	-	5.2[2]	V
		Input voltage on true open-drain pins (PC0 and PC1) with $V_{DD} \geq 2$ V		-	5.5[2]	
		Input voltage on five-volt tolerant (FT) pins with V_{DD} < 2 V		-	5.2[2]	
		Input voltage on five-volt tolerant (FT) pins with $V_{DD} \geq 2$ V		-	5.5[2]	
		Input voltage on any other pin		-	V_{DD}+0.3[2]	
V_{hys}	Schmitt trigger voltage hysteresis [3]	Standard I/Os	-	200	-	mV
		True open drain I/Os	-	200	-	
I_{lkg}	Input leakage current [4]	$V_{SS} \leq V_{IN} \leq V_{DD}$ Standard I/Os	-	-	50	nA
		$V_{SS} \leq V_{IN} \leq V_{DD}$ True open drain I/Os	-	-	200	
		$V_{SS} \leq V_{IN} \leq V_{DD}$ PA0 with high sink LED driver capability	-	-	200	
R_{PU}	Weak pull-up equivalent resistor[5]	$V_{IN}=V_{SS}$	30[6]	45	60[6]	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. V_{DD} = 3.0 V, T_A = -40 to 125 °C unless otherwise specified.
2. If V_{IH} maximum is not respected, the injection current must be limited externally to $I_{INJ(PIN)}$ maximum.
3. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested.
4. The max. value may be exceeded if negative current is injected on adjacent pins.
5. R_{PU} pull-up equivalent resistor based on a resistive transistor (corresponding I_{PU} current characteristics described in *Figure 28*).
6. Guaranteed by characterization results.

Table 42. Output driving current (high sink ports)

I/O Type	Symbol	Parameter	Conditions	Min.	Max.	Unit
Standard	V_{OL} (1)	Output low-level voltage for an I/O pin	I_{IO} = +2 mA, V_{DD} = 3.0 V	-	0.45	V
			I_{IO} = +2 mA, V_{DD} = 1.8 V	-	0.45	V
			I_{IO} = +10 mA, V_{DD} = 3.0 V	-	0.7	V
	V_{OH} (2)	Output high-level voltage for an I/O pin	I_{IO} = -2 mA, V_{DD} = 3.0 V	V_{DD}-0.45	-	V
			I_{IO} = -1 mA, V_{DD} = 1.8 V	V_{DD}-0.45	-	V
			I_{IO} = -10 mA, V_{DD} = 3.0 V	V_{DD}-0.7	-	V

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Table 16* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. The I_{IO} current sourced must always respect the absolute maximum rating specified in *Table 16* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.

Table 43. Output driving current (true open drain ports)

I/O Type	Symbol	Parameter	Conditions	Min.	Max.	Unit
Open drain	V_{OL} (1)	Output low-level voltage for an I/O pin	I_{IO} = +3 mA, V_{DD} = 3.0 V	-	0.45	V
			I_{IO} = +1 mA, V_{DD} = 1.8 V	-	0.45	

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Table 16* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.

Table 44. Output driving current (PA0 with high sink LED driver capability)

I/O Type	Symbol	Parameter	Conditions	Min.	Max.	Unit
IR	V_{OL} (1)	Output low-level voltage for an I/O pin	I_{IO} = +20 mA, V_{DD} = 2.0 V	-	0.45	V

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Table 16* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.

In the following table, data are guaranteed by design, not tested in production, unless otherwise specified.

Table 52. Comparator 2 characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
V_{DDA}	Analog supply voltage	-	1.65	-	3.6	V
V_{IN}	Comparator 2 input voltage range	-	0	-	V_{DDA}	V
t_{START}	Comparator startup time	Fast mode	-	15	20	µs
		Slow mode	-	20	25	
$t_{d\ slow}$	Propagation delay(2) in slow mode	1.65 V ≤V_{DDA} ≤2.7 V	-	1.8	3.5	
		2.7 V ≤V_{DDA} ≤3.6 V	-	2.5	6	
$t_{d\ fast}$	Propagation delay(2) in fast mode	1.65 V ≤V_{DDA} ≤2.7 V	-	0.8	2	
		2.7 V ≤V_{DDA} ≤3.6 V	-	1.2	4	
V_{offset}	Comparator offset error	-	-	±4	±20	mV
$d_{Threshold}/dt$	Threshold voltage temperature coefficient	V_{DDA} = 3.3V T_A = 0 to 50 °C V- = V_{REF+}, 3/4 V_{REF+}, 1/2 V_{REF+}, 1/4 V_{REF+}.	-	15	30	ppm /°C
I_{COMP2}	Current consumption(3)	Fast mode	-	3.5	5	µA
		Slow mode	-	0.5	2	

1. Guaranteed by characterization results.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
3. Comparator consumption only. Internal reference voltage (necessary for comparator operation) is not included.

9.3.13 12-bit DAC characteristics

In the following table, data are guaranteed by design, not tested in production.

Table 53. DAC characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	Analog supply voltage	-	1.8	-	3.6	V
V_{REF+}	Reference supply voltage	-	1.8	-	V_{DDA}	
I_{VREF}	Current consumption on V_{REF+} supply	V_{REF+} = 3.3 V, no load, middle code (0x800)	-	130	220	µA
		V_{REF+} = 3.3 V, no load, worst code (0x000)	-	220	350	
I_{VDDA}	Current consumption on V_{DDA} supply	V_{DDA} = 3.3 V, no load, middle code (0x800)	-	210	320	
		V_{DDA} = 3.3 V, no load, worst code (0x000)	-	320	520	
T_A	Temperature range	-	-40	-	125	°C
R_L (1) (2)	Resistive load	DACOUT buffer ON	5	-		kΩ
R_O	Output impedance	DACOUT buffer OFF	-	8	10	kΩ
C_L (3)	Capacitive load	-	-	-	50	pF
DAC_OUT (4)	DAC_OUT voltage	DACOUT buffer ON	0.2	-	V_{DDA} - 0.2	V
		DACOUT buffer OFF	0	-	V_{REF+} -1 LSB	V
$t_{settling}$	Settling time (full scale: for a 12-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches the final value ±1LSB)	R_L ≥5 kΩ, C_L≤ 50 pF	-	7	12	µs
Update rate	Max frequency for a correct DAC_OUT (@95%) change when small variation of the input code (from code i to i+1LSB).	R_L ≥ 5 kΩ, C_L ≤50 pF	-	-	1	Msps
t_{WAKEUP}	Wakeup time from OFF state. Input code between lowest and highest possible codes.	R_L ≥5 kΩ, C_L≤50 pF	-	9	15	µs
PSRR+	Power supply rejection ratio (to V_{DDA}) (static DC measurement)	R_L≥ 5 kΩ, C_L≤50 pF	-	-60	-35	dB

1. Resistive load between DACOUT and GNDA
2. Output on PF0 or PF1
3. Capacitive load at DACOUT pin
4. It gives the output excursion of the DAC

9.3.15 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electromagnetic susceptibility)

Based on a simple running application on the product (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms to the ANSI/ESDA/JEDEC JS-001, JESD22-A115 and ANSI/ESD S5.3.1.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 61000 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Prequalification trials:

Most of the common failures (unexpected reset and program counter corruption) are reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress is applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software is hardened to prevent unrecoverable errors occurring (see application note AN1015).

Table 60. EMS data

Symbol	Parameter	Conditions		Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{CPU}= 16 MHz, conforms to IEC 61000		2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{CPU} = 16 MHz, conforms to IEC 61000	Using HSI	4A
			Using HSE	2B