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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	68
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 28x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8al3le8atcy

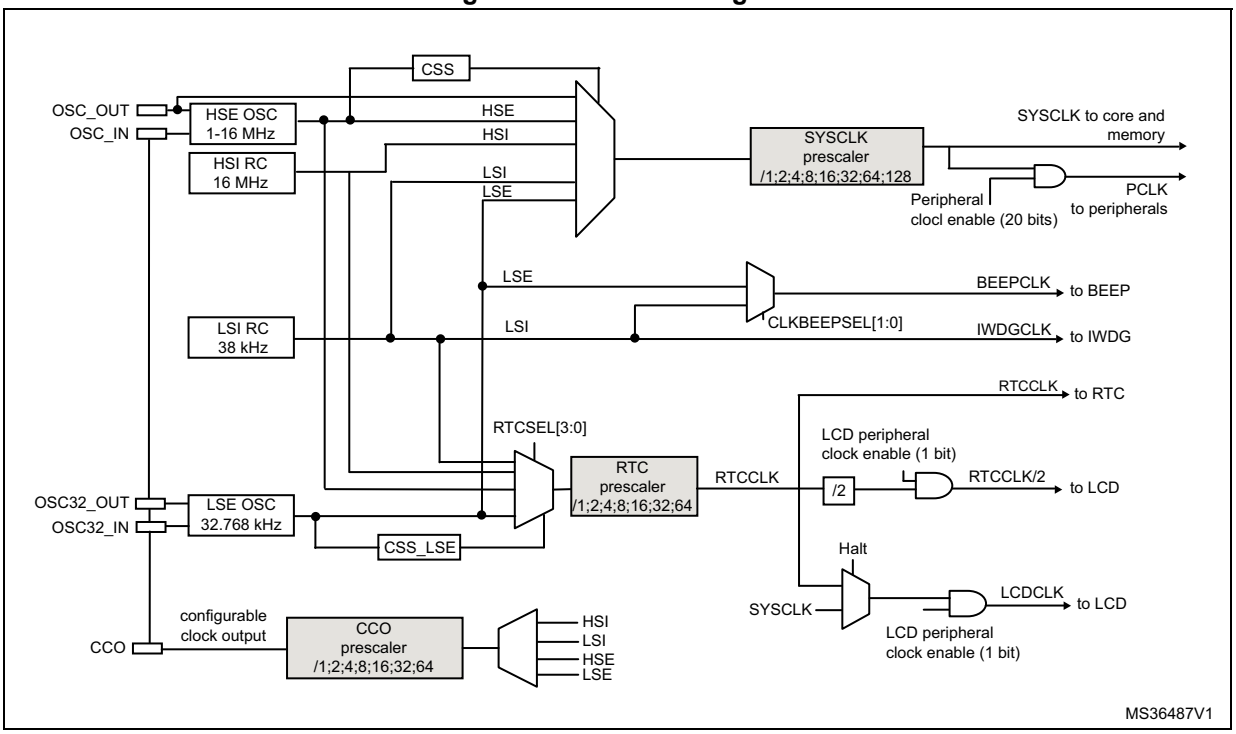
BOR: Brownout reset
DMA: Direct memory access
DAC: Digital-to-analog converter
I²C: Inter-integrated circuit multimaster interface
IWDG: Independent watchdog
LCD: Liquid crystal display
POR/PDR: Power on reset / power-down reset
RTC: Real-time clock
SPI: Serial peripheral interface
SWIM: Single wire interface module
USART: Universal synchronous asynchronous receiver transmitter
WWDG: Window watchdog

3.1 Low-power modes

The high-density STM8AL3xE8x devices support five low-power modes to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- **Wait mode**: CPU clock is stopped, but selected peripherals keep running. An internal or external interrupt or a Reset is used to exit the microcontroller from Wait mode (WFE or WFI mode).
- **Low-power run mode**: The CPU and the selected peripherals are running. Execution is done from RAM with a low speed oscillator (LSI or LSE). Flash memory and data EEPROM are stopped and the voltage regulator is configured in ultra-low-power mode. The microcontroller enters Low-power run mode by software and exits from this mode by software or by a reset.
  All interrupts must be masked and are not used to exit the microcontroller from this mode.
- **Low-power wait mode:** This mode is entered when executing a Wait for event in Low-power run mode. It is similar to Low-power run mode except that the CPU clock is stopped. The wakeup from this mode is triggered by a Reset or by an internal or external event (peripheral event generated by the timers, serial interfaces, DMA controller (DMA1), comparators and I/O ports). When the wakeup is triggered by an event, the system goes back to Low-power run mode.
  All interrupts must be masked and arenot used to exit the microcontroller from this mode.
- **Active-halt mode**: CPU and peripheral clocks are stopped, except RTC. The wakeup is triggered by RTC interrupts, external interrupts or reset.
- **Halt mode**: CPU and peripheral clocks are stopped, the device remains powered on. The RAM content is preserved. The wakeup is triggered by an external interrupt or reset. A few peripherals have also a wakeup from Halt capability. Switching off the internal reference voltage reduces power consumption. Through software configuration it is also possible to wake up the device without waiting for the internal reference voltage wakeup time to have a fast wakeup time of 5 µs.

Figure 2. Clock tree diagram



1. The HSE clock source is either an external crystal/ceramic resonator or an external source (HSE bypass). Refer to Section HSE clock in STM8L051/L052 Value Line, STM8L151/L152, STM8L162, STM8AL31, STM8AL3L MCU lines reference manual (RM0031).
2. The LSE clock source is either an external crystal/ceramic resonator or a external source (LSE bypass). Refer to Section LSE clock in STM8L051/L052 Value Line, STM8L151/L152, STM8L162, STM8AL31, STM8AL3L MCU lines reference manual (RM0031).

3.5 Low-power real-time clock

The real-time clock (RTC) is an independent binary coded decimal (BCD) timer/counter.

Six byte locations contain the second, minute, hour (12/24 hour), week day, date, month, year, in BCD (binary coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day months are made automatically. The subsecond field is also readable in binary format.

The calendar is adjustable from 1 to 32767 RTC clock pulses. This allows to make a synchronization to a master clock.

The RTC offers a digital calibration which allows an accuracy of +/-0.5ppm.

It provides a programmable alarm and programmable periodic interrupts with wakeup from Halt capability.

- Periodic wakeup time using the 32.768 kHz LSE with the lowest resolution (of 61 µs) is from min. 122 µs to max. 3.9 s. With a different resolution, the wakeup time reaches 36 hours
- Periodic alarms based on the calendar are generated from LSE period to every year

A clock security system detects a failure on LSE, and provides an interrupt with wakeup capability. The RTC clock automatically switches to LSI in case of LSE failure.

The RTC also provides 3 anti-tamper detection pins. This detection embeds a programmable filter and wakes-up the MCU.

It is clocked by the internal LSI RC clock source, and thus stays active even in case of a CPU clock failure.

3.16 Beeper

The beeper function outputs a signal on the BEEP pin for sound generation. The signal is in the range of 1, 2 or 4 kHz.

3.17 Communication interfaces

3.17.1 SPI

The serial peripheral interfaces (SPI1 and SPI2) provide half/ full duplex synchronous serial communication with external devices.

- Maximum speed: 8 Mbit/s ($f_{SYSCLK}/2$) both for master and slave
- Full duplex synchronous transfers
- Simplex synchronous transfers on 2 lines with a possible bidirectional data line
- Master or slave operation - selectable by hardware or software
- Hardware CRC calculation
- Slave/master selection input pin

Note: SPI1 and SPI2 can be served by the DMA1 Controller.

3.17.2 I^2C

The I^2C bus interface (I2C1) provides multi-master capability, and controls all I²C bus-specific sequencing, protocol, arbitration and timing.

- Master, slave and multi-master capability
- Standard mode up to 100 kHz and fast speed modes up to 400 kHz.
- 7-bit and 10-bit addressing modes.
- SMBus 2.0 and PMBus support
- Hardware CRC calculation

Note: I^2C1 can be served by the DMA1 Controller.

Table 5. High-density STM8AL3xE8x pin description (continued)

Pin number			Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP80	LQFP64	LQFP48				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
73	61	45	PC6/OSC32_OUT/ *[SPI1_SCK]*(2)/ *[USART1_RX]*(2)	I/O	FT(5)	**X**	X	X	HS	X	X	**Port C6**	LSE oscillator output */ [SPI1 clock] / [USART1 receive]*
74	62	-	PC7/LCD_SEG25(3)/ ADC1_IN3/COMP2_INM/ COMP1_INP	I/O	FT(5)	**X**	X	X	HS	X	X	**Port C7**	LCD segment 25 /ADC1_IN3/ Comparator negative input / Comparator 1 positive input
-	-	46	PC7/LCD_SEG25(3)/ ADC1_IN3/USART3_CK/ COMP2_INM/ COMP1_INP	I/O	FT(5)	**X**	X	X	HS	X	X	**Port C7**	LCD segment 25 /ADC1_IN3/ USART3 synchronous clock/ Comparator 2 negative input / Comparator 1 positive input
29	25	20	PD0/TIM3_CH2/ *[ADC1_TRIG]*(2)/ LCD_SEG7(3)/ ADC1_IN22/COMP2_INP	I/O	FT(5)	**X**	X	X	HS	X	X	**Port D0**	Timer 3 - channel 2 / *[ADC1_Trigger]* / LCD segment 7 / ADC1_IN22 / Comparator 2 positive input 2
30	26	21	PD1/TIM3_ETR/ LCD_COM3(3)/ ADC1_IN21/COMP1_INP/ COMP2_INP	I/O	FT(5)	**X**	X	X	HS	X	X	**Port D1**	Timer 3 - trigger / LCD_COM3 / ADC1_IN21 / comparator 1 positive input/ comparator 2 positive input
31	27	22	PD2/TIM1_CH1 /LCD_SEG8(3)/ ADC1_IN20/COMP1_INP	I/O	FT(5)	**X**	X	X	HS	X	X	**Port D2**	Timer 1 - channel 1 / LCD segment 8 / ADC1_IN20/Comparator 1 positive input
32	28	23	PD3/ TIM1_ETR/ LCD_SEG9(3)/ ADC1_IN19/ COMP1_INP	I/O	FT(5)	**X**	X	X	HS	X	X	**Port D3**	Timer 1 - trigger / LCD segment 9 / ADC1_IN19/Comparator 1 positive input
57	45	-	PD4/TIM1_CH2 /LCD_SEG18(3)/ ADC1_IN10/ COMP1_INP	I/O	FT(5)	**X**	X	X	HS	X	X	**Port D4**	Timer 1 - channel 2 / LCD segment 18 / ADC1_IN10/Comparator 1 positive input
-	-	33	PD4/TIM1_CH2 /LCD_SEG18(3)/ ADC1_IN10/SPI2_MISO/ COMP1_INP	I/O	FT(5)	**X**	X	X	HS	X	X	**Port D4**	Timer 1 - channel 2 / LCD segment 18 / ADC1_IN10/SPI2 master in/slave out/Comparator 1 positive input

Table 5. High-density STM8AL3xE8x pin description (continued)

Pin number			Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP80	LQFP64	LQFP48				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
64	52	-	PG7/LCD_SEG35/ SPI2_MISO	I/O	FT(5)	**X**	X	X	HS	X	X	**Port G7**	LCD segment 35 / SPI2 master in- slave out
23	-	-	PE0/LCD_SEG1(3)/ TIM5_CH2	I/O	FT(5)	**X**	X	X	HS	X	X	**Port E0**	LCD segment 1 /Timer 5 channel 2
-	19	14	PE0/LCD_SEG1(3)/ TIM5_CH2/RTC_TAMP1	I/O	FT(5)	**X**	X	X	HS	X	X	**Port E0**	LCD segment 1 /Timer 5 channel 2 / RTC tamper 1
24	-	-	PE1/TIM1_CH2N /LCD_SEG2(3)	I/O	FT(5)	**X**	X	X	HS	X	X	**Port E1**	Timer 1 - inverted channel 2 / LCD segment 2
-	20	15	PE1/TIM1_CH2N /LCD_SEG2(3)/ RTC_TAMP2	I/O	FT(5)	**X**	X	X	HS	X	X	**Port E1**	Timer 1 - inverted channel 2 / LCD segment 2 / RTC tamper 2
25	-	-	PE2/TIM1_CH3N /LCD_SEG3(3)	I/O	FT(5)	**X**	X	X	HS	X	X	**Port E2**	Timer 1 - inverted channel 3 / LCD segment 3
-	21	16	PE2/TIM1_CH3N /LCD_SEG3(3)/ RTC_TAMP3	I/O	FT(5)	**X**	X	X	HS	X	X	**Port E2**	Timer 1 - inverted channel 3 / LCD segment 3 / RTC tamper 3
26	-	-	PE3/LCD_SEG4(3)	I/O	FT(5)	**X**	X	X	HS	X	X	**Port E3**	LCD segment 4
-	22	17	PE3/LCD_SEG4(3)/ USART2_RX	I/O	FT(5)	**X**	X	X	HS	X	X	**Port E3**	LCD segment 4/ USART2 receive
27	-	-	PE4/LCD_SEG5(3)/ DAC_TRIG1	I/O	FT(5)	**X**	X	X	HS	X	X	**Port E4**	LCD segment 5/ DAC 1 trigger
-	23	18	PE4/LCD_SEG5(3)/ DAC_TRIG2/USART2_TX	I/O	FT(5)	**X**	X	X	HS	X	X	**Port E4**	LCD segment 5/ DAC 2 trigger/ USART2 transmit
28	-	-	PE5/LCD_SEG6(3)/ ADC1_IN23/COMP1_INP/ COMP2_INP	I/O	FT(5)	**X**	X	X	HS	X	X	**Port E5**	LCD segment 6 / ADC1_IN23/Comparator 1 positive input/Comparator 2 positive input
-	24	19	PE5/LCD_SEG6(3)/ ADC1_IN23/COMP1_INP/ COMP2_INP/ USART2_CK	I/O	FT(5)	**X**	X	X	HS	X	X	**Port E5**	LCD segment 6 / ADC1_IN23/ Comparator 1 positive input/ Comparator 2 positive input/USART2 synchronous clock
-	-	47	PE6/LCD_SEG26(3)/ PVD_IN/TIM5_BKIN/ USART3_TX	I/O	FT(5)	**X**	X	X	HS	X	X	**Port E6**	LCD segment 26 /PVD_IN /TIM5 break input / USART3 transmit

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 53C8 to 0x00 53CF	Reserved area			
0x00 53D0	AES	AES_CR	AES control register	0x00
0x00 53D1		AES_SR	AES status register	0x00
0x00 53D2		AES_DINR	AES data input register	0x00
0x00 53D3		AES_DOUTR	AES data output register	0x00
0x00 53D4 to 0x00 53DF	Reserved area			
0x00 53E0	USART2	USART2_SR	USART2 status register	0xC0
0x00 53E1		USART2_DR	USART2 data register	0xXX
0x00 53E2		USART2_BRR1	USART2 baud rate register 1	0x00
0x00 53E3		USART2_BRR2	USART2 baud rate register 2	0x00
0x00 53E4		USART2_CR1	USART2 control register 1	0x00
0x00 53E5		USART2_CR2	USART2 control register 2	0x00
0x00 53E6		USART2_CR3	USART2 control register 3	0x00
0x00 53E7		USART2_CR4	USART2 control register 4	0x00
0x00 53E8		USART2_CR5	USART2 control register 5	0x00
0x00 53E9		USART2_GTR	USART2 guard time register	0x00
0x00 53EA		USART2_PSCR	USART2 prescaler register	0x00
0x00 53EB to 0x00 53EF	Reserved area			
0x00 53F0	USART3	USART3_SR	USART3 status register	0xC0
0x00 53F1		USART3_DR	USART3 data register	0xXX
0x00 53F2		USART3_BRR1	USART3 baud rate register 1	0x00
0x00 53F3		USART3_BRR2	USART3 baud rate register 2	0x00
0x00 53F4		USART3_CR1	USART3 control register 1	0x00
0x00 53F5		USART3_CR2	USART3 control register 2	0x00
0x00 53F6		USART3_CR3	USART3 control register 3	0x00
0x00 53F7		USART3_CR4	USART3 control register 4	0x00
0x00 53F8		USART3_CR5	USART3 control register 5	0x00
0x00 53F9		USART3_GTR	USART3 guard time register	0x00
0x00 53FA		USART3_PSCR	USART3 prescaler register	0x00
0x00 53FB to 0x00 53FF	Reserved area			

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5400	LCD	LCD_CR1	LCD control register 1	0x00
0x00 5401		LCD_CR2	LCD control register 2	0x00
0x00 5402		LCD_CR3	LCD control register 3	0x00
0x00 5403		LCD_FRQ	LCD frequency selection register	0x00
0x00 5404		LCD_PM0	LCD Port mask register 0	0x00
0x00 5405		LCD_PM1	LCD Port mask register 1	0x00
0x00 5406		LCD_PM2	LCD Port mask register 2	0x00
0x00 5407		LCD_PM3	LCD Port mask register 3	0x00
0x00 5408		LCD_PM4	LCD Port mask register 4	0x00
0x00 5409		LCD_PM5	LCD Port mask register 5	0x00
0x00 540A to 0x00 540B	Reserved area (2 byte)			
0x00 540C	LCD	LCD_RAM0	LCD display memory 0	0x00
0x00 540D		LCD_RAM1	LCD display memory 1	0x00
0x00 540E		LCD_RAM2	LCD display memory 2	0x00
0x00 540F		LCD_RAM3	LCD display memory 3	0x00
0x00 5410		LCD_RAM4	LCD display memory 4	0x00
0x00 5411		LCD_RAM5	LCD display memory 5	0x00
0x00 5412		LCD_RAM6	LCD display memory 6	0x00
0x00 5413		LCD_RAM7	LCD display memory 7	0x00
0x00 5414		LCD_RAM8	LCD display memory 8	0x00
0x00 5415		LCD_RAM9	LCD display memory 9	0x00
0x00 5416		LCD_RAM10	LCD display memory 10	0x00
0x00 5417		LCD_RAM11	LCD display memory 11	0x00
0x00 5418		LCD_RAM12	LCD display memory 12	0x00
0x00 5419		LCD_RAM13	LCD display memory 13	0x00
0x00 541A		LCD_RAM14	LCD display memory 14	0x00
0x00 541B		LCD_RAM15	LCD display memory 15	0x00
0x00 541C		LCD_RAM16	LCD display memory 16	0x00
0x00 541D		LCD_RAM17	LCD display memory 17	0x00
0x00 541E		LCD_RAM18	LCD display memory 18	0x00
0x00 541F		LCD_RAM19	LCD display memory 19	0x00
0x00 5420		LCD_RAM20	LCD display memory 20	0x00
0x00 5421		LCD_RAM21	LCD display memory 21	0x00

7 Option byte

Option byte contain configurations for device hardware features as well as the memory protection of the device. They are stored in a dedicated memory block.

All option byte can be modified in ICP mode (with SWIM) by accessing the EEPROM address. See *Table 12* for details on option byte addresses.

The option byte can also be modified 'on the fly' by the application in IAP mode, except for the ROP, UBC and PCODESIZE values which are only taken into account when they are modified in ICP mode (with the SWIM).

Refer to the STM8AL31E8x/STM8AL3LE8x Flash programming manual (PM0054) and STM8 SWIM and Debug Manual (UM0470) for information on SWIM programming procedures.

Table 12. Option byte addresses

Address	Option name	Option byte No.	Option bits								Factory default setting
			7	6	5	4	3	2	1	0	
00 4800	Read-out protection (ROP)	OPT0	ROP[7:0]								0xAA
00 4802	UBC (User Boot code size)	OPT1	UBC[7:0]								0x00
00 4807	PCODESIZE	OPT2	PCODE[7:0]								0x00
00 4808	Independent watchdog option	OPT3 [3:0]	Reserved				WWDG _HALT	WWDG _HW	IWDG _HALT	IWDG _HW	0x00
00 4809	Number of stabilization clock cycles for HSE and LSE oscillators	OPT4	Reserved				LSECNT[1:0]		HSECNT[1:0]		0x00
00 480A	Brownout reset (BOR)	OPT5 [3:0]	Reserved				BOR_TH			BOR_ ON	0x01
00 480B	Bootloader option byte (OPTBL)	OPTBL [15:0]	OPTBL[15:0]								0x00
00 480C											0x00

8 Unique ID

STM8 devices feature a 96-bit unique device identifier which provides a reference number that is unique for any device and in any context. The 96 bits of the identifier are never altered by the user.

The unique device identifier is read in single byte and may then be concatenated using a custom algorithm.

The unique device identifier is ideally suited:

- For use as serial numbers
- For use as security keys to increase the code security in the program memory while using and combining this unique ID with software cryptographic primitives and protocols before programming the internal memory.
- To activate secure boot processes

Table 14. Unique ID registers (96 bits)

Address	Content description	Unique ID bits							
		7	6	5	4	3	2	1	0
0x4926	X co-ordinate on the wafer	U_ID[7:0]							
0x4927		U_ID[15:8]							
0x4928	Y co-ordinate on the wafer	U_ID[23:16]							
0x4929		U_ID[31:24]							
0x492A	Wafer number	U_ID[39:32]							
0x492B	Lot number	U_ID[47:40]							
0x492C		U_ID[55:48]							
0x492D		U_ID[63:56]							
0x492E		U_ID[71:64]							
0x492F		U_ID[79:72]							
0x4930		U_ID[87:80]							
0x4931		U_ID[95:88]							

9.3 Operating conditions

Subject to general operating conditions for V_{DD} and T_A.

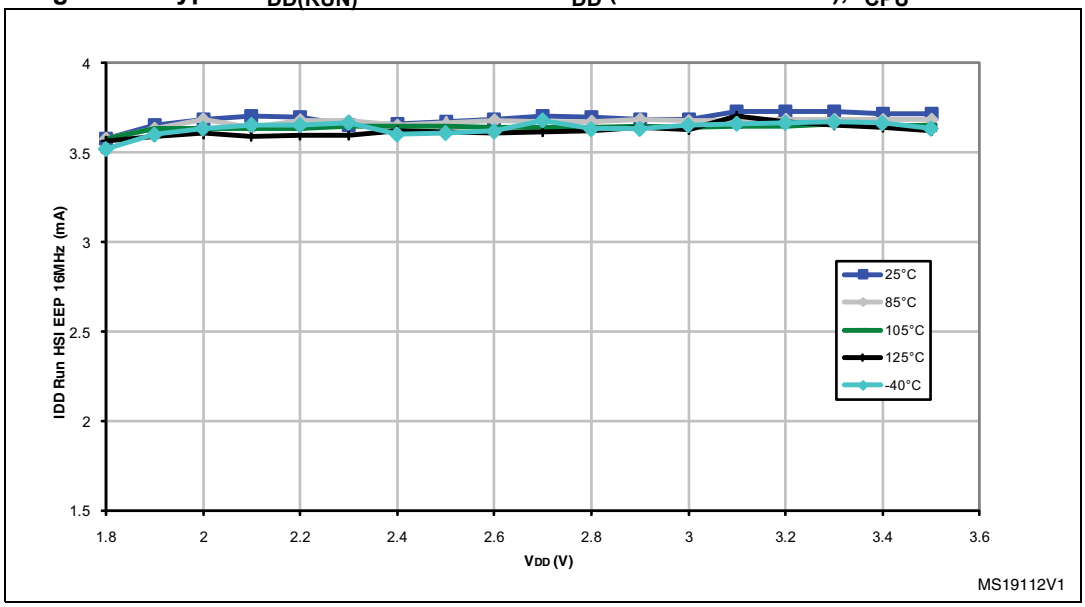
9.3.1 General operating conditions

Table 19. General operating conditions

Symbol	Parameter	Conditions		Min.	Max.	Unit
f_{SYSCLK}(1)	System clock frequency	1.65 V ≤V_{DD} < 3.6 V		0	16	MHz
V_{DD}	Standard operating voltage	BOR detector enabled		1.65(2)	3.6	V
V_{DDA}	Analog operating voltage	ADC and DAC not used	Must be at the same potential as V_{DD}	1.65(2)	3.6	V
		ADC or DAC used		1.8	3.6	V
P_D(3)	Power dissipation at T_A= 85 °C for suffix A devices	LQFP80	-	-	288	mW
		LQFP64	-	-	288	
		LQFP48	-	-	288	
	Power dissipation at T_A= 125 °C for suffix C devices	LQFP80	-	-	131	
		LQFP64	-	-	104	
		LQFP48	-	-	77	
T_A	Temperature range	1.65 V ≤V_{DD} < 3.6 V (A suffix version)	-	-40	85	°C
		1.65 V ≤V_{DD} < 3.6 V (C suffix version)	-	-40	125	
T_J	Junction temperature range	-40 °C ≤T_A < 85 °C (A suffix version)		-40	105	
		-40 °C≤ T_A < 125 °C (C suffix version)		-40	130	

1. $f_{SYSCLK} = f_{CPU}$
2. 1.8 V at power-up, 1.65 V at power-down if BOR is disabled.
3. To calculate $P_{Dmax}(T_A)$, use the formula $P_{Dmax}=(T_{Jmax} - T_A)/\Theta_{JA}$ with T_{Jmax} in this table and Θ_{JA} in “Thermal characteristics” table.

Figure 14. Typical $I_{DD(RUN)}$ from Flash vs. V_{DD} (HSI clock source), f_{CPU} = 16 MHz(1)



1. Typical current consumption measured with code executed from Flash.

In the following table, data are based on characterization results, unless otherwise specified.

Table 22. Total current consumption in Wait mode

Symbol	Parameter	Conditions[1]			Typ	Max	Unit
$I_{DD(Wait)}$	Supply current in Wait mode	CPU not clocked, all peripherals OFF, code executed from RAM with Flash in I_{DDQ} mode,[2] V_{DD} from 1.65 V to 3.6 V	HSI	f_{CPU} = 125 kHz	0.35	0.45[4]	mA
				f_{CPU} = 1 MHz	0.35	0.50[4]	
				f_{CPU} = 4 MHz	0.40	0.60[4]	
				f_{CPU} = 8 MHz	0.50	0.60[4]	
				f_{CPU} = 16 MHz	0.70	0.85	
			HSE external clock (f_{CPU}=f_{HSE})[3]	f_{CPU} = 125 kHz	0.05	0.10[4]	
				f_{CPU} = 1 MHz	0.10	0.20[4]	
				f_{CPU} = 4 MHz	0.20	0.40[4]	
				f_{CPU} = 8 MHz	0.40	0.65[4]	
				f_{CPU} = 16 MHz	0.76	1.15[4]	
			LSI	f_{CPU} = f_{LSI}	60	80[4]	µA
			LSE[5] external clock (32.768 kHz)	f_{CPU} = f_{LSE}	50	70[4]	
$I_{DD(Wait)}$	Supply current in Wait mode	CPU not clocked, all peripherals OFF, code executed from Flash, V_{DD} from 1.65 V to 3.6 V	HSI	f_{CPU} = 125 kHz	0.38	0.55[4]	mA
				f_{CPU} = 1 MHz	0.40	0.60[4]	
				f_{CPU} = 4 MHz	0.50	0.65[4]	
				f_{CPU} = 8 MHz	0.60	0.75[4]	
				f_{CPU} = 16 MHz	0.80	0.90	
			HSE[3] external clock (f_{CPU}= HSE)	f_{CPU} = 125 kHz	0.07	0.15[4]	
				f_{CPU} = 1 MHz	0.10	0.20[4]	
				f_{CPU} = 4 MHz	0.25	0.45[4]	
				f_{CPU} = 8 MHz	0.50	0.65[4]	
				f_{CPU} = 16 MHz	1.00	1.20[4]	
			LSI	f_{CPU} = f_{LSI}	50	100[4]	µA
			LSE[5] external clock (32.768 kHz)	f_{CPU} = f_{LSE}	50	80[4]	

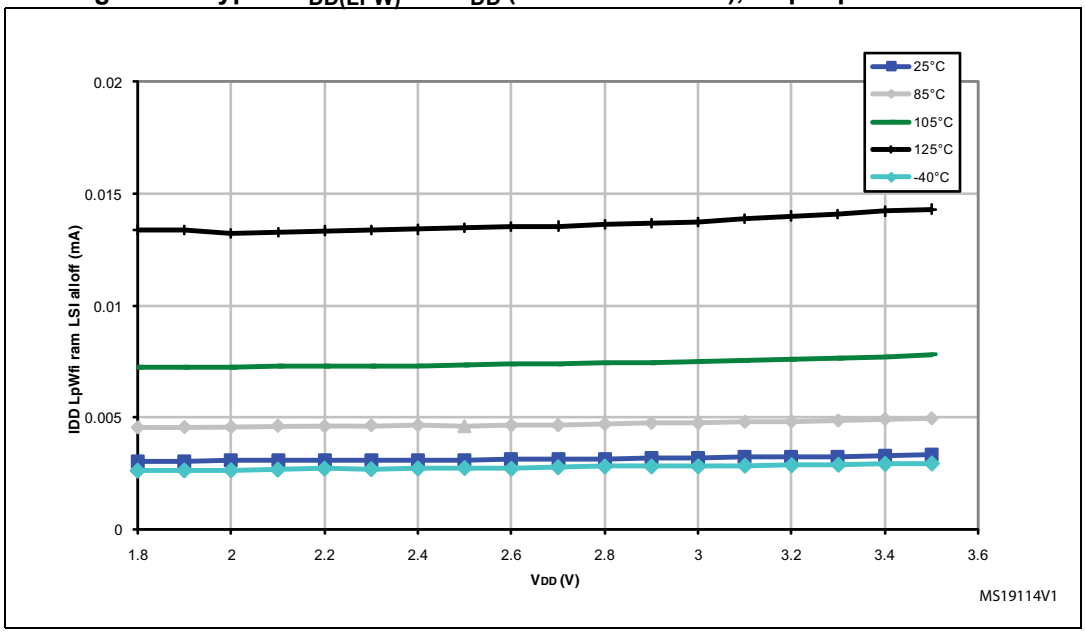
1. All peripherals OFF, V_{DD} from 1.65 V to 3.6 V, HSI internal RC osc., f_{CPU} = f_{SYSCLK}
2. Flash is configured in I_{DDQ} mode in Wait mode by setting the EPM or WAITM bit in the Flash_CR1 register.
3. Oscillator bypassed (HSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the HSE consumption ($I_{DD\ HSE}$) must be added. Refer to *Table 32*.
4. Guaranteed by characterization results.
5. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ HSE}$) must be added. Refer to *Table 33*

Table 24. Total current consumption in low-power wait mode at V_{DD} = 1.65 V to 3.6 V

Symbol	Parameter	Conditions(1)			Typ.	Max.	Unit
$I_{DD(LPW)}$	Supply current in low-power wait mode	LSI RC osc. (at 38 kHz)	all peripherals OFF	T_A = -40 °C to 25 °C	3.00	3.30(2)	µA
				T_A = 85 °C	4.40	9.00(3)	
				T_A = 125 °C	11.00	18.00(3)	
		LSE external clock(4) (32.768 kHz)		T_A = -40 °C to 25 °C	2.35	2.70(2)	
				T_A = 85 °C	3.10	3.70(2)	
				T_A = 125 °C	12.0	14.0(2)	

1. No floating I/Os.
2. Guaranteed by characterization results.
3. Tested at 85°C for temperature range A or 125°C for temperature range C.
4. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ LSE}$) must be added. Refer to *Table 33*.

Figure 18. Typical $I_{DD(LPW)}$ vs. V_{DD} (LSI clock source), all peripherals OFF(1)



1. Typical current consumption measured with code executed from RAM.

Table 25. Total current consumption and timing in Active-halt mode at V_{DD} = 1.65 V to 3.6 V (continued)

Symbol	Parameter	Conditions(1)			Typ.	Max.(2)	Unit
$t_{WU\_HSI(AH)}$(9)(10)	Wakeup time from Active-halt mode to Run mode (using HSI)	-	-	-	4.70	7.00	µs
$t_{WU\_LSI(AH)}$(9)(10)	Wakeup time from Active-halt mode to Run mode (using LSI)	-	-	-	150.0	-	µs

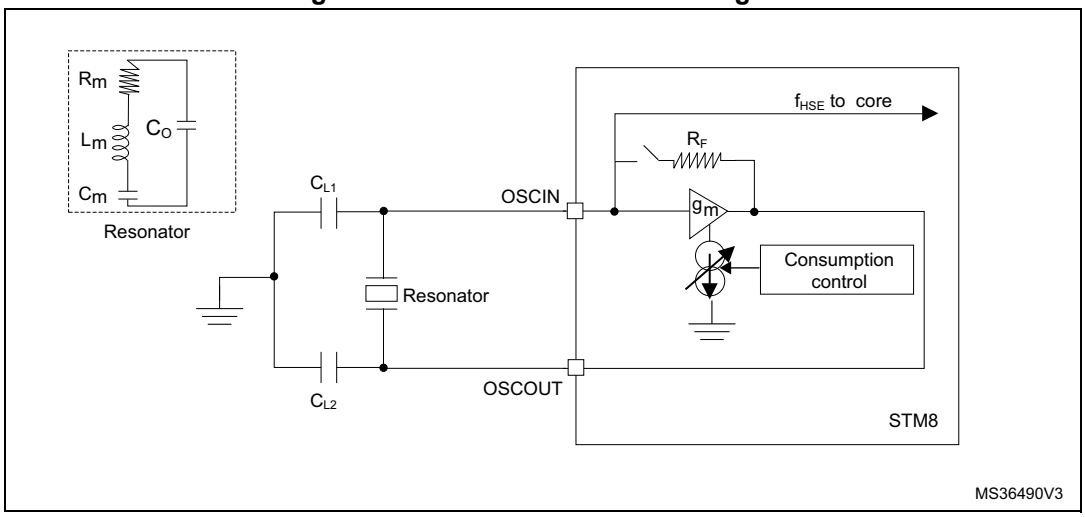
1. No floating I/O, unless otherwise specified.
2. Guaranteed by characterization results.
3. RTC enabled. Clock source = LSI
4. RTC enabled, LCD enabled with external V_{LCD} = 3 V, static duty, division ratio = 256, all pixels active, no LCD connected.
5. RTC enabled, LCD enabled with external V_{LCD}, 1/4 duty, 1/3 bias, division ratio = 64, all pixels active, no LCD connected.
6. LCD enabled with internal LCD booster V_{LCD} = 3 V, 1/4 duty, 1/3 bias, division ratio = 64, all pixels active, no LCD connected.
7. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ LSE}$) must be added. Refer to *Table 33*
8. RTC enabled. Clock source = LSE
9. Wakeup time until start of interrupt vector fetch.
   The first word of interrupt routine is fetched 4 CPU cycles after t_{WU}.
10. ULP=0 or ULP=1 and FWU=1 in the PWR_CSR2 register.

Table 26. Typical current consumption in Active-halt mode, RTC clocked by LSE external crystal

Symbol	Parameter	Condition(1)		Typ.	Unit
$I_{DD(AH)}$ (2)	Supply current in Active-halt mode	V_{DD} = 1.8 V	LSE	1.15	µA
			LSE/32(3)	1.05	
		V_{DD} = 3 V	LSE	1.30	
			LSE/32(3)	1.20	
		V_{DD} = 3.6 V	LSE	1.45	
			LSE/32(3)	1.35	

1. No floating I/O, unless otherwise specified.
2. Based on measurements on bench with 32.768 kHz external crystal oscillator.
3. RTC clock is LSE divided by 32.

Figure 21. HSE oscillator circuit diagram



HSE oscillator critical g_m formula

$$g_{mcrit} = (2 \times \Pi \times f_{HSE})^2 \times R_m(2Co + C)^2$$

R_m: Motional resistance (see crystal specification), L_m: Motional inductance (see crystal specification), C_m: Motional capacitance (see crystal specification), Co: Shunt capacitance (see crystal specification), C_{L1}=C_{L2}=C: Grounded external capacitance

$g_m >> g_{mcrit}$

LSE crystal/ceramic resonator oscillator

The LSE is available on STM8AL31E8x devices only.

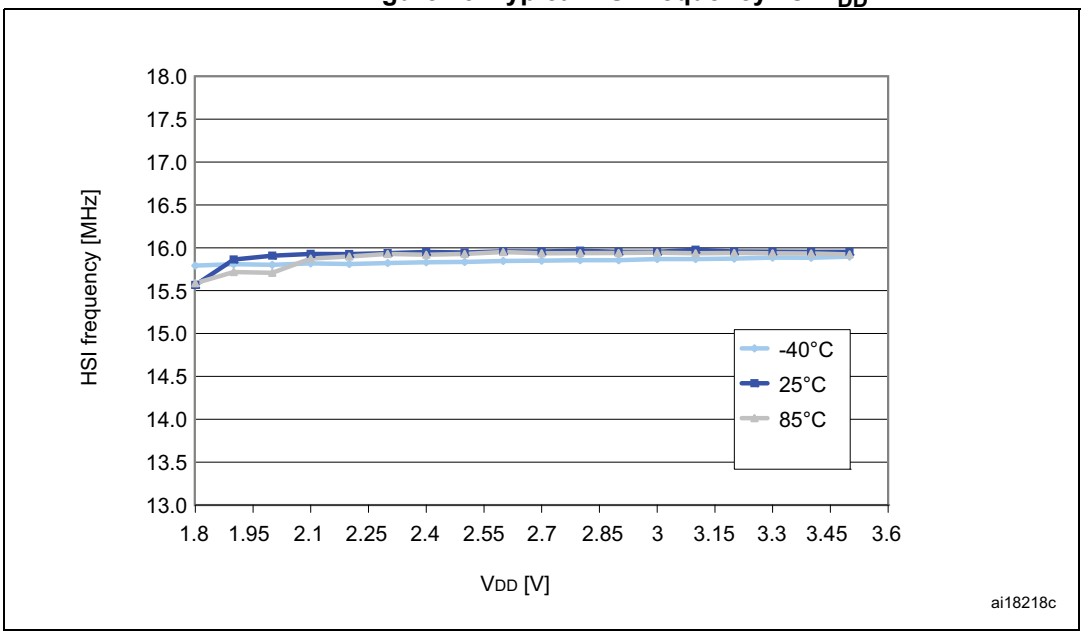
The LSE clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

Table 34. HSI oscillator characteristics

Symbol	Parameter	Conditions(1)	Min.	Typ.	Max.	Unit
f_{HSI}	Frequency	V_{DD} = 3.0 V	-	16	-	MHz
ACC_{HSI}	HSI oscillator user trimming accuracy	Trimmed by the application for any V_{DD} and T_A conditions	-1	-	1	%
	HSI oscillator accuracy (factory calibrated)	V_{DD} ≤1.8 V≤ V_{DD} ≤ 3.6 V -40 °C ≤T_A ≤ 125 °C	-5	-	5	
TRIM	HSI user trimming step(2)	Trimming code ≠ multiple of 16	-	0.4	0.7(2)	%
		Trimming code = multiple of 16	-	-	± 1.5(2)	
$t_{su(HSI)}$	HSI oscillator setup time (wakeup time)	-	-	3.7	6 (3)	µs
$I_{DD(HSI)}$	HSI oscillator power consumption	-	-	100	140(3)	µA

1. V_{DD} = 3.0 V, T_A = -40 to 125 °C unless otherwise specified.
2. The trimming step differs depending on the trimming code. It is usually negative on the codes which are multiples of 16 (0x00, 0x10, 0x20, 0x30...0xE0). Refer to the AN3101 “STM8L15x internal RC oscillator calibration” application note for more details.
3. Guaranteed by design.

Figure 23. Typical HSI frequency vs. V_{DD}



Low speed internal RC oscillator (LSI)

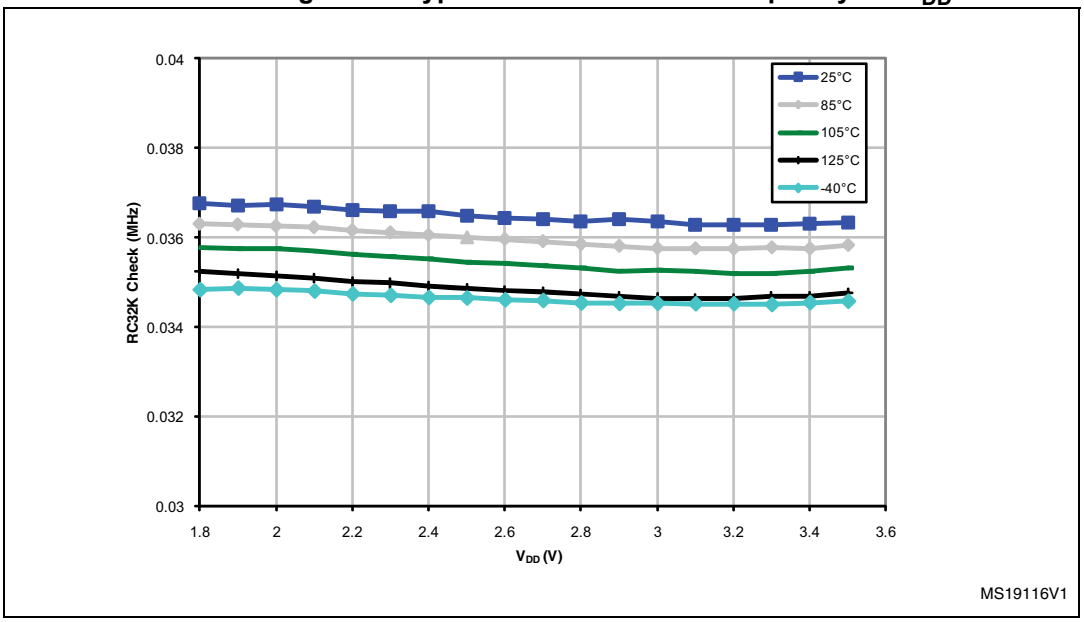
In the following table, data are based on characterization results, not tested in production, unless otherwise specified.

Table 35. LSI oscillator characteristics

Symbol	Parameter	Conditions(1)	Min.	Typ.	Max.	Unit
f_{LSI}	Frequency	-	26	38	56	kHz
$t_{su(LSI)}$	LSI oscillator wakeup time	-	-	-	200(2)	µs
$D_{(LSI)}$	LSI oscillator frequency drift(3)	0 °C ≤T_A ≤85 °C	-12	-	11	%

1. V_{DD} = 1.65 V to 3.6 V, T_A = -40 to 125 °C unless otherwise specified.
2. Guaranteed by design.
3. This is a deviation for an individual part, once the initial frequency has been measured.

Figure 24. Typical LSI clock source frequency vs. V_{DD}



9.3.5 Memory characteristics

T_A = -40 to 125 °C unless otherwise specified.

Table 36. RAM and hardware registers

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{RM}	Data retention mode (1)	Halt mode (or Reset)	1.65	-	-	V

1. Minimum supply voltage without losing data stored in RAM (in Halt mode or under Reset) or in hardware registers (only in Halt mode). Guaranteed by characterization results.

9.3.6 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error, out of spec current injection on adjacent pins or other functional failure (for example reset, oscillator frequency deviation, LCD levels, etc.).

The test results are given in the following table.

Table 40. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on true open-drain pins	-5	+0	mA
	Injected current on all 5 V tolerant (FT) pins	-5	+0	
	Injected current on any other pin	-5	+5	

9.3.7 I/O port pin characteristics

General characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified. All unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor.

NRST pin

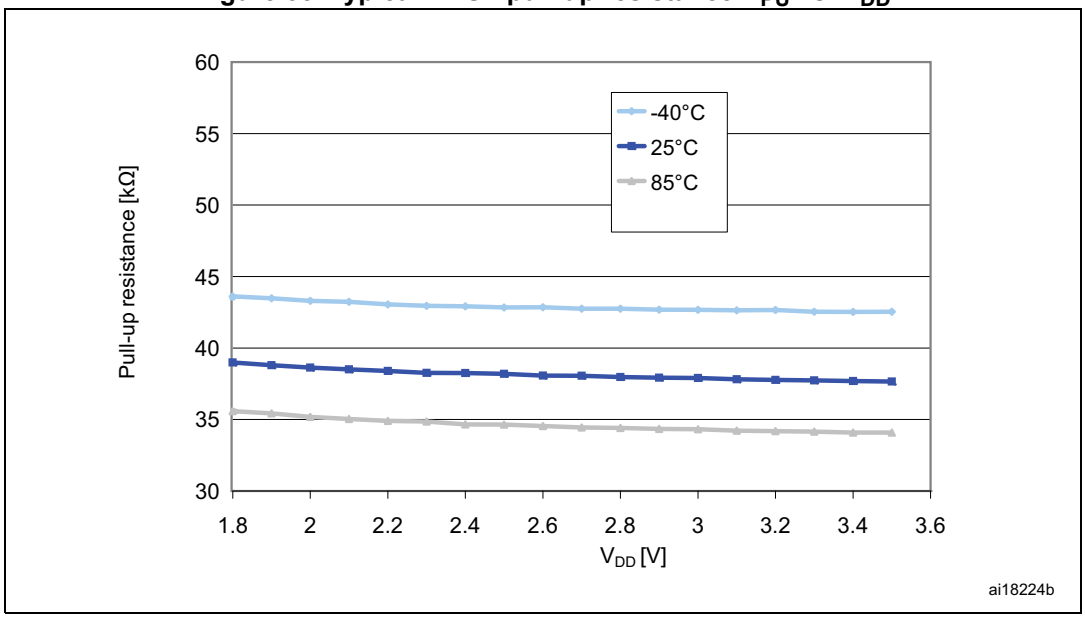
Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 45. $\overline{\text{NRST}}$ pin characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{IL(NRST)}$	NRST input low-level voltage	-	V_{SS}(1)	-	0.8(1)	V
$V_{IH(NRST)}$	NRST input high-level voltage (1)	-	1.4(1)	-	V_{DD}(1)	
$V_{OL(NRST)}$	NRST output low-level voltage (1)	I_{OL} = 2 mA for 2.7 V ≤V_{DD} ≤3.6 V	-	-	0.4(1)	
		I_{OL} = 1.5 mA for V_{DD} < 2.7 V	-	-		
V_{HYST}	NRST input hysteresis	-	10%V_{DD} (2)(3)	-	-	mV
$R_{PU(NRST)}$	NRST pull-up equivalent resistor	-	30(1)	45	60(1)	kΩ
$V_{F(NRST)}$	NRST input filtered pulse	-	-	-	50(3)	ns
$V_{NF(NRST)}$	NRST input not filtered pulse	-	300(3)	-	-	

1. Guaranteed by characterization results.
2. 200 mV min.
3. Guaranteed by design.

Figure 35. Typical NRST pull-up resistance R_{PU} vs. V_{DD}



9.3.10 Embedded reference voltage

In the following table, data are based on characterization results, not tested in production, unless otherwise specified.

Table 49. Reference voltage characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{REFINT}	Internal reference voltage consumption	-	-	1.4	-	µA
$T_{S\_VREFINT}$(1)(2)	ADC sampling time when reading the internal reference voltage	-	-	5	10	µs
I_{BUF}(1)	Internal reference voltage buffer consumption (used for ADC)	-	-	13.5	25	µA
$V_{REFINT\ out}$	Reference voltage output	-	1.202 (3)	1.224	1.242 (3)	V
I_{LPBUF}(1)	Internal reference voltage low-power buffer consumption (used for comparators or output)	-	-	730	1200	nA
I_{REFOUT}(1)(4)	Buffer output current	-	-	-	1	µA
C_{REFOUT}	Reference voltage output load	-	-	-	50	pF
$t_{VREFINT}$(1)	Internal reference voltage startup time	-	-	2	3	ms
t_{BUFEN}(1)(2)	Internal reference voltage buffer startup time once enabled	-	-	-	10	µs
$ACC_{VREFINT}$(5)	Accuracy of V_{REFINT} stored in the VREFINT_Factory_CONV byte	-	-	-	± 5	mV
$STAB_{VREFINT}$	Stability of V_{REFINT} over temperature	-40 °C ≤T_A ≤ 125 °C	-	20	50	ppm/°C
	Stability of V_{REFINT} over temperature	0 °C ≤T_A ≤ 50 °C	-	-	20	ppm/°C
$STAB_{VREFINT}$	Stability of V_{REFINT} after 1000 hours	-	-	-	TBD	ppm

1. Guaranteed by design.
2. Defined when ADC output reaches its final value ±1/2LSB
3. Tested in production at V_{DD} = 3 V ±10 mV.
4. To guarantee less than 1% V_{REFOUT} deviation
5. Measured at V_{DD} = 3 V ±10 mV. This value takes into account V_{DD} accuracy and ADC conversion accuracy.