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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	C28x
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, I²C, McBSP, SCI, SPI, uPP, UART/USART, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	97
Program Memory Size	1MB (512K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	82K x 16
Voltage - Supply (Vcc/Vdd)	1.14V ~ 3.47V
Data Converters	A/D 20x12b, 20x16b; D/A 3x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TJ)
Mounting Type	Surface Mount
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-HLQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/texas-instruments/tms320f28377sptps

2 Description

The high-density STM8AL3xE8x ultra-low-power devices feature an enhanced STM8 CPU core providing increased processing power (up to 16 MIPS at 16 MHz) while maintaining the advantages of a CISC architecture with improved code density, a 24-bit linear addressing space and an optimized architecture for low-power operations.

The family includes an integrated debug module with a hardware interface (SWIM) which allows non-intrusive in-application debugging and ultrafast Flash programming.

All high-density STM8AL3xE8x microcontrollers feature embedded data EEPROM and low-power low-voltage single-supply program Flash memory.

The devices incorporate an extensive range of enhanced I/Os and peripherals, a 12-bit ADC, two DACs, two comparators, a real-time clock, AES, 8x40 or 4x44-segment LCD, four 16-bit timers, one 8-bit timer, as well as standard communication interfaces such as two SPIs, an I^2C interface, and three USARTs. One 8x40 or 4x44-segment LCD is available on the STM8AL3LE8x devices. The modular design of the peripheral set allows the same peripherals to be found in different ST microcontroller families including 32-bit families. This makes any transition to a different family very easy, and simplified even more by the use of a common set of development tools.

2.1 STM8AL ultra-low-power 8-bit family benefits

High-density STM8AL3xE8x devices are part of the STM8AL automotive ultra-low-power 8-bit family providing the following benefits:

- Integrated system
  - 64 Kbytes of high-density embedded Flash program memory
  - 2 Kbytes of data EEPROM
  - 4 Kbytes of RAM
  - Internal high-speed and low-power low speed RC.
  - Embedded reset
- Ultra-low-power consumption
  - 1 µA in Active-halt mode
  - Clock gated system and optimized power management
  - Capability to execute from RAM for Low-power wait mode and Low-power run mode
- Advanced features
  - Up to 16 MIPS at 16 MHz CPU clock frequency
  - Direct memory access (DMA) for memory-to-memory or peripheral-to-memory access.
- Short development cycles
  - Application scalability across a common family product architecture with compatible pinout, memory map and modular peripherals.
  - Wide choice of development tools

BOR: Brownout reset
DMA: Direct memory access
DAC: Digital-to-analog converter
I²C: Inter-integrated circuit multimaster interface
IWDG: Independent watchdog
LCD: Liquid crystal display
POR/PDR: Power on reset / power-down reset
RTC: Real-time clock
SPI: Serial peripheral interface
SWIM: Single wire interface module
USART: Universal synchronous asynchronous receiver transmitter
WWDG: Window watchdog

3.1 Low-power modes

The high-density STM8AL3xE8x devices support five low-power modes to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- **Wait mode**: CPU clock is stopped, but selected peripherals keep running. An internal or external interrupt or a Reset is used to exit the microcontroller from Wait mode (WFE or WFI mode).
- **Low-power run mode**: The CPU and the selected peripherals are running. Execution is done from RAM with a low speed oscillator (LSI or LSE). Flash memory and data EEPROM are stopped and the voltage regulator is configured in ultra-low-power mode. The microcontroller enters Low-power run mode by software and exits from this mode by software or by a reset.
  All interrupts must be masked and are not used to exit the microcontroller from this mode.
- **Low-power wait mode:** This mode is entered when executing a Wait for event in Low-power run mode. It is similar to Low-power run mode except that the CPU clock is stopped. The wakeup from this mode is triggered by a Reset or by an internal or external event (peripheral event generated by the timers, serial interfaces, DMA controller (DMA1), comparators and I/O ports). When the wakeup is triggered by an event, the system goes back to Low-power run mode.
  All interrupts must be masked and arenot used to exit the microcontroller from this mode.
- **Active-halt mode**: CPU and peripheral clocks are stopped, except RTC. The wakeup is triggered by RTC interrupts, external interrupts or reset.
- **Halt mode**: CPU and peripheral clocks are stopped, the device remains powered on. The RAM content is preserved. The wakeup is triggered by an external interrupt or reset. A few peripherals have also a wakeup from Halt capability. Switching off the internal reference voltage reduces power consumption. Through software configuration it is also possible to wake up the device without waiting for the internal reference voltage wakeup time to have a fast wakeup time of 5 µs.

3.3.3 Voltage regulator

The high-density STM8AL3xE8x devices embed an internal voltage regulator for generating the 1.8 V power supply for the core and peripherals.

This regulator has two different modes:

- Main voltage regulator mode (MVR) for Run, Wait for interrupt (WFI) and Wait for event (WFE) modes.
- Low-power voltage regulator mode (LPVR) for Halt, Active-halt, Low-power run and Low-power wait modes.

When entering Halt or Active-halt modes, the system automatically switches from the MVR to the LPVR in order to reduce current consumption.

3.4 Clock management

The clock controller distributes the system clock (SYSCLK) coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness.

Features

- **Clock prescaler:** to get the best compromise between speed and current consumption, the clock frequency to the CPU and peripherals has to be adjusted by a programmable prescaler
- **Safe clock switching:** Clock sources are adaptable safely on the fly in run mode through a configuration register.
- **Clock management:** To reduce power consumption, the clock controller stops the clock to the core, individual peripherals or memory.
- **System clock sources:** 4 different clock sources are available to drive the system clock:
  - 1-16 MHz High speed external crystal (HSE)
  - 16 MHz High speed internal RC oscillator (HSI)
  - 32.768 Low speed external crystal (LSE)
  - 38 kHz Low speed internal RC (LSI)
- **RTC and LCD clock sources:** the above four sources are available to clock the RTC and the LCD, whatever the system clock.
- **Startup clock:** After reset, the microcontroller restarts by default with an internal 2 MHz clock (HSI/8). The prescaler ratio and clock source is adjustable by the application program as soon as the code execution starts.
- **Clock security system (CSS):** This feature is enabled by software. If a HSE clock failure occurs, the system clock is automatically switched to HSI.
- **Configurable main clock output (CCO):** This outputs an external clock for use by the application.

3.6 LCD (Liquid crystal display)

The LCD is only available on STM8AL3LE8x devices.

The liquid crystal display drives up to 8 common terminals and up to 40 segment terminals to drive up to 320 pixels. This LCD is configurable to drive up to 4 common and 44 segments (up to 176 pixels).

- Internal step-up converter to guarantee contrast control whatever V_{DD}.
- Static 1/2, 1/3, 1/4, 1/8 duty supported.
- Static 1/2, 1/3, 1/4 bias supported.
- Phase inversion to reduce power consumption and EMI.
- Up to 8 pixels programmable to blink.
- The LCD controller operating in Halt mode.

Note: Unnecessary segments and common pins can be used as general I/O pins.

3.7 Memories

The high-density STM8AL3xE8x devices have the following main features:

- 4 Kbytes of RAM
- The non-volatile memory is divided into three arrays:
  - 64 Kbytes of medium-density embedded Flash program memory
  - 2 Kbytes of Data EEPROM
  - Option byte.

The memory supports the read-while-write (RWW): it is possible to execute the code from the program matrix while programming/erasing the data matrix.

The option byte protects part of the Flash program memory from write and readout piracy.

3.8 DMA

A 4-channel direct memory access controller (DMA1) offers a memory-to-memory and peripherals-from/to-memory transfer capability. The 4 channels are shared between the following IPs with DMA capability: ADC1, DAC1,DAC2, AES, I2C1, SPI1, SPI2, USART1, USART2, USART3, and the 5 Timers.

Table 5. High-density STM8AL3xE8x pin description (continued)

Pin number			Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP80	LQFP64	LQFP48				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
53	41	-	PF4/LCD_COM4	I/O	FT(5)	**X**	X	X	HS	X	X	**Port F4**	LCD COM4
54	42	-	PF5/LCD_COM5	I/O	FT(5)	**X**	X	X	HS	X	X	**Port F5**	LCD COM5
55	43	-	PF6/LCD_COM6	I/O	FT(5)	**X**	X	X	HS	X	X	**Port F6**	LCD COM6
56	44	-	PF7/LCD_COM7	I/O	FT(5)	**X**	X	X	HS	X	X	**Port F7**	LCD COM7
22	18	13	VLCD(7)	S	-	**-**	-	-	-	-	-	LCD booster external capacitor	
15	11	10	V_{DD1}	S	-	**-**	-	-	-	-	-	Digital power supply	
14	10	-	V_{SS1}	-	-	**-**	-	-	-	-	-	I/O ground	
16	12	11	V_{DDA}	S	-	**-**	-	-	-	-	-	Analog supply voltage	
17	13	12	V_{REF+}/V_{REF+_DAC}	S	-	**-**	-	-	-	-	-	ADC1 and DAC1/2 positive voltage reference	
18	14	-	PG0/LCD SEG 28(3)/USART3_RX/ *[TIM2_BKIN]*	I/O	FT(5)	**X**	X	X	HS	X	X	**Port G0**	LCD segment 28/ USART3 receive / *[Timer 2 - break input]*
19	15	-	PG1/LCD SEG 29(3)/USART3_TX/ *[TIM3_BKIN]*	I/O	FT(5)	**X**	X	X	HS	X	X	**Port G1**	LCD segment 29/ USART3 transmit / *[Timer 3 -break input]*
20	16	-	PG2/LCD_SEG 30(3)/ USART3_CK	I/O	FT(5)	**X**	X	X	HS	X	X	**Port G2**	LCD segment 30/ USART 3 synchronous clock
21	17	-	PG3/LCD SEG 31 (3)/ *[TIM3_ETR]*	I/O	FT(5)	**X**	X	X	HS	X	X	**Port G3**	LCD segment 31/ *[Timer 3 - trigger]*
33	-	-	PH4/USART2_RX	I/O	FT(5)	**X**	X	X	HS	X	X	**Port H4**	USART2 receive
34	-	-	PH5/USART2_TX	I/O	FT(5)	**X**	X	X	HS	X	X	**Port H5**	USART2 transmit
35	-	-	PH6/USART2_CK/ TIM5_CH1	I/O	FT(5)	**X**	X	X	HS	X	X	**Port H6**	USART2 synchronous clock/ Timer 5 - channel 1
36	-	-	PH7/TIM5_CH2	I/O	FT(5)	**X**	X	X	HS	X	X	**Port H7**	Timer 5 - channel 2
-	-	9	$V_{SS}/V_{SSA}/V_{REF-}$	S	-	-	-	-	-	-	-	I/O ground / Analog ground voltage / ADC1 negative voltage reference	
13	9	-	V_{SSA}/V_{REF-}	S	-	-	-	-	-	-	-	Analog ground voltage / ADC1 negative voltage reference	
37	29	-	V_{DD3}	S	-	-	-	-	-	-	-	IOs supply voltage	
38	30	-	V_{SS3}	S	-	-	-	-	-	-	-	IOs ground voltage	

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5386 to 0x00 5387	Reserved area (2 byte)			
0x00 5388	DAC	DAC_CH1RDHRH	DAC channel 1 right aligned data holding register high	0x00
0x00 5389		DAC_CH1RDHRL	DAC channel 1 right aligned data holding register low	0x00
0x00 538A to 0x00 538B	Reserved area (2 byte)			
0x00 538C	DAC	DAC_CH1LDHRH	DAC channel 1 left aligned data holding register high	0x00
0x00 538D		DAC_CH1LDHRL	DAC channel 1 left aligned data holding register low	0x00
0x00 538E to 0x00 538F	Reserved area (2 byte)			
0x00 5390	DAC	DAC_CH1DHR8	DAC channel 1 8-bit data holding register	0x00
0x00 5391 to 0x00 5393	Reserved area (3 byte)			
0x00 5394	DAC	DAC_CH2RDHRH	DAC channel 2 right aligned data holding register high	0x00
0x00 5395		DAC_CH2RDHRL	DAC channel 2 right aligned data holding register low	0x00
0x00 5396 to 0x00 5397	Reserved area (2 byte)			
0x00 5398	DAC	DAC_CH2LDHRH	DAC channel 2 left aligned data holding register high	0x00
0x00 5399		DAC_CH2LDHRL	DAC channel 2 left aligned data holding register low	0x00
0x00 539A to 0x00 539B	Reserved area (2 byte)			
0x00 539C	DAC	DAC_CH2DHR8	DAC channel 2 8-bit data holding register	0x00
0x00 539D to 0x00 539F	Reserved area (3 byte)			
0x00 53A0	DAC	DAC_DCH1RDHRH	DAC channel 1 right aligned data holding register high	0x00
0x00 53A1		DAC_DCH1RDHRL	DAC channel 1 right aligned data holding register low	0x00
0x00 53A2 to 0x00 53AB	Reserved area (3 byte)			

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 53AC	DAC	DAC_DORH	DAC data output register high	0x00
0x00 53AD		DAC_DORL	DAC data output register low	0x00
0x00 53A2		DAC_DCH2RDHRH	DAC channel 2 right aligned data holding register high	0x00
0x00 53A3		DAC_DCH2RDHRL	DAC channel 2 right aligned data holding register low	0x00
0x00 53A4		DAC_DCH1LDHRH	DAC channel 1left aligned data holding register high	0x00
0x00 53A5		DAC_DCH1LDHRL	DAC channel 1left aligned data holding register low	0x00
0x00 53A6		DAC_DCH2LDHRH	DAC channel 2 left aligned data holding register high	0x00
0x00 53A7		DAC_DCH2LDHRL	DAC channel 2 left aligned data holding register low	0x00
0x00 53A8		DAC_DCH1DHR8	DAC channel 1 8-bit mode data holding register	0x00
0x00 53A9		DAC_DCH2DHR8	DAC channel 2 8-bit mode data holding register	0x00
0x00 53AA to 0x00 53AB	Reserved area (2 byte)			
0x00 53AC	DAC	DAC_CH1DORH Reset value	DAC channel 1 data output register high	0x00
0x00 53AD		DAC_CH1DORL Reset value	DAC channel 1 data output register low	0x00
0x00 53AE to 0x00 53AF	Reserved area (2 byte)			
0x00 53B0	DAC	DAC_CH2DORH Reset value	DAC channel 2 data output register high	0x00
0x00 53B1		DAC_CH2DORL Reset value	DAC channel 2 data output register low	0x00
0x00 53B2 to 0x00 53BF	Reserved area			
0x00 53C0	SPI2	SPI2_CR1	SPI2 control register 1	0x00
0x00 53C1		SPI2_CR2	SPI2 control register 2	0x00
0x00 53C2		SPI2_ICR	SPI2 interrupt control register	0x00
0x00 53C3		SPI2_SR	SPI2 status register	0x02
0x00 53C4		SPI2_DR	SPI2 data register	0x00
0x00 53C5		SPI2_CRCPR	SPI2 CRC polynomial register	0x07
0x00 53C6		SPI2_RXCRCR	SPI2 Rx CRC register	0x00
0x00 53C7		SPI2_TXCRCR	SPI2 Tx CRC register	0x00

Table 10. CPU/SWIM/debug module/interrupt controller registers (continued)

Address	Block	Register label	Register name	Reset status
0x00 7F90	DM	DM_BK1RE	DM breakpoint 1 register extended byte	0xFF
0x00 7F91		DM_BK1RH	DM breakpoint 1 register high byte	0xFF
0x00 7F92		DM_BK1RL	DM breakpoint 1 register low byte	0xFF
0x00 7F93		DM_BK2RE	DM breakpoint 2 register extended byte	0xFF
0x00 7F94		DM_BK2RH	DM breakpoint 2 register high byte	0xFF
0x00 7F95		DM_BK2RL	DM breakpoint 2 register low byte	0xFF
0x00 7F96		DM_CR1	DM Debug module control register 1	0x00
0x00 7F97		DM_CR2	DM Debug module control register 2	0x00
0x00 7F98		DM_CSR1	DM Debug module control/status register 1	0x10
0x00 7F99		DM_CSR2	DM Debug module control/status register 2	0x00
0x00 7F9A		DM_ENFCTR	DM enable function register	0xFF
0x00 7F9B to 0x00 7F9F	Reserved area (5 byte)			

1. Accessible by debug module only

Table 13. Option byte description (continued)

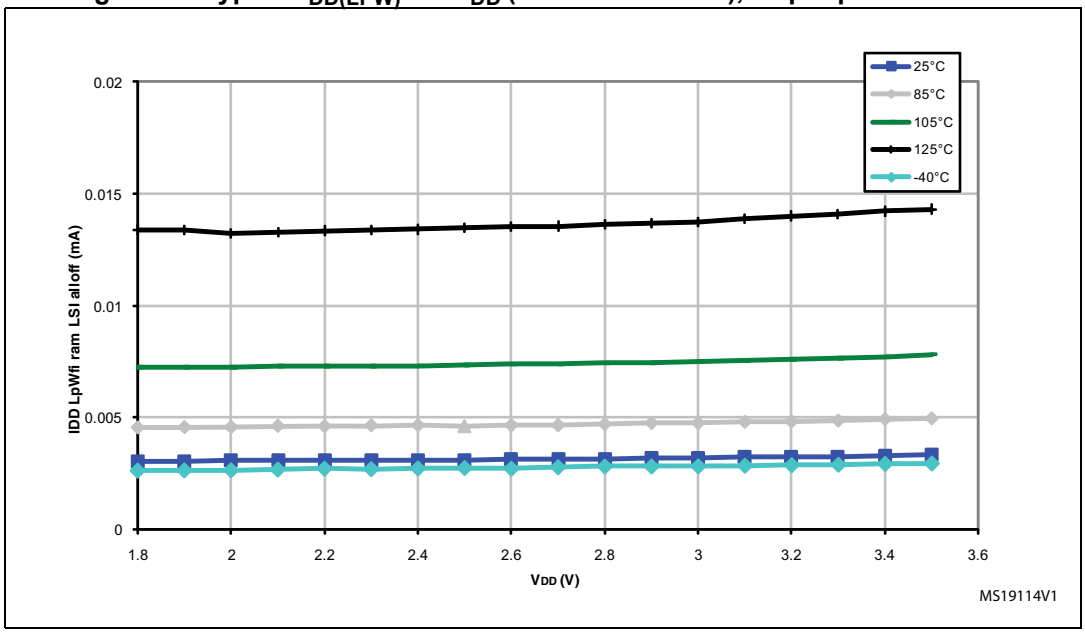
Option byte no.	Option description
OPT5	**BOR_ON**: 0: Brownout reset off 1: Brownout reset on
	BOR_TH[3:1]: Brownout reset thresholds. Refer to *Table 20* for details on the thresholds according to the value of BOR_TH bits.
OPTBL	**OPTBL[15:0]**: This option is checked by the boot ROM code after reset. Depending on the content of addresses 00 480B, 00 480C and 0x8000 (reset vector) the CPU jumps to the bootloader or to the reset vector. Refer to the UM0560 bootloader user manual for more details.

Table 24. Total current consumption in low-power wait mode at V_{DD} = 1.65 V to 3.6 V

Symbol	Parameter	Conditions(1)			Typ.	Max.	Unit
$I_{DD(LPW)}$	Supply current in low-power wait mode	LSI RC osc. (at 38 kHz)	all peripherals OFF	T_A = -40 °C to 25 °C	3.00	3.30(2)	µA
				T_A = 85 °C	4.40	9.00(3)	
				T_A = 125 °C	11.00	18.00(3)	
		LSE external clock(4) (32.768 kHz)		T_A = -40 °C to 25 °C	2.35	2.70(2)	
				T_A = 85 °C	3.10	3.70(2)	
				T_A = 125 °C	12.0	14.0(2)	

1. No floating I/Os.
2. Guaranteed by characterization results.
3. Tested at 85°C for temperature range A or 125°C for temperature range C.
4. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ LSE}$) must be added. Refer to *Table 33*.

Figure 18. Typical $I_{DD(LPW)}$ vs. V_{DD} (LSI clock source), all peripherals OFF(1)



1. Typical current consumption measured with code executed from RAM.

5. Data based on a differential I_{DD} measurement between the on-chip peripheral in reset configuration and not clocked and the on-chip peripheral when clocked and not kept under reset. The CPU is in Wait mode in both cases. No I/O pins toggling. Not tested in production.
6. Data based on a differential I_{DD} measurement between the on-chip peripheral in reset configuration and not clocked and the on-chip peripheral when clocked and not kept under reset. The CPU is in Wait mode in both cases. No I/O pins toggling. Not tested in production.
7. Data based on a differential I_{DD} measurement between the on-chip peripheral in reset configuration and not clocked and the on-chip peripheral when clocked and not kept under reset. The CPU is in Wait mode in both cases. No I/O pins toggling. Not tested in production.
8. Peripherals listed above the $I_{DD(ALL)}$ parameter ON: TIM1, TIM2, TIM3, TIM4, USART1, SPI1, I2C1, DMA1, WWDG.
9. Data based on a differential I_{DD} measurement between ADC in reset configuration and continuous ADC conversion.
10. Data based on a differential I_{DD} measurement between DAC in reset configuration and continuous DAC conversion of V_{DD} /2. Floating DAC output.
11. Data based on a differential I_{DD} measurement between COMP1 or COMP2 in reset configuration and COMP1 or COMP2 enabled with static inputs. Supply current of internal reference voltage excluded.
12. Including supply current of internal reference voltage.

Table 29. Current consumption under external reset

Symbol	Parameter	Conditions		Typ.	Unit
$I_{DD(RST)}$	Supply current under external reset (1)	PB1/PB3/PA5 pins are externally tied to V_{DD}	V_{DD} = 1.8 V	48	µA
			V_{DD} = 3 V	80	
			V_{DD} = 3.6 V	95	

1. All pins except PA0, PB0 and PB4 are floating under reset. PA0, PB0 and PB4 are configured with pull-up under reset. PB1, PB3 and PA5 must be tied externally under reset to avoid the consumption due to their schmitt trigger.

9.3.4 Clock and timing characteristics

HSE external clock (HSEBYP = 1 in CLK_ECKCR)

Subject to general operating conditions for V_{DD} and T_A.

Table 30. HSE external clock characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{HSE_ext} (1)	External clock source frequency	-	1	-	16	MHz
V_{HSEH}	OSC_IN input pin high-level voltage		0.7 x V_{DD}	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low-level voltage		V_{SS}	-	0.3 x V_{DD}	
$C_{in(HSE)}$ (1)	OSC_IN input capacitance	-	-	2.6	-	pF
I_{LEAK_HSE}	OSC_IN input leakage current	$V_{SS} < V_{IN} < V_{DD}$	-	-	±500	nA

1. Guaranteed by design.

Low speed internal RC oscillator (LSI)

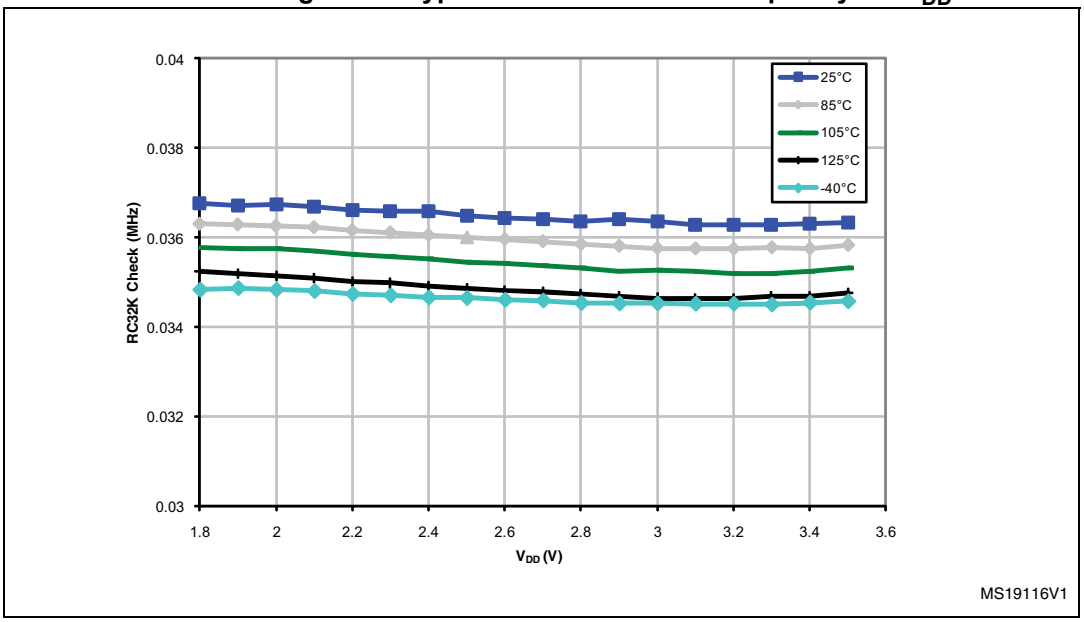
In the following table, data are based on characterization results, not tested in production, unless otherwise specified.

Table 35. LSI oscillator characteristics

Symbol	Parameter	Conditions(1)	Min.	Typ.	Max.	Unit
f_{LSI}	Frequency	-	26	38	56	kHz
$t_{su(LSI)}$	LSI oscillator wakeup time	-	-	-	200(2)	µs
$D_{(LSI)}$	LSI oscillator frequency drift(3)	0 °C ≤T_A ≤85 °C	-12	-	11	%

1. V_{DD} = 1.65 V to 3.6 V, T_A = -40 to 125 °C unless otherwise specified.
2. Guaranteed by design.
3. This is a deviation for an individual part, once the initial frequency has been measured.

Figure 24. Typical LSI clock source frequency vs. V_{DD}



9.3.5 Memory characteristics

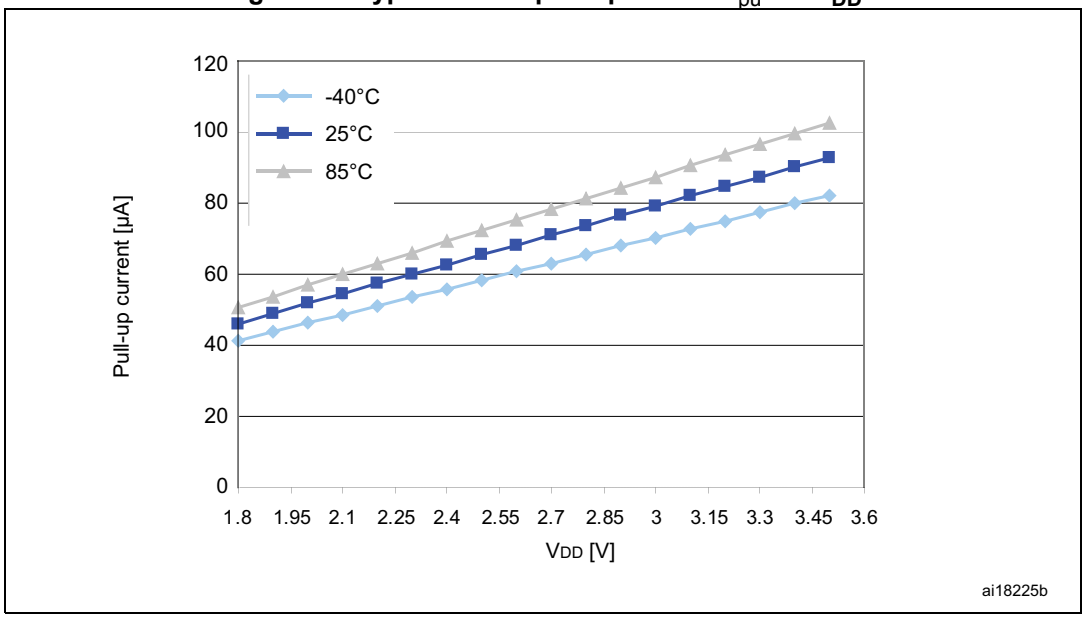
T_A = -40 to 125 °C unless otherwise specified.

Table 36. RAM and hardware registers

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{RM}	Data retention mode (1)	Halt mode (or Reset)	1.65	-	-	V

1. Minimum supply voltage without losing data stored in RAM (in Halt mode or under Reset) or in hardware registers (only in Halt mode). Guaranteed by characterization results.

Figure 36. Typical NRST pull-up current I_{pu} vs. V_{DD}



The reset network shown in *Figure 37* protects the device against parasitic resets. The user must ensure that the level on the NRST pin goes below the V_{IL} max. level specified in *Table 45*. Otherwise the reset is not taken into account internally. For power consumption-sensitive applications, the capacity of the external reset capacitor has to be reduced to limit the charge/discharge current. If the NRST signal is used to reset the external circuitry, the user must pay attention to the charge/discharge time of the external capacitor to meet the reset timing conditions of the external devices. The minimum recommended capacity is 10 nF.

Figure 37. Recommended NRST pin configuration

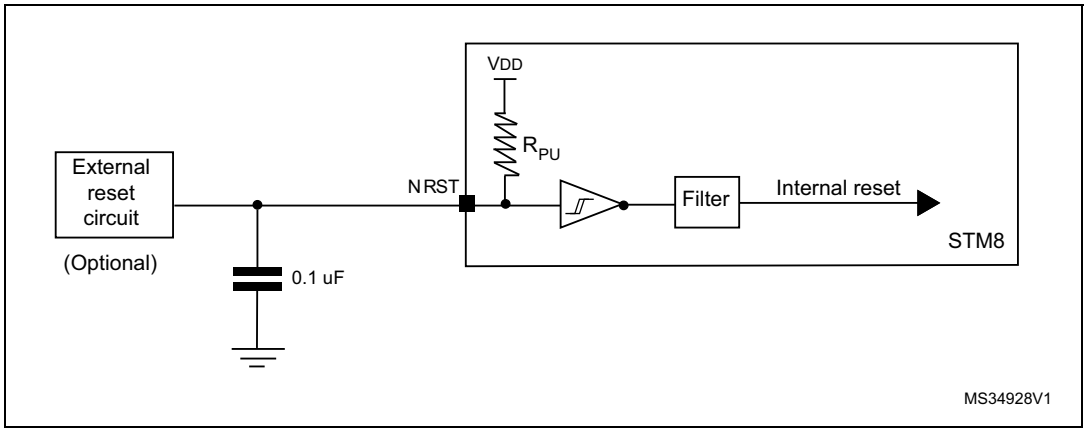


Figure 38. SPI1 timing diagram - slave mode and CPHA=0

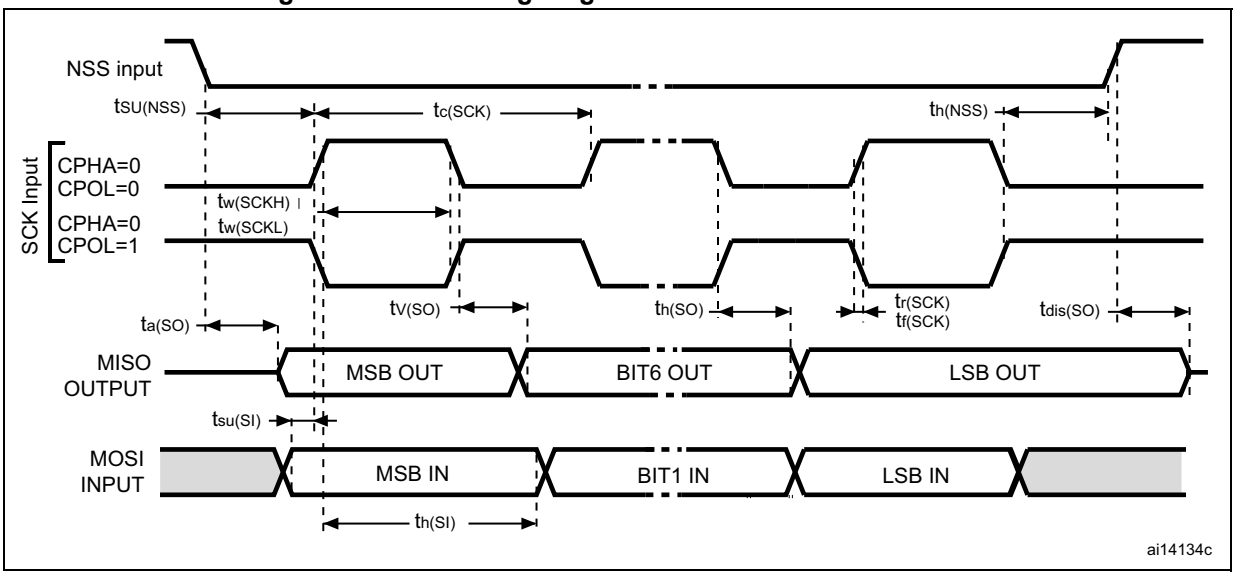
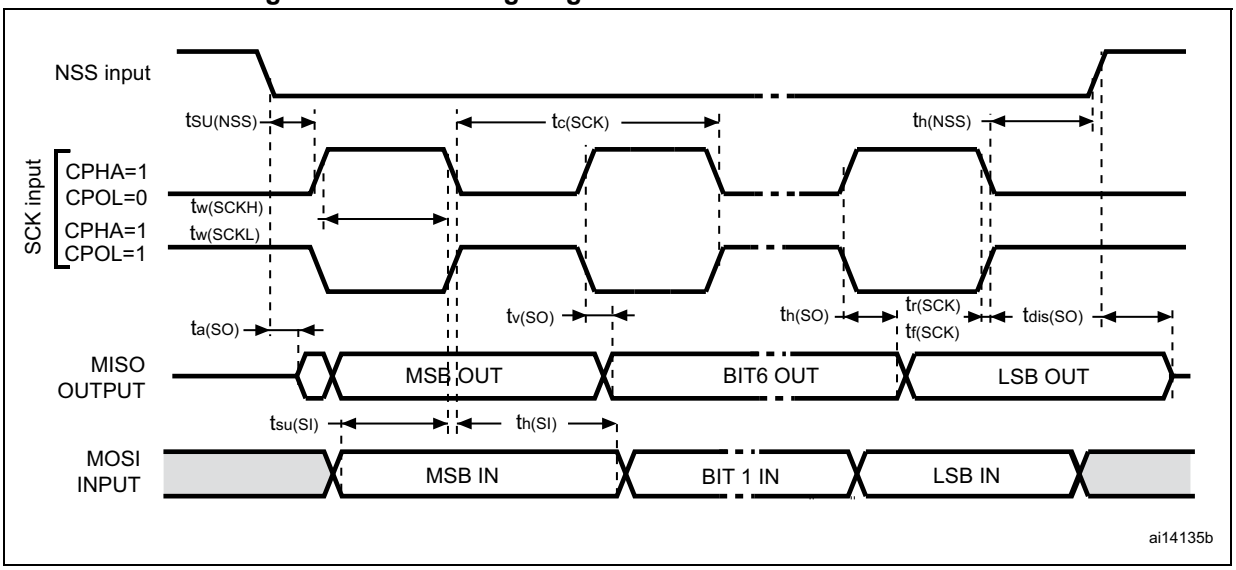


Figure 39. SPI1 timing diagram - slave mode and CPHA=1(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

9.3.10 Embedded reference voltage

In the following table, data are based on characterization results, not tested in production, unless otherwise specified.

Table 49. Reference voltage characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{REFINT}	Internal reference voltage consumption	-	-	1.4	-	µA
$T_{S\_VREFINT}$(1)(2)	ADC sampling time when reading the internal reference voltage	-	-	5	10	µs
I_{BUF}(1)	Internal reference voltage buffer consumption (used for ADC)	-	-	13.5	25	µA
$V_{REFINT\ out}$	Reference voltage output	-	1.202 (3)	1.224	1.242 (3)	V
I_{LPBUF}(1)	Internal reference voltage low-power buffer consumption (used for comparators or output)	-	-	730	1200	nA
I_{REFOUT}(1)(4)	Buffer output current	-	-	-	1	µA
C_{REFOUT}	Reference voltage output load	-	-	-	50	pF
$t_{VREFINT}$(1)	Internal reference voltage startup time	-	-	2	3	ms
t_{BUFEN}(1)(2)	Internal reference voltage buffer startup time once enabled	-	-	-	10	µs
$ACC_{VREFINT}$(5)	Accuracy of V_{REFINT} stored in the VREFINT_Factory_CONV byte	-	-	-	± 5	mV
$STAB_{VREFINT}$	Stability of V_{REFINT} over temperature	-40 °C ≤T_A ≤ 125 °C	-	20	50	ppm/°C
	Stability of V_{REFINT} over temperature	0 °C ≤T_A ≤ 50 °C	-	-	20	ppm/°C
$STAB_{VREFINT}$	Stability of V_{REFINT} after 1000 hours	-	-	-	TBD	ppm

1. Guaranteed by design.
2. Defined when ADC output reaches its final value ±1/2LSB
3. Tested in production at V_{DD} = 3 V ±10 mV.
4. To guarantee less than 1% V_{REFOUT} deviation
5. Measured at V_{DD} = 3 V ±10 mV. This value takes into account V_{DD} accuracy and ADC conversion accuracy.

Table 59. ADC1 accuracy with $V_{DDA} = V_{REF}^{+} = 1.8$ V to 2.4 V (continued)

Symbol	Parameter	Typ.	Max.(1)	Unit
Offset	Offset error	2	3	LSB
Gain	Gain error	2	3	LSB

1. Guaranteed by characterization results.

Figure 42. ADC1 accuracy characteristics

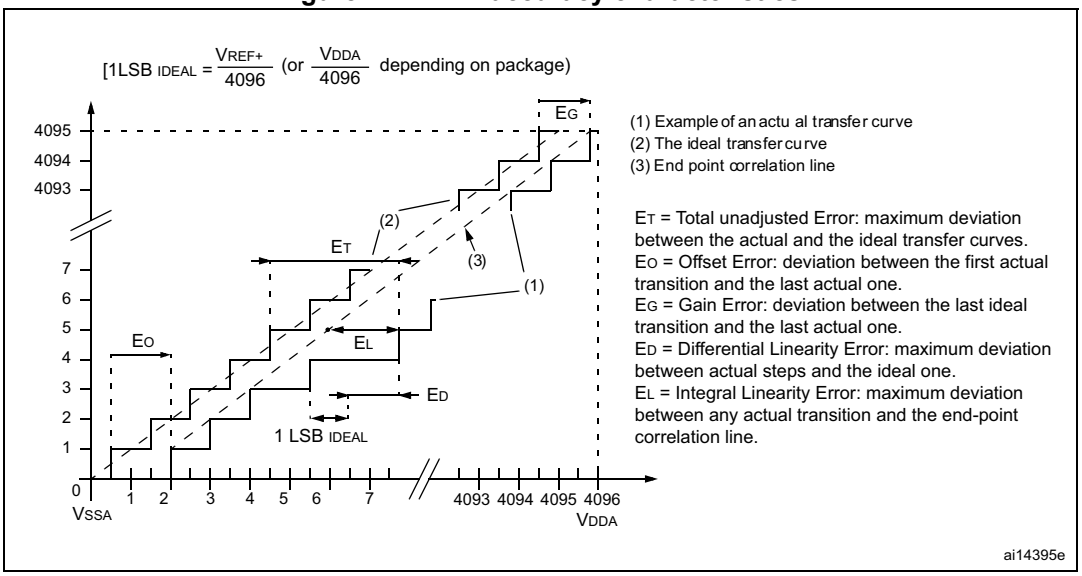
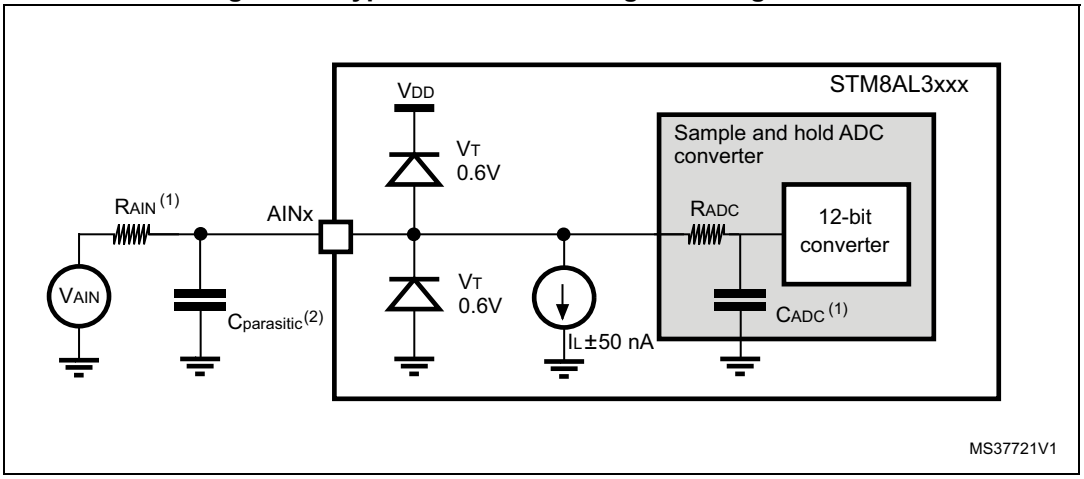


Figure 43. Typical connection diagram using the ADC



1. Refer to *Table 56* for the values of R_{AIN} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 44* or *Figure 45*, depending on whether V_{REF+} is connected to V_{DDA} or not. Good quality ceramic 10 nF capacitors should be used. They should be placed as close as possible to the chip.

Figure 44. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})

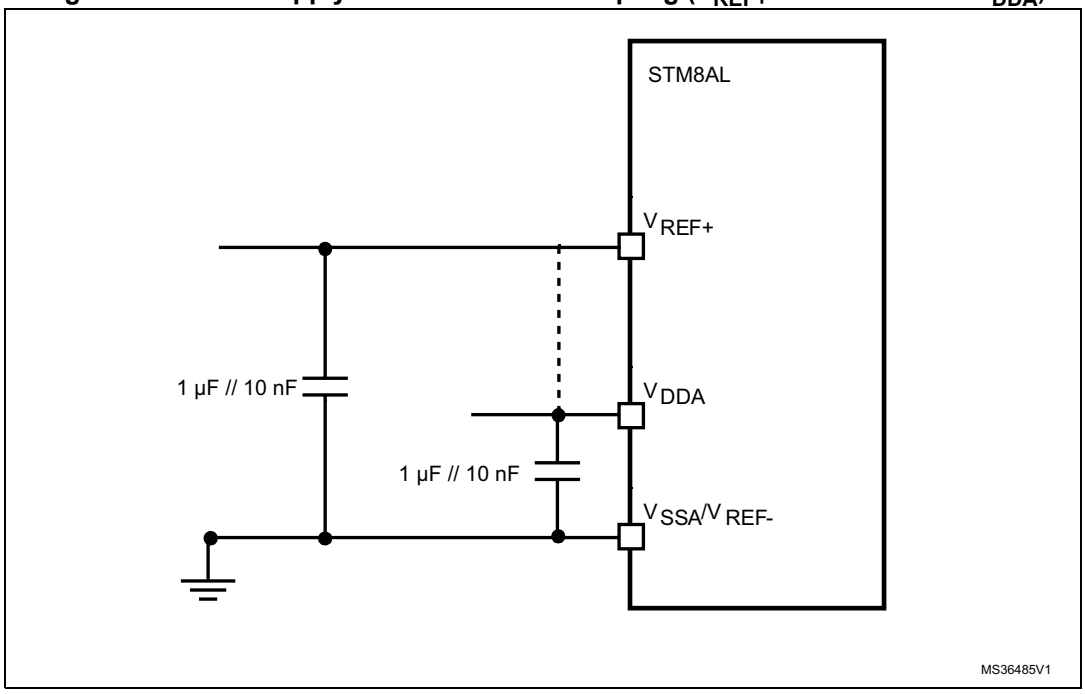


Figure 45. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})

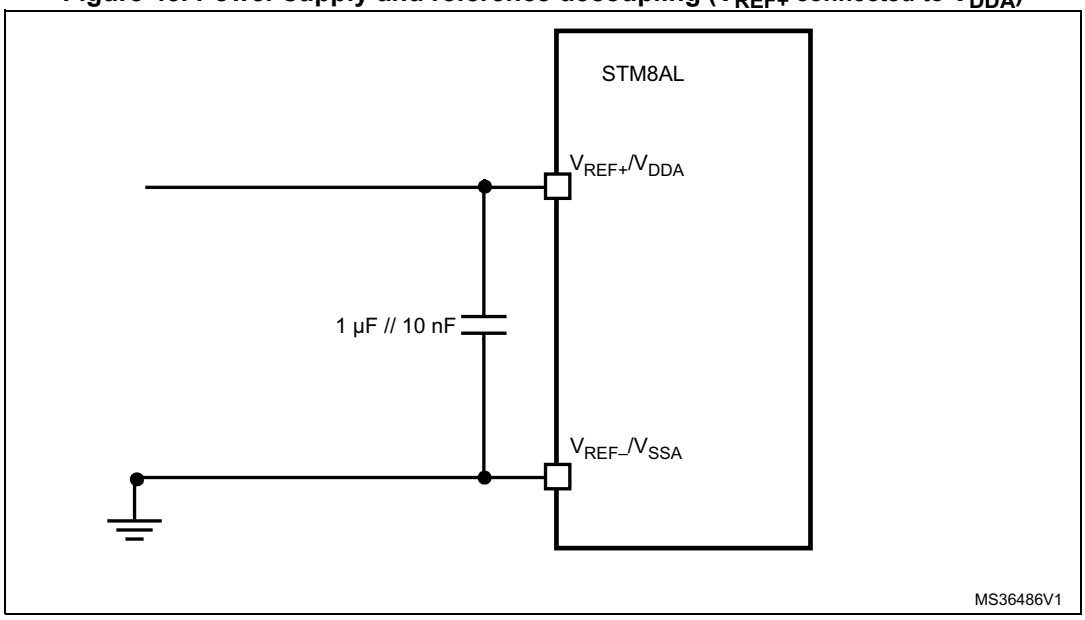


Table 65. LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package mechanical data(1)

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.220	0.320	0.380	0.0087	0.0126	0.0150
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.350	-	-	0.4862	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.350	-	-	0.4862	-
e	-	0.650	-	-	0.0256	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.100	-	-	0.0039

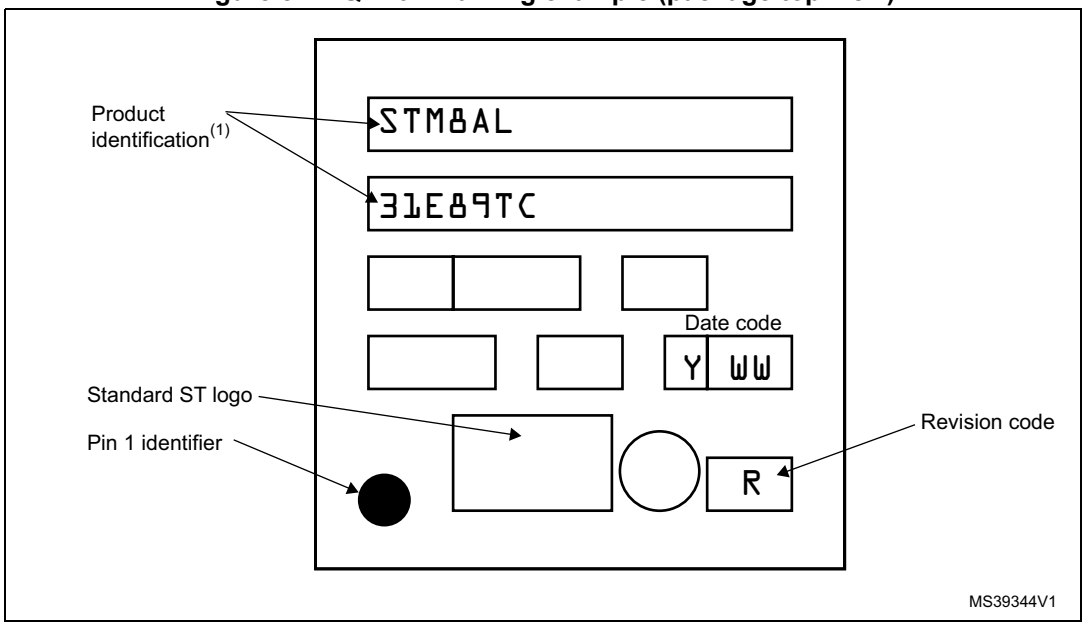
1. Values in inches are converted from mm and rounded to 4 decimal digits.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 51. LQFP64 marking example (package top view)



1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted to run a qualification activity prior to any decision to use these engineering samples.