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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	C28x
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, I²C, McBSP, SCI, SPI, uPP, UART/USART, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	41
Program Memory Size	1MB (512K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	82K x 16
Voltage - Supply (Vcc/Vdd)	1.14V ~ 3.47V
Data Converters	A/D 14x12b, 14x16b; D/A 3x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP Exposed Pad
Supplier Device Package	100-HTQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/texas-instruments/tms320f28377spzpq

STM8AL ultra-low-power microcontrollers operates either from 1.8 to 3.6 V (down to 1.65 V at power-down) or from 1.65 to 3.6 V. They are available in the -40 to +85 °C and -40 to +125 °C temperature ranges.

These features make the STM8AL ultra-low-power microcontroller families suitable for a wide range of applications.

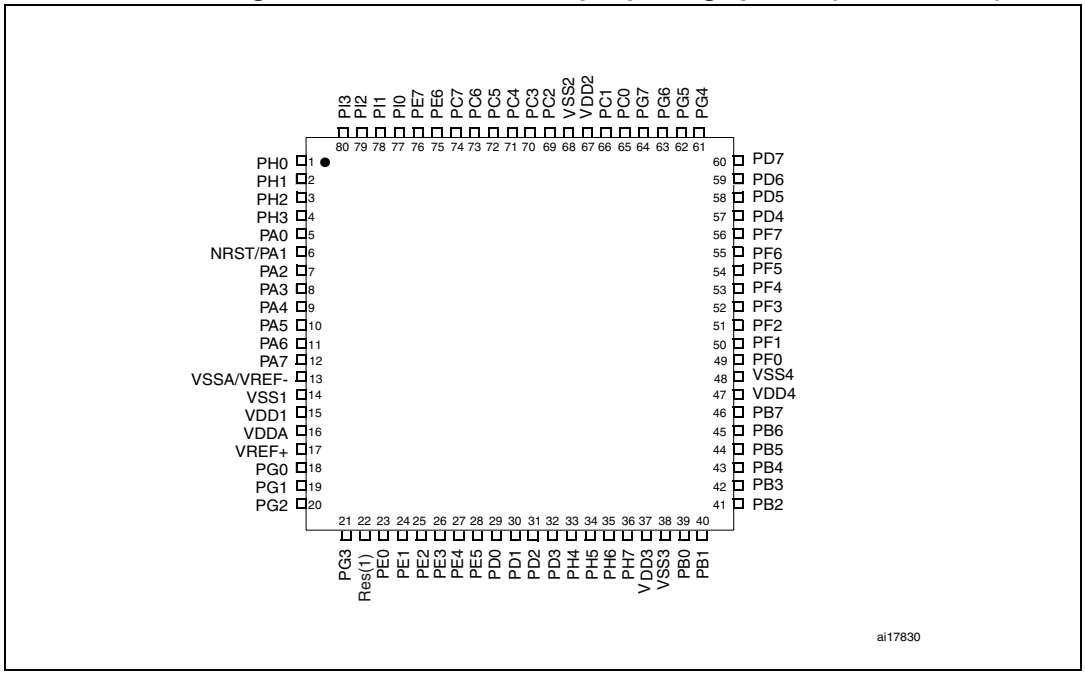
The devices are offered in one 48-pin package. Different sets of peripherals are included depending on the device. Refer to *Section 3* for an overview of the complete range of peripherals proposed in this family.

All STM8AL ultra-low-power products are based on the same architecture with the same memory mapping and a coherent pinout.

Figure 1 shows the block diagram of the high-density STM8AL3xE8x families.

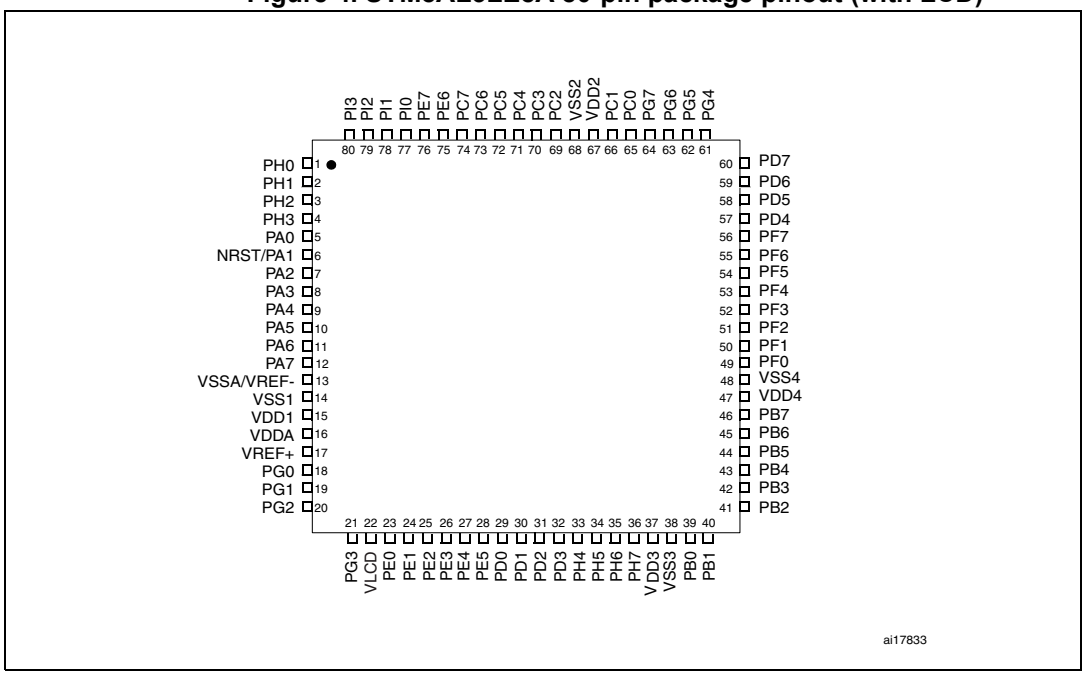
4 Pin description

Figure 3. STM8AL31E8A 80-pin package pinout (without LCD)



1. Pin 22 is reserved and must be tied to V_{DD}.
2. The above figure shows the package top view.

Figure 4. STM8AL3LE8A 80-pin package pinout (with LCD)



1. The above figure shows the package top view.

Table 5. High-density STM8AL3xE8x pin description (continued)

Pin number			Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP80	LQFP64	LQFP48				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
12	8	8	PA7/LCD_SEG0(3)/ TIM5_CH1	I/O	FT(5)	**X**	X	X	HS	X	X	**Port A7**	LCD segment 0 / TIM5 channel 1
39	31	24	PB0(4)/TIM2_CH1/ LCD_SEG10(3)/ ADC1_IN18/ COMP1_INP	I/O	FT(5)	**X**	X	X	HS	X	X	**Port B0**	Timer 2 - channel 1 / LCD segment 10 / ADC1_IN18/Comparator 1 positive input
40	32	25	PB1/TIM3_CH1/ LCD_SEG11(3)/ ADC1_IN17/ COMP1_INP	I/O	FT(5)	**X**	X	X	HS	X	X	**Port B1**	Timer 3 - channel 1 / LCD segment 11 / ADC1_IN17/Comparator 1 positive input
41	33	26	PB2/ TIM2_CH2/ LCD_SEG12(3)/ ADC1_IN16/ COMP1_INP	I/O	FT(5)	**X**	X	X	HS	X	X	**Port B2**	Timer 2 - channel 2 / LCD segment 12 / ADC1_IN16/Comparator 1 positive input
42	34	27	PB3/TIM2_ETR/ LCD_SEG13(3)/ ADC1_IN15/COMP1_INP	I/O	FT(5)	**X**	X	X	HS	X	X	**Port B3**	Timer 2 - trigger / LCD segment 13 /ADC1_IN15/Comparator 1 positive input
43	35	-	PB4(4)/SPI1_NSS/ LCD_SEG14(3)/ ADC1_IN14/COMP1_INP	I/O	FT(5)	**X**	X	X	HS	X	X	**Port B4**	SPI1 master/slave select / LCD segment 14 / ADC1_IN14/Comparator 1 positive input
-	-	28	PB4(4)/SPI1_NSS/ LCD_SEG14(3)/ ADC1_IN14/DAC_OUT2/ COMP1_INP	I/O	FT(5)	**X**	X	X	HS	X	X	**Port B4**	SPI1 master/slave select / LCD segment 14 / ADC1_IN14 / DAC channel 2 output/Comparator 1 positive input
44	36	-	PB5/SPI1_SCK/ LCD_SEG15(3)/ ADC1_IN13 COMP1_INP	I/O	FT(5)	**X**	X	X	HS	X	X	**Port B5**	SPI1 clock / LCD segment 15 / ADC1_IN13/Comparator 1 positive input
-	-	29	PB5/SPI1_SCK/ LCD_SEG15(3)/ ADC1_IN13/DAC_OUT2/ COMP1_INP	I/O	FT(5)	**X**	X	X	HS	X	X	**Port B5**	[SPI1 clock] / LCD segment 15 / ADC1_IN13 / DAC channel 2 output/Comparator 1 positive input

Table 5. High-density STM8AL3xE8x pin description (continued)

Pin number			Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP80	LQFP64	LQFP48				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
5	1	1	PA0[8]/*[USART1_CK]*[2]/ SWIM/BEEP/IR_TIM [9]	I/O	-	X	**X**	X	HS	X	X	**Port A0**	*[USART1 synchronous clock]*[2] / SWIM input and output / Beep output / Infrared Timer output
68	56	40	V_{SS2}	S	-	**-**	-	-	-	-	-	IOs ground voltage	
67	55	39	V_{DD2}	S	-	**-**	-	-	-	-	-	IOs supply voltage	
48	-	-	V_{SS4}	S	-	**-**	-	-	-	-	-	IOs ground voltage	
47	-	-	V_{DD4}	S	-	**-**	-	-	-	-	-	IOs supply voltage	

1. At power-up, the PA1/NRST pin is a reset input pin with pull-up. To be used as a general purpose pin (PA1), it can be configured only as output open-drain or push-pull, not as a general purpose input. Refer to Section *Configuring NRST/PA1 pin as general purpose output* in STM8L051/L052 Value Line, STM8L151/L152, STM8L162, STM8AL31, STM8AL3L MCU lines reference manual (RM0031).
2. [ ] Alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).
3. Available onSTM8AL3LE8xdevices only.
4. A pull-up is applied to PB0 and PB4 during the reset phase. These two pins are input floating after reset release.
5. In the 5 V tolerant I/Os, the protection diode to V_{DD} is not implemented.
6. In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer, weak pull-up and protection diode to V_{DD} are not implemented).
7. Available on STM8AL3LE8x devices only. On STM8AL31E8x devices it is reserved and must be tied to V_{DD}.
8. The PA0 pin is in input pull-up during the reset phase and after reset release.
9. High Sink LED driver capability available on PA0.

Note: The slope control of all GPIO pins, except true open drain pins, are programmable. By default the slope control is limited to 2 MHz.

System configuration options

As shown in *Table 5: High-density STM8AL3xE8x pin description*, some alternate functions can be remapped on different I/O ports by programming one of the two remapping registers described in the "Routing interface (RI) and system configuration controller" section in STM8L051/L052 Value Line, STM8L151/L152, STM8L162, STM8AL31, STM8AL3L MCU lines reference manual (RM0031).

Table 6. Flash and RAM boundary addresses

Memory area	Size	Start address	End address
RAM	4 Kbyte	0x00 0000	0x00 0FFF
Flash program memory	64 Kbyte	0x00 8000	0x01 7FFF

5.2 Register map

Table 7. Factory conversion registers

Address	Block	Register label	Register name	Reset status
0x00 4910	-	VREFINT_Factory_CONV(1)	Internal reference voltage factory conversion	0xXX
0x00 4911	-	TS_Factory_CONV_V125(2)	Temperature sensor output voltage	0xXX

1. The VREFINT_Factory_CONV byte represents the 8 LSB of the result of the VREFINT 12-bit ADC conversion performed in factory. The 2 MSB have a fixed value: 0x6.
2. The TS_Factory_CONV_V125 byte represents the 8 LSB of the result of the V125 12-bit ADC conversion performed in factory. The 2 MSB have a fixed value: 0x3.

Table 8. I/O port hardware register map

Address	Block	Register label	Register name	Reset status
0x00 5000	Port A	PA_ODR	Port A data output latch register	0x00
0x00 5001		PA_IDR	Port A input pin value register	0xXX
0x00 5002		PA_DDR	Port A data direction register	0x00
0x00 5003		PA_CR1	Port A control register 1	0x01
0x00 5004		PA_CR2	Port A control register 2	0x00
0x00 5005	Port B	PB_ODR	Port B data output latch register	0x00
0x00 5006		PB_IDR	Port B input pin value register	0xXX
0x00 5007		PB_DDR	Port B data direction register	0x00
0x00 5008		PB_CR1	Port B control register 1	0x00
0x00 5009		PB_CR2	Port B control register 2	0x00
0x00 500A	Port C	PC_ODR	Port C data output latch register	0x00
0x00 500B		PB_IDR	Port C input pin value register	0xXX
0x00 500C		PC_DDR	Port C data direction register	0x00
0x00 500D		PC_CR1	Port C control register 1	0x00
0x00 500E		PC_CR2	Port C control register 2	0x00

Table 8. I/O port hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 500F	Port D	PD_ODR	Port D data output latch register	0x00
0x00 5010		PD_IDR	Port D input pin value register	0xXX
0x00 5011		PD_DDR	Port D data direction register	0x00
0x00 5012		PD_CR1	Port D control register 1	0x00
0x00 5013		PD_CR2	Port D control register 2	0x00
0x00 5014	Port E	PE_ODR	Port E data output latch register	0x00
0x00 5015		PE_IDR	Port E input pin value register	0xXX
0x00 5016		PE_DDR	Port E data direction register	0x00
0x00 5017		PE_CR1	Port E control register 1	0x00
0x00 5018		PE_CR2	Port E control register 2	0x00
0x00 5019	Port F	PF_ODR	Port F data output latch register	0x00
0x00 501A		PF_IDR	Port F input pin value register	0xXX
0x00 501B		PF_DDR	Port F data direction register	0x00
0x00 501C		PF_CR1	Port F control register 1	0x00
0x00 501D		PF_CR2	Port F control register 2	0x00
0x00 501E	Port G	PG_ODR	Port F data output latch register	0x00
0x00 501F		PG_IDR	Port G input pin value register	0xXX
0x00 5020		PG_DDR	Port G data direction register	0x00
0x00 5021		PG_CR1	Port G control register 1	0x00
0x00 5022		PG_CR2	Port G control register 2	0x00
0x00 5023	Port H	PH_ODR	Port H data output latch register	0x00
0x00 5024		PH_IDR	Port H input pin value register	0xXX
0x00 5025		PH_DDR	Port H data direction register	0x00
0x00 5026		PH_CR1	Port H control register 1	0x00
0x00 5027		PH_CR2	Port H control register 2	0x00
0x00 5028	Port I	PI_ODR	Port I data output latch register	0x00
0x00 5029		PI_IDR	Port I input pin value register	0xXX
0x00 502A		PI_DDR	Port I data direction register	0x00
0x00 502B		PI_CR1	Port I control register 1	0x00
0x00 502C		PI_CR2	Port I control register 2	0x00

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5084	Reserved area (1 byte)			
0x00 5085	DMA1	DMA1_C1M0ARH	DMA1 memory 0 address high register (channel 1)	0x00
0x00 5086		DMA1_C1M0ARL	DMA1 memory 0 address low register (channel 1)	0x00
0x00 5087 0x00 5088	Reserved area (2 byte)			
0x00 5089	DMA1	DMA1_C2CR	DMA1 channel 2 configuration register	0x00
0x00 508A		DMA1_C2SPR	DMA1 channel 2 status & priority register	0x00
0x00 508B		DMA1_C2NDTR	DMA1 number of data to transfer register (channel 2)	0x00
0x00 508C		DMA1_C2PARH	DMA1 peripheral address high register (channel 2)	0x52
0x00 508D		DMA1_C2PARL	DMA1 peripheral address low register (channel 2)	0x00
0x00 508E		Reserved area (1 byte)		
0x00 508F		DMA1_C2M0ARH	DMA1 memory 0 address high register (channel 2)	0x00
0x00 5090		DMA1_C2M0ARL	DMA1 memory 0 address low register (channel 2)	0x00
0x00 5091 0x00 5092	Reserved area (2 byte)			
0x00 5093	DMA1	DMA1_C3CR	DMA1 channel 3 configuration register	0x00
0x00 5094		DMA1_C3SPR	DMA1 channel 3 status & priority register	0x00
0x00 5095		DMA1_C3NDTR	DMA1 number of data to transfer register (channel 3)	0x00
0x00 5096		DMA1_C3PARH_ C3M1ARH	DMA1 peripheral address high register (channel 3)	0x40
0x00 5097		DMA1_C3PARL_ C3M1ARL	DMA1 peripheral address low register (channel 3)	0x00
0x00 5098		DMA_C3M0EAR	DMA channel 3 memory 0 extended address register	0x00
0x00 5099		DMA1_C3M0ARH	DMA1 memory 0 address high register (channel 3)	0x00
0x00 509A		DMA1_C3M0ARL	DMA1 memory 0 address low register (channel 3)	0x00
0x00 509B to 0x00 509C	Reserved area (3 byte)			

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 50CA	CLK	CLK_CSSR	Clock security system register	0x00
0x00 50CB		CLK_CBEEPR	Clock BEEP register	0x00
0x00 50CC		CLK_HSICALR	HSI calibration register	0xXX
0x00 50CD		CLK_HSITRIMR	HSI clock calibration trimming register	0x00
0x00 50CE		CLK_HSIUNLCKR	HSI unlock register	0x00
0x00 50CF		CLK_REGCSR	Main regulator control status register	0bxx11 100X
0x00 50D0		CLK_PCKENR3	Peripheral clock gating register 3	0x00
0x00 50D1 to 0x00 50D2	Reserved area (2 byte)			
0x00 50D3	WWDG	WWDG_CR	WWDG control register	0x7F
0x00 50D4		WWDG_WR	WWDR window register	0x7F
0x00 50D5 to 00 50DF	Reserved area (11 byte)			
0x00 50E0	IWDG	IWDG_KR	IWDG key register	0xXX
0x00 50E1		IWDG_PR	IWDG prescaler register	0x00
0x00 50E2		IWDG_RLR	IWDG reload register	0xFF
0x00 50E3 to 0x00 50EF	Reserved area (13 byte)			
0x00 50F0	BEEP	BEEP_CSR1	BEEP control/status register 1	0x00
0x00 50F1 0x00 50F2		Reserved area (2 byte)		
0x00 50F3		BEEP_CSR2	BEEP control/status register 2	0x1F
0x00 50F4 to0x00 513F	Reserved area (76 byte)			
0x00 5140	RTC	RTC_TR1	Time register 1	0x00
0x00 5141		RTC_TR2	Time register 2	0x00
0x00 5142		RTC_TR3	Time register 3	0x00
0x00 5143	Reserved area (1 byte)			
0x00 5144	RTC	RTC_DR1	Date register 1	0x01
0x00 5145		RTC_DR2	Date register 2	0x21
0x00 5146		RTC_DR3	Date register 3	0x00
0x00 5147	Reserved area (1 byte)			

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 52B0	TIM1	TIM1_CR1	TIM1 control register 1	0x00
0x00 52B1		TIM1_CR2	TIM1 control register 2	0x00
0x00 52B2		TIM1_SMCR	TIM1 Slave mode control register	0x00
0x00 52B3		TIM1_ETR	TIM1 external trigger register	0x00
0x00 52B4		TIM1_DER	TIM1 DMA1 request enable register	0x00
0x00 52B5		TIM1_IER	TIM1 Interrupt enable register	0x00
0x00 52B6		TIM1_SR1	TIM1 status register 1	0x00
0x00 52B7		TIM1_SR2	TIM1 status register 2	0x00
0x00 52B8		TIM1_EGR	TIM1 event generation register	0x00
0x00 52B9		TIM1_CCMR1	TIM1 Capture/Compare mode register 1	0x00
0x00 52BA		TIM1_CCMR2	TIM1 Capture/Compare mode register 2	0x00
0x00 52BB		TIM1_CCMR3	TIM1 Capture/Compare mode register 3	0x00
0x00 52BC		TIM1_CCMR4	TIM1 Capture/Compare mode register 4	0x00
0x00 52BD		TIM1_CCER1	TIM1 Capture/Compare enable register 1	0x00
0x00 52BE		TIM1_CCER2	TIM1 Capture/Compare enable register 2	0x00
0x00 52BF		TIM1_CNTRH	TIM1 counter high	0x00
0x00 52C0		TIM1_CNTRL	TIM1 counter low	0x00
0x00 52C1		TIM1_PSCRH	TIM1 prescaler register high	0x00
0x00 52C2		TIM1_PSCRL	TIM1 prescaler register low	0x00
0x00 52C3		TIM1_ARRH	TIM1 Auto-reload register high	0xFF
0x00 52C4		TIM1_ARRL	TIM1 Auto-reload register low	0xFF
0x00 52C5		TIM1_RCR	TIM1 Repetition counter register	0x00
0x00 52C6		TIM1_CCR1H	TIM1 Capture/Compare register 1 high	0x00
0x00 52C7		TIM1_CCR1L	TIM1 Capture/Compare register 1 low	0x00
0x00 52C8		TIM1_CCR2H	TIM1 Capture/Compare register 2 high	0x00
0x00 52C9		TIM1_CCR2L	TIM1 Capture/Compare register 2 low	0x00
0x00 52CA		TIM1_CCR3H	TIM1 Capture/Compare register 3 high	0x00
0x00 52CB		TIM1_CCR3L	TIM1 Capture/Compare register 3 low	0x00
0x00 52CC		TIM1_CCR4H	TIM1 Capture/Compare register 4 high	0x00
0x00 52CD		TIM1_CCR4L	TIM1 Capture/Compare register 4 low	0x00
0x00 52CE		TIM1_BKR	TIM1 break register	0x00
0x00 52CF		TIM1_DTR	TIM1 dead-time register	0x00
0x00 52D0		TIM1_OISR	TIM1 output idle state register	0x00
0x00 52D1		TIM1_DCR1	DMA1 control register 1	0x00

Table 10. CPU/SWIM/debug module/interrupt controller registers (continued)

Address	Block	Register label	Register name	Reset status
0x00 7F90	DM	DM_BK1RE	DM breakpoint 1 register extended byte	0xFF
0x00 7F91		DM_BK1RH	DM breakpoint 1 register high byte	0xFF
0x00 7F92		DM_BK1RL	DM breakpoint 1 register low byte	0xFF
0x00 7F93		DM_BK2RE	DM breakpoint 2 register extended byte	0xFF
0x00 7F94		DM_BK2RH	DM breakpoint 2 register high byte	0xFF
0x00 7F95		DM_BK2RL	DM breakpoint 2 register low byte	0xFF
0x00 7F96		DM_CR1	DM Debug module control register 1	0x00
0x00 7F97		DM_CR2	DM Debug module control register 2	0x00
0x00 7F98		DM_CSR1	DM Debug module control/status register 1	0x10
0x00 7F99		DM_CSR2	DM Debug module control/status register 2	0x00
0x00 7F9A		DM_ENFCTR	DM enable function register	0xFF
0x00 7F9B to 0x00 7F9F	Reserved area (5 byte)			

1. Accessible by debug module only

Table 13. Option byte description (continued)

Option byte no.	Option description
OPT5	**BOR_ON**: 0: Brownout reset off 1: Brownout reset on
	BOR_TH[3:1]: Brownout reset thresholds. Refer to *Table 20* for details on the thresholds according to the value of BOR_TH bits.
OPTBL	**OPTBL[15:0]**: This option is checked by the boot ROM code after reset. Depending on the content of addresses 00 480B, 00 480C and 0x8000 (reset vector) the CPU jumps to the bootloader or to the reset vector. Refer to the UM0560 bootloader user manual for more details.

9 Electrical parameters

9.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

9.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A= 25 °C and T_A = T_A max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production.

9.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3 V. They are given only as design guidelines and are not tested.

Typical ADC and DAC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range.

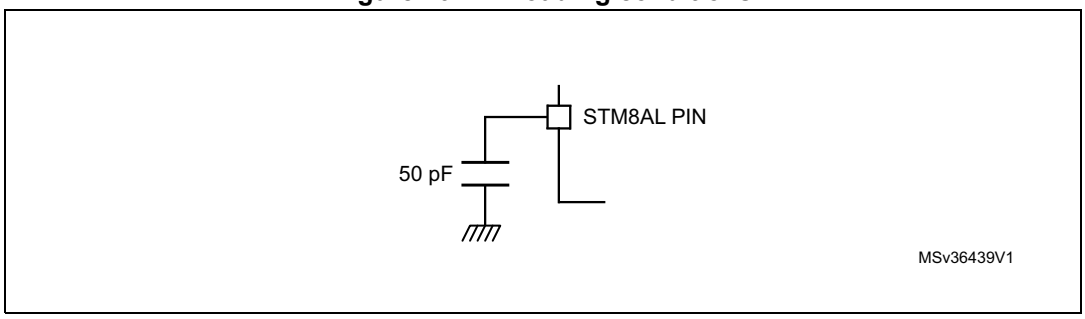
9.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

9.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 10*.

Figure 10. Pin loading conditions



9.3.2 Embedded reset and power control block characteristics

Table 20. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{VDD}	V_{DD} rise time rate	BOR detector enabled	0(1)	-	∞(1)	µs/V
	V_{DD} fall time rate	BOR detector enabled	20(1)	-	∞(1)	µs/V
t_{TEMP}	Reset release delay	V_{DD} rising BOR detector enabled	-	3	-	ms
V_{PDR}	Power-down reset threshold	Falling edge	1.3	1.5	1.65(2)	V
V_{BOR0}	Brown-out reset threshold 0 (BOR_TH[2:0]=000)	Falling edge	1.67	1.7	1.74(2)	
		Rising edge	1.69(2)	1.75	1.80	
V_{BOR1}	Brown-out reset threshold 1 (BOR_TH[2:0]=001)	Falling edge	1.87	1.93	1.97(2)	
		Rising edge	1.96(2)	2.04	2.07	
V_{BOR2}	Brown-out reset threshold 2 (BOR_TH[2:0]=010)	Falling edge	2.22	2.3	2.35(2)	
		Rising edge	2.31(2)	2.41	2.44	
V_{BOR3}	Brown-out reset threshold 3 (BOR_TH[2:0]=011)	Falling edge	2.45	2.55	2.60(2)	
		Rising edge	2.54(2)	2.66	2.7	
V_{BOR4}	Brown-out reset threshold 4 (BOR_TH[2:0]=100)	Falling edge	2.68	2.80	2.85(2)	
		Rising edge	2.78(2)	2.90	2.95	
V_{PVD0}	PVD threshold 0	Falling edge	1.80	1.84	1.88(2)	V
		Rising edge	1.88(2)	1.94	1.99	
V_{PVD1}	PVD threshold 1	Falling edge	1.98	2.04	2.09(2)	
		Rising edge	2.08(2)	2.14	2.18	
V_{PVD2}	PVD threshold 2	Falling edge	2.2	2.24	2.28(2)	
		Rising edge	2.28(2)	2.34	2.38	
V_{PVD3}	PVD threshold 3	Falling edge	2.39	2.44	2.48(2)	
		Rising edge	2.47(2)	2.54	2.58	
V_{PVD4}	PVD threshold 4	Falling edge	2.57	2.64	2.69(2)	
		Rising edge	2.68(2)	2.74	2.79	
V_{PVD5}	PVD threshold 5	Falling edge	2.77	2.83	2.88(2)	
		Rising edge	2.87(2)	2.94	2.99	
V_{PVD6}	PVD threshold 6	Falling edge	2.97	3.05	3.09(2)	
		Rising edge	3.08(2)	3.15	3.20	

Table 25. Total current consumption and timing in Active-halt mode at V_{DD} = 1.65 V to 3.6 V (continued)

Symbol	Parameter	Conditions(1)			Typ.	Max.(2)	Unit
$t_{WU\_HSI(AH)}$(9)(10)	Wakeup time from Active-halt mode to Run mode (using HSI)	-	-	-	4.70	7.00	µs
$t_{WU\_LSI(AH)}$(9)(10)	Wakeup time from Active-halt mode to Run mode (using LSI)	-	-	-	150.0	-	µs

1. No floating I/O, unless otherwise specified.
2. Guaranteed by characterization results.
3. RTC enabled. Clock source = LSI
4. RTC enabled, LCD enabled with external V_{LCD} = 3 V, static duty, division ratio = 256, all pixels active, no LCD connected.
5. RTC enabled, LCD enabled with external V_{LCD}, 1/4 duty, 1/3 bias, division ratio = 64, all pixels active, no LCD connected.
6. LCD enabled with internal LCD booster V_{LCD} = 3 V, 1/4 duty, 1/3 bias, division ratio = 64, all pixels active, no LCD connected.
7. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ LSE}$) must be added. Refer to *Table 33*
8. RTC enabled. Clock source = LSE
9. Wakeup time until start of interrupt vector fetch.
   The first word of interrupt routine is fetched 4 CPU cycles after t_{WU}.
10. ULP=0 or ULP=1 and FWU=1 in the PWR_CSR2 register.

Table 26. Typical current consumption in Active-halt mode, RTC clocked by LSE external crystal

Symbol	Parameter	Condition(1)		Typ.	Unit
$I_{DD(AH)}$ (2)	Supply current in Active-halt mode	V_{DD} = 1.8 V	LSE	1.15	µA
			LSE/32(3)	1.05	
		V_{DD} = 3 V	LSE	1.30	
			LSE/32(3)	1.20	
		V_{DD} = 3.6 V	LSE	1.45	
			LSE/32(3)	1.35	

1. No floating I/O, unless otherwise specified.
2. Based on measurements on bench with 32.768 kHz external crystal oscillator.
3. RTC clock is LSE divided by 32.

LSE external clock (LSEBYP=1 in CLK_ECKCR)

The LSE is available on STM8AL31E8x devices only.

Subject to general operating conditions for V_{DD} and T_A.

Table 31. LSE external clock characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{LSE_ext}	External clock source frequency	-	32.768	-	kHz
V_{LSEH}	OSC32_IN input pin high-level voltage	$0.7xV_{DD}$(1)	-	V_{DD}(1)	V
V_{LSEL}	OSC32_IN input pin low-level voltage	V_{SS}(1)		$0.3xV_{DD}$(1)	
$C_{in(LSE)}$	OSC32_IN input capacitance	-	0.6	-	pF
I_{LEAK_LSE}	OSC32_IN input leakage current	-	-	±500	nA

1. Guaranteed by characterization results.

HSE crystal/ceramic resonator oscillator

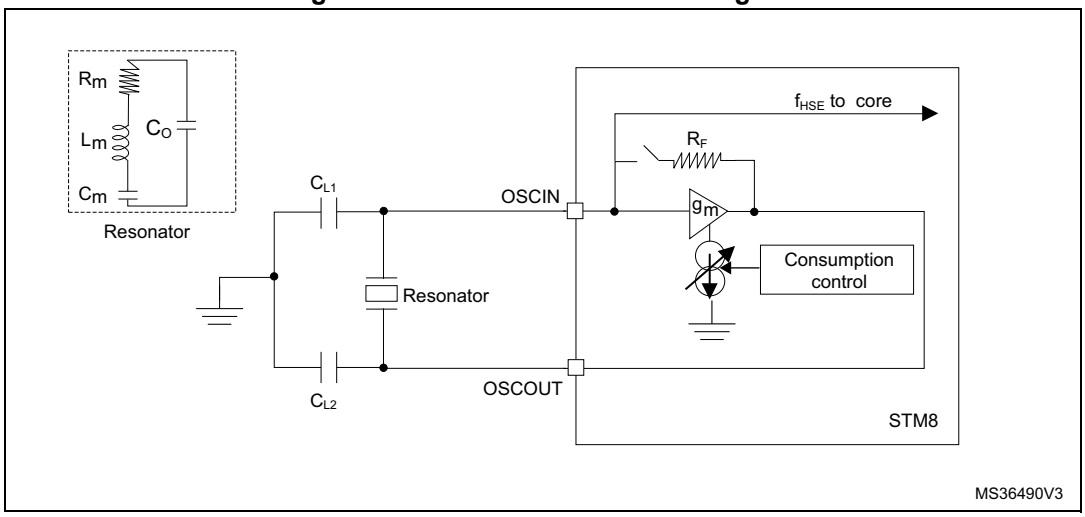
The HSE clock can be supplied with a 1 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

Table 32. HSE oscillator characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{HSE}	High speed external oscillator frequency	-	1	-	16	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
$C^{(1)(2)}$	Recommended load capacitance	-	-	20	-	pF
$I_{DD(HSE)}$	HSE oscillator power consumption	C = 20 pF, f_{OSC} = 16 MHz	-	-	2.5 (startup) 0.7 (stabilized)(3)	mA
		C = 10 pF, f_{OSC} =16 MHz	-	-	2.5 (startup) 0.46 (stabilized)(3)	
g_m	Oscillator transconductance	-	3.5(3)	-	-	mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized		1	-	ms

1. $C=C_{L1}=C_{L2}$ is approximately equivalent to 2 x crystal C_{LOAD}.
2. The oscillator selection can be optimized in terms of supply current using a high quality resonator with small R_m value. Refer to crystal manufacturer for more details
3. Guaranteed by design.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 16 MHz oscillation. This value is measured for a standard crystal resonator and it varies significantly with the crystal manufacturer.

Figure 21. HSE oscillator circuit diagram



HSE oscillator critical g_m formula

$$g_{mcrit} = (2 \times \Pi \times f_{HSE})^2 \times R_m(2Co + C)^2$$

R_m: Motional resistance (see crystal specification), L_m: Motional inductance (see crystal specification), C_m: Motional capacitance (see crystal specification), Co: Shunt capacitance (see crystal specification), C_{L1}=C_{L2}=C: Grounded external capacitance

$g_m >> g_{mcrit}$

LSE crystal/ceramic resonator oscillator

The LSE is available on STM8AL31E8x devices only.

The LSE clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

Flash memory

Table 37. Flash program memory/data EEPROM memory

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operating voltage (all modes, read/write/erase)	f_{SYSCLK} = 16 MHz	1.65	-	3.6	V
t_{prog}	Programming time for 1 or 128 byte (block) erase/write cycles (on programmed byte)	-	-	6	-	ms
	Programming time for 1 to 128 byte (block) write cycles (on erased byte)	-	-	3	-	ms
I_{prog}	Programming/ erasing consumption	T_A=+25 °C, V_{DD} = 3.0 V	-	0.7	-	mA
		T_A=+25 °C, V_{DD} = 1.8 V	-		-	

Table 38. Flash program memory

Symbol	Parameter	Conditions	Min.	Max.	Unit
T_{WE}	Temperature for writing and erasing	-	-40	125	°C
N_{WE}	Flash program memory endurance (erase/write cycles)(1)	T_A= 25 °C	1000	-	cycles
t_{RET}	Data retention time	T_A= 25 °C	40	-	years
		T_A= 55 °C	20	-	

1. The physical granularity of the memory is 4 byte, so cycling is performed on 4 byte even when a write/erase operation addresses a single byte.

Data memory

Table 39. Data memory

Symbol	Parameter	Conditions	Min.	Max.	Unit
T_{WE}	Temperature for writing and erasing	-	-40	125	°C
N_{WE}	Data memory endurance (erase/write cycles)(1)	T_A= 25 °C	300 k	-	cycles
		T_A= -40 to 125 °C	100 k(2)	-	
t_{RET}	Data retention time	T_A= 25 °C	40(2) (3)	-	years
		T_A= 55 °C	20(2) (3)	-	

1. The physical granularity of the memory is 4 byte, so cycling is performed on 4 byte even when a write/erase operation addresses a single byte.
2. More information on the relationship between data retention time and number of write/erase cycles is available in a separate technical document.
3. Retention time for 256B of data memory after up to 1000 cycles at 125 °C.

9.3.8 Communication interfaces

SPI1 - Serial peripheral interface

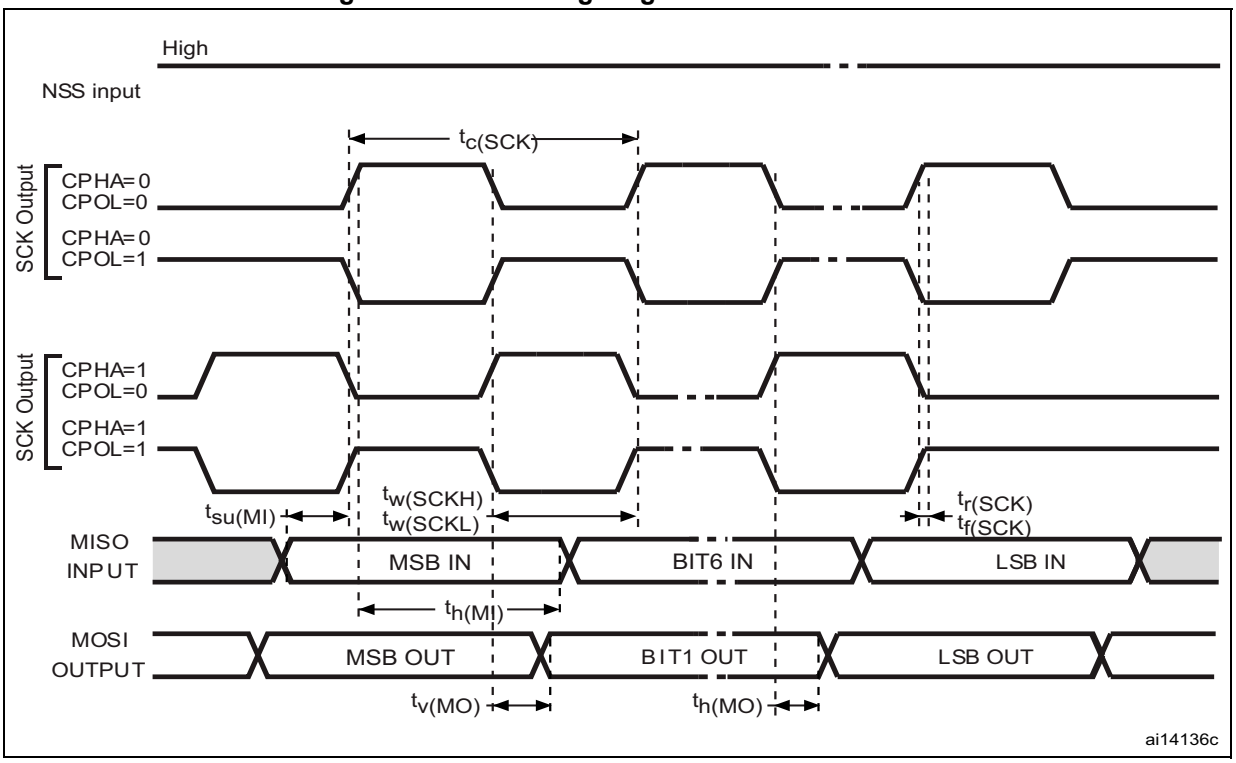
Unless otherwise specified, the parameters given in *Table 46* are derived from tests performed under ambient temperature, f_{SYSCLK} frequency and V_{DD} supply voltage conditions summarized in *Section 9.3.1*. Refer to I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 46. SPI1 characteristics

Symbol	Parameter	Conditions(1)	Min.	Max.	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI1 clock frequency	Master mode	0	8	MHz
		Slave mode	0	8	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI1 clock rise and fall time	Capacitive load: C = 30 pF	-	30	ns
$t_{su(NSS)}$(2)	NSS setup time	Slave mode	4 x $1/f_{SYSCLK}$	-	
$t_{h(NSS)}$(2)	NSS hold time	Slave mode	80	-	
$t_{w(SCKH)}$(2) $t_{w(SCKL)}$(2)	SCK high and low time	Master mode, f_{MASTER} = 8 MHz, f_{SCK}= 4 MHz	105	145	
$t_{su(MI)}$(2) $t_{su(SI)}$(2)	Data input setup time	Master mode	30	-	
		Slave mode	3	-	
$t_{h(MI)}$(2) $t_{h(SI)}$(2)	Data input hold time	Master mode	15	-	
		Slave mode	0	-	
$t_{a(SO)}$(2)(3)	Data output access time	Slave mode	-	3x $1/f_{SYSCLK}$	
$t_{dis(SO)}$(2)(4)	Data output disable time	Slave mode	30	-	
$t_{v(SO)}$(2)	Data output valid time	Slave mode (after enable edge)	-	60	
$t_{v(MO)}$(2)	Data output valid time	Master mode (after enable edge)	-	20	
$t_{h(SO)}$(2)	Data output hold time	Slave mode (after enable edge)	15	-	
$t_{h(MO)}$(2)		Master mode (after enable edge)	1	-	

1. Parameters are given by selecting 10 MHz I/O output frequency.
2. Guaranteed by characterization results or by design.
3. Min. time is for the minimum time to drive the output and max. time is for the maximum time to validate the data.
4. Min. time is for the minimum time to invalidate the output and max. time is for the maximum time to put the data in Hi-Z.

Figure 40. SPI1 timing diagram - master mode(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.