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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

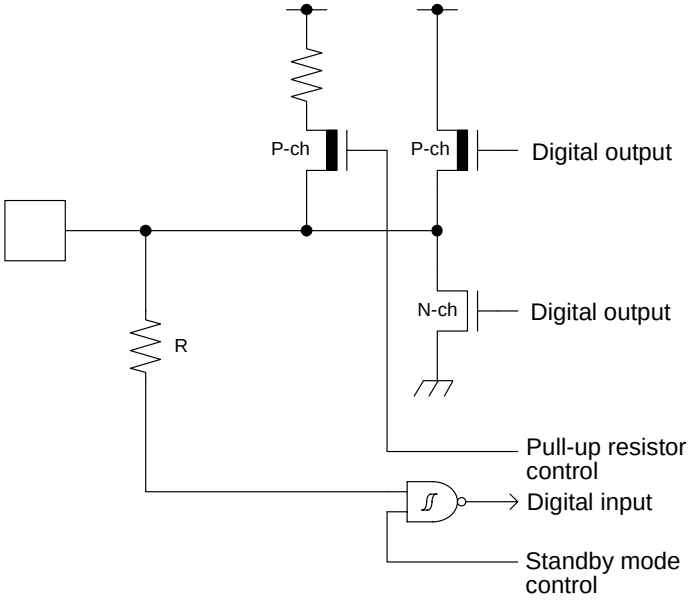
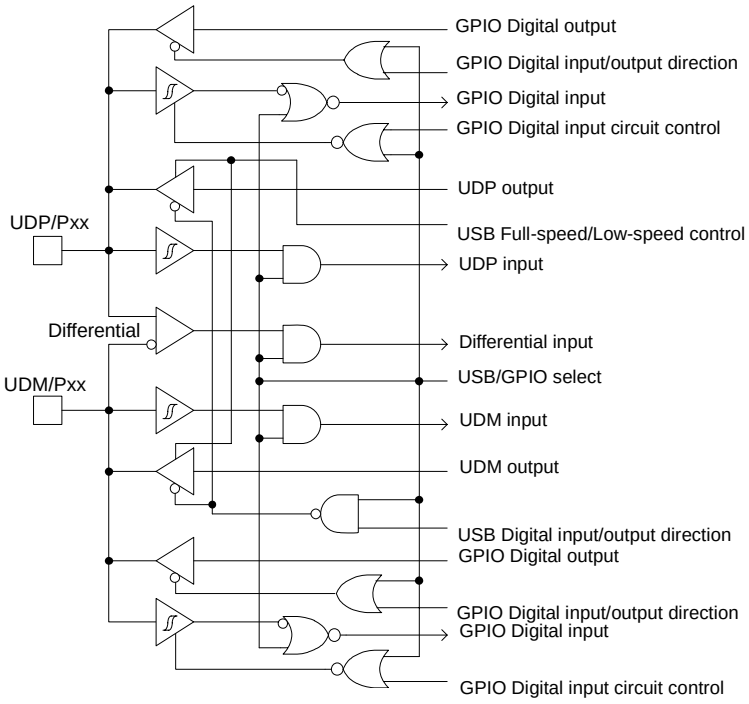
Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CSIO, EBI/EMI, Ethernet, I²C, LINbus, SD, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	120
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2c28h0agv2000a

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
29	-	-	-	P5B FRCK0_1 TIOB5_1 MADATA27_0	E	I
30	21	18	G3	P08 SIN14_0 TIOB12_0 INT17_0 MDQM0_0	E	K
31	22	19	G4	P09 SOT14_0 (SDA14_0) TIOB13_0 INT18_0 MDQM1_0	E	K
32	23	20	G5	P0A ADTG_1 SCK14_0 (SCL14_0) AIN2_1 MCLKOUT_0	L	I
33	-	-	-	P5C TIOA11_2 MADATA28_0 RTCCO_1 SUBOUT_1	E	I
34	24	-	G6	P30 TIOA13_2 INT03_2 MDQM2_0 I2SDI0_0	E	K
35	25	-	H4	P31 TIOB13_2 MDQM3_0 I2SCK0_0	E	I
36	26	21	H2	P32 BIN2_1 INT19_0 S_DATA1_0	L	K
37	27	22	J1	P33 FRCK0_0 ZIN2_1 S_DATA0_0	L	I
38	28	23	H3	P34 IC03_0 INT00_1 S_CLK_0	L	K
39	29	24	H1	VCC	-	-
40	30	25	H5	VSS	-	-
41	31	26	H6	P35 IC02_0 INT01_1 S_CMD_0	L	K

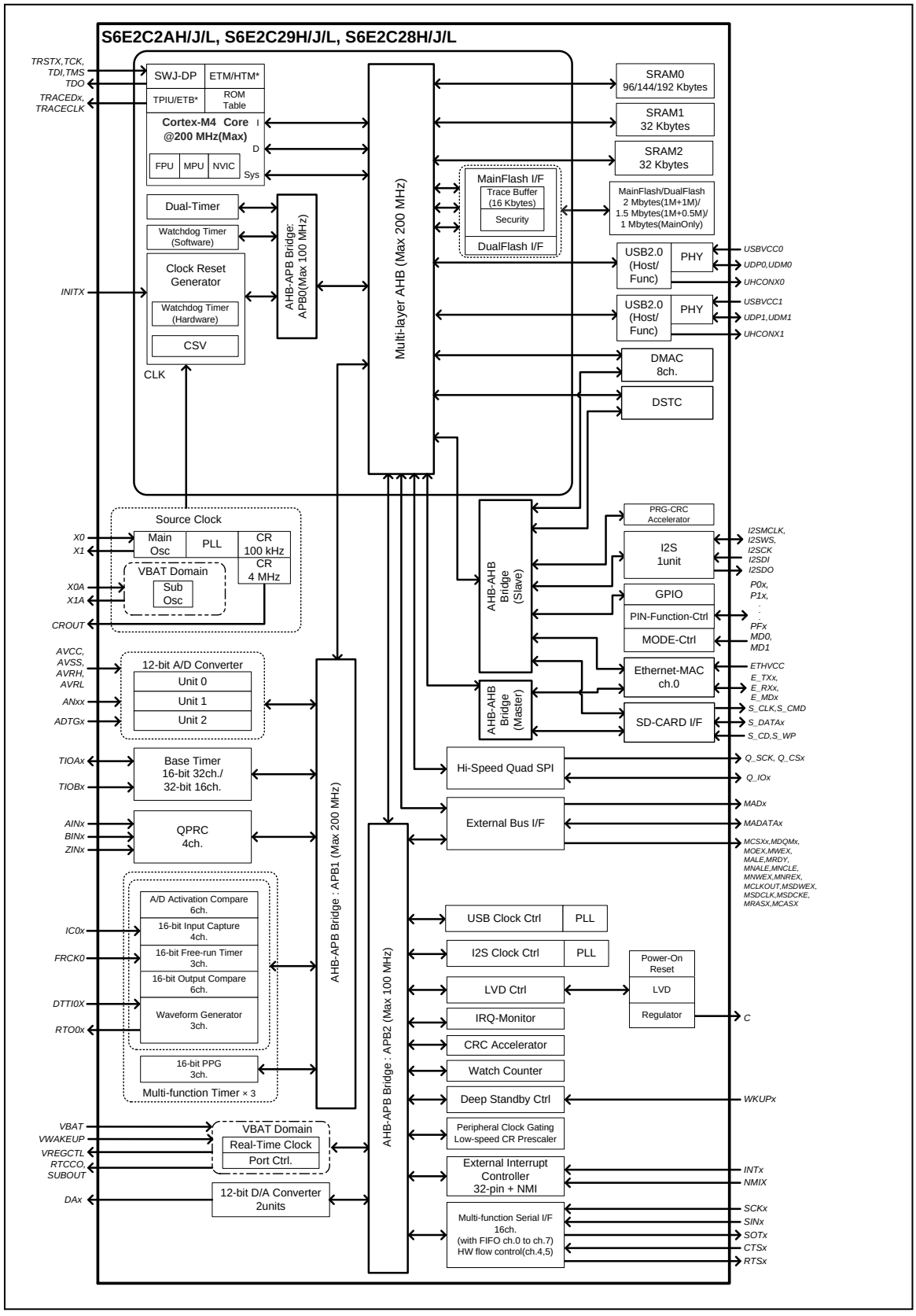
Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
74	59	51	P6	P47 X1A	Q	T
75	60	52	P8	VBAT	-	-
76	61	53	N6	P48 VREGCTL	O	U
77	62	54	M6	P49 VWAKEUP	O	U
78	63	-	K5	PF0 SCS63_0 FRCK1_1 TIOA15_1 INT22_1	E	K
79	64	-	K6	PF1 SCS62_0 TIOB15_1 INT23_1	E	K
80	65	55	L6	P70 ADTG_8 SIN1_1 INT06_0 MRDY_0	I	K
81	66	56	J6	P71 SOT1_1 (SDA1_1) MAD00_0	E	I
82	67	57	L8	P72 SIN9_0 TIOB0_0 INT07_0 MAD01_0	E	K
83	68	58	K8	P73 SOT9_0 (SDA9_0) TIOB1_0 MAD02_0	E	I
84	69	59	J8	P74 SCK9_0 (SCL9_0) TIOB2_0 MAD03_0	E	I
85	70	-	N8	PF2 RTO10_1 (PPG10_1) TIOA6_1 MRASX_0	L	I
86	71	-	M8	PF3 RTO11_1 (PPG10_1) TIOB6_1 INT05_1 MCASX_0	L	K

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
198	166	136	D6	P6E ADTG_5 SCK4_1 (SCL4_1) IC23_1 INT29_0 E_PPS	E	W
199	-	-	-	P6D SCK14_1 (SCL14_1) IC22_1 TIOB6_2	E	I
200	-	-	-	P6C SOT14_1 (SDA14_1) IC21_1 TIOA6_2	E	I
201	-	-	-	P6B SIN14_1 IC20_1 TIOB7_2 INT14_2	E	K
202	-	-	-	P6A DTTI2X_1 TIOA7_2	E	I
203	-	-	-	P69 RTO20_1 (PPG20_1) TIOB14_2	E	I
204	-	-	-	P68 SCK13_1 (SCL13_0) RTO21_1 (PPG20_1) TIOA14_2	E	I
205	-	-	-	P67 SOT13_1 (SDA13_1) RTO22_1 (PPG22_1) TIOB15_2	E	I
206	-	-	-	P66 SIN13_1 RTO23_1 (PPG22_1) TIOA15_2 INT15_2	E	K
207	167	-	E6	P65 RTO24_1 (PPG24_1) INT28_1	E	K
208	168	-	B5	P64 CTS4_0 RTO25_1 (PPG24_1) INT29_1	I	K

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Real-time clock	RTCCO_0	0.5 seconds pulse output pin of real-time clock	211	171	139	C4
	RTCCO_1		33	-	-	-
	SUBOUT_0	Sub-clock output pin	211	171	139	C4
	SUBOUT_1		33	-	-	-
USB0	UDM0	USB ch 0 device/host D – pin	214	174	142	A3
	UDP0	USB ch 0 device/host D + pin	215	175	143	A2
	UHCONX0	USB ch 0 external pull-up control pin	211	171	139	C4
USB1	UDM1	USB ch 1 device/host D – pin	160	130	106	D14
	UDP1	USB ch 1 device/host D + pin	161	131	107	C14
	UHCONX1	USB ch 1 external pull-up control pin	155	125	101	E13
Low power consump-tion mode	WKUP0	Deep standby mode return signal input pin 0	158	128	104	C13
	WKUP1	Deep standby mode return signal input pin 1	14	13	10	E5
	WKUP2	Deep standby mode return signal input pin 2	70	55	47	L5
	WKUP3	Deep standby mode return signal input pin 3	212	172	140	B3
D/A converter	DA0	D/A converter ch 0 analog output pin	100	83	67	M11
	DA1	D/A converter ch 1 analog output pin	99	82	66	N11
VBAT	VREGCTL	On-board regulator control pin	76	61	53	N6
	VWAKEUP	The return signal input pin from a hibernation state	77	62	54	M6
SD I/F	S_CLK_0	SD memory card interface SD memory card clock output pin	38	28	23	H3
	S_CMD_0	SD memory card interface SD memory card command output	41	31	26	H6
	S_DATA1_0	SD memory card interface SD memory card data bus	36	26	21	H2
	S_DATA0_0		37	27	22	J1
	S_DATA3_0		42	32	27	J5
	S_DATA2_0		43	33	28	J4
	S_CD_0	SD memory card interface SD memory card detection pin	45	35	30	J2
	S_WP_0	SD memory card interface SD memory card write protection	44	34	29	J3

Type	Circuit	Remarks
G		・ CMOS level output ・ CMOS level hysteresis input ・ Pull-up resistor control ・ Standby mode control ・ Pull-up resistor: approximately 50 kΩ ・ I_{OH} = -12 mA, I_{OL} = 12 mA ・ When this pin is used as an I^2C pin, the digital output P-ch transistor is always off.
H		It is possible to select either USB I/O or GPIO function. When the USB I/O is selected: ・ Full-speed, low-speed control When the GPIO is selected: ・ CMOS level output ・ CMOS level hysteresis input ・ Standby mode control ・ I_{OH} = -20.5 mA, I_{OL} = 18.5 mA

8. Block Diagram



Peripheral Address Map

Start Address	End Address	Bus	Peripherals
0x4000_0000	0x4000_0FFF	AHB	MainFlash I/F register
0x4000_1000	0x4000_FFFF		Reserved
0x4001_0000	0x4001_0FFF	APB0	Clock/reset control
0x4001_1000	0x4001_1FFF		Hardware watchdog timer
0x4001_2000	0x4001_2FFF		Software watchdog timer
0x4001_3000	0x4001_4FFF		Reserved
0x4001_5000	0x4001_5FFF		Dual-timer
0x4001_6000	0x4001_FFFF		Reserved
0x4002_0000	0x4002_0FFF	APB1	Multi-Function Timer unit 0
0x4002_1000	0x4002_1FFF		Multi-Function Timer unit 1
0x4002_2000	0x4002_2FFF		Multi-Function Timer unit 1
0x4002_3000	0x4002_3FFF		Reserved
0x4002_4000	0x4002_4FFF		PPG
0x4002_5000	0x4002_5FFF		Base timer
0x4002_6000	0x4002_6FFF		Quadrature position/revolution counter
0x4002_7000	0x4002_7FFF		A/D converter
0x4002_8000	0x4002_DFFF		Reserved
0x4002_E000	0x4002_EFFF		Internal CR trimming
0x4002_F000	0x4002_FFFF		Reserved
0x4003_0000	0x4003_0FFF	APB2	External interrupt controller
0x4003_1000	0x4003_1FFF		Interrupt request batch-read function
0x4003_2000	0x4003_2FFF		Reserved
0x4003_3000	0x4003_3FFF		D/A converter
0x4003_4000	0x4003_4FFF		Reserved
0x4003_5000	0x4003_57FF		Low voltage detector
0x4003_5800	0x4003_5FFF		Deep standby mode Controller
0x4003_6000	0x4003_6FFF		USB clock generator
0x4003_7000	0x4003_7FFF		Reserved
0x4003_8000	0x4003_8FFF		Multi-function serial interface
0x4003_9000	0x4003_9FFF		CRC
0x4003_A000	0x4003_AFFF		Watch counter
0x4003_B000	0x4003_BFFF		RTC/port control
0x4003_C000	0x4003_C0FF		Low-speed CR prescaler
0x4003_C100	0x4003_C7FF		Peripheral clock gating
0x4003_C800	0x4003_CFFF		Reserved
0x4003_D000	0x4003_DFFF		I^2S prescaler
0x4003_E000	0x4003_EFFF		Reserved
0x4003_F000	0x4003_FFFF		External memory interface

11. Pin Status in Each CPU State

The terms used for pin status have the following meanings:

- INITX = 0

  This is the period when the INITX pin is at the L level.

- INITX = 1

  This is the period when the INITX pin is at the H level.

- SPL = 0

  This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to 0.

- SPL = 1

  This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to 1.

- Input enabled

  Indicates that the input function can be used.

- Internal input fixed at 0

  This is the status that the input function cannot be used. Internal input is fixed at L.

- Hi-Z

  Indicates that the pin drive transistor is disabled and the pin is put in the Hi-Z state.

- Setting disabled

  Indicates that the setting is disabled.

- Maintain previous state

  Maintains the state that was immediately prior to entering the current mode.
  If a built-in peripheral function is operating, the output follows the peripheral function.
  If the pin is being used as a port, that output is maintained.

- Analog input is enabled

  Indicates that the analog input is enabled.

- Trace output

  Indicates that the trace function can be used.

- GPIO selected

  In Deep standby mode, pins switch to the general-purpose I/O port.

- Setting prohibition

  Prohibition of a setting by specification limitation

Pin Status Type	Function Group	Power-On Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC mode or Deep Standby Stop mode State		Return From Deep Standby mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
M	Analog input selected	Hi-Z	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled
	External interrupt enable selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	Resource other than above selected						Hi-Z/internal input fixed at 0			
	GPIO selected									
N	Analog input selected	Hi-Z	Hi-Z/ internal input fixed at0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled
	Trace selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Trace output	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	Resource other than above selected						Hi-Z/internal input fixed at 0			
	GPIO selected									

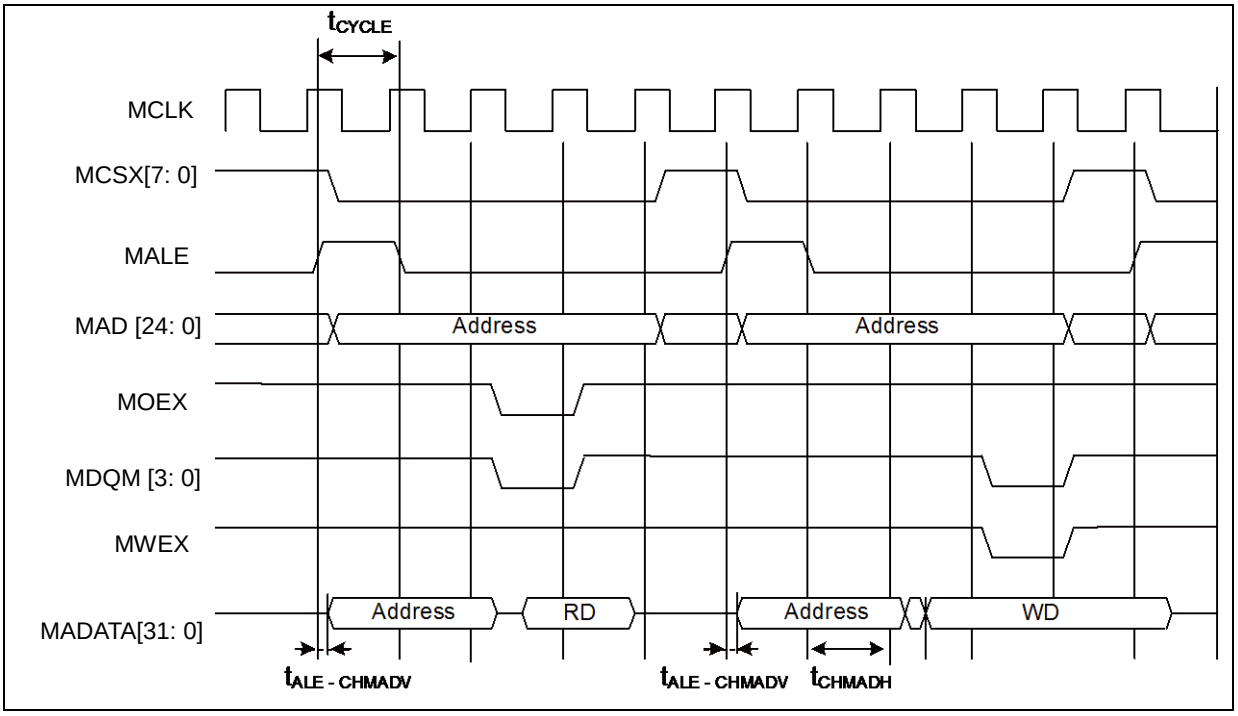
Multiplexed Bus Access Asynchronous SRAM Mode

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Multiplexed address delay time	$t_{ALE-CHMADV}$	MALE, MAD[24: 0]	-	0	10	ns	
Multiplexed address hold time	t_{CHMADH}		-	MCLK×n+0	MCLK×n+10	ns	

Note:

- *When the external load capacitance C_L = 30 pF (m = 0 to 15, n = 1 to 16)*

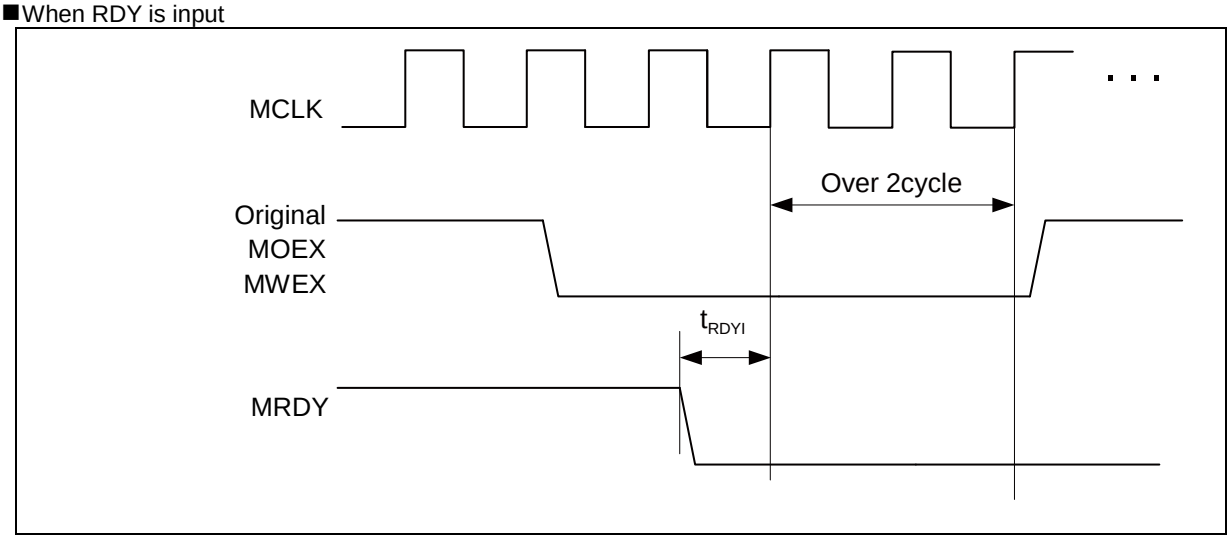


External Ready Input Timing

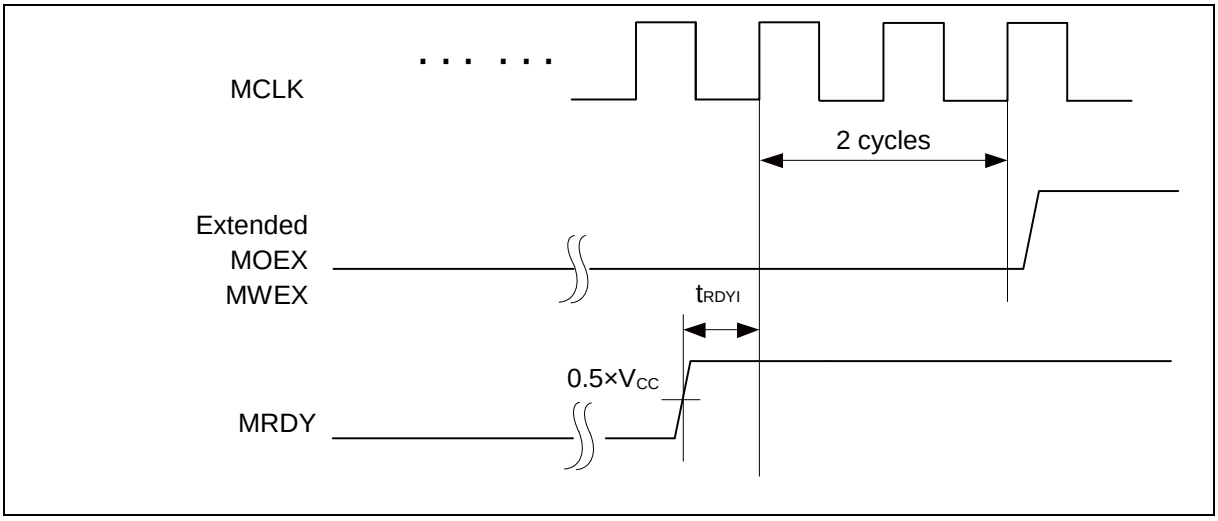
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

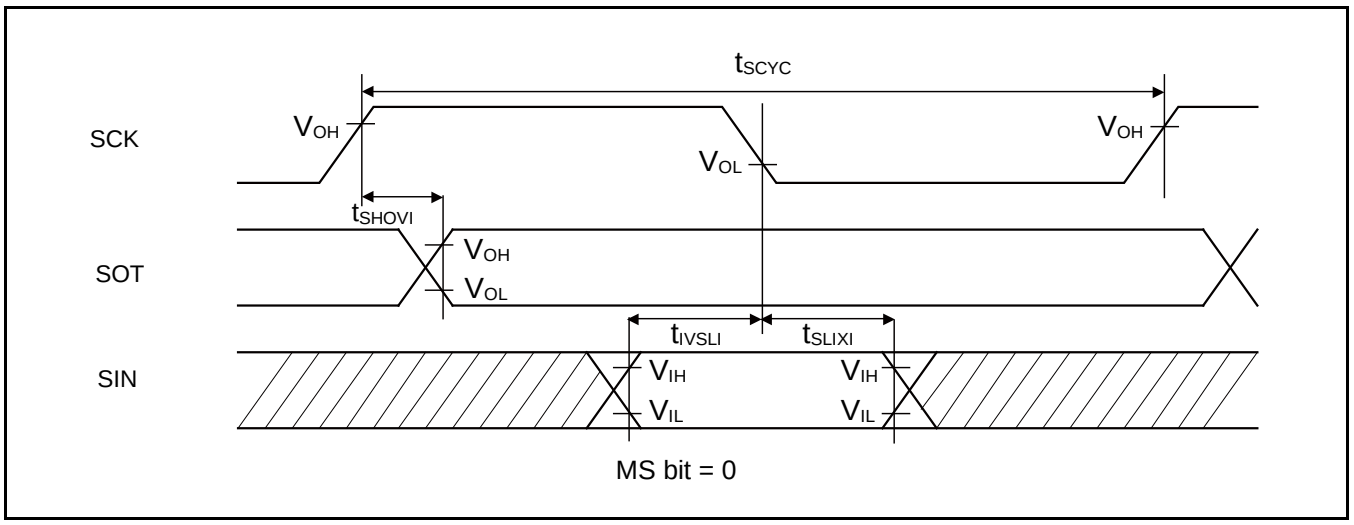
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
MCLK↑ MRDY input setup time	t_{RDYI}	MCLK, MRDY	-	19	-	ns	

■When RDY is input

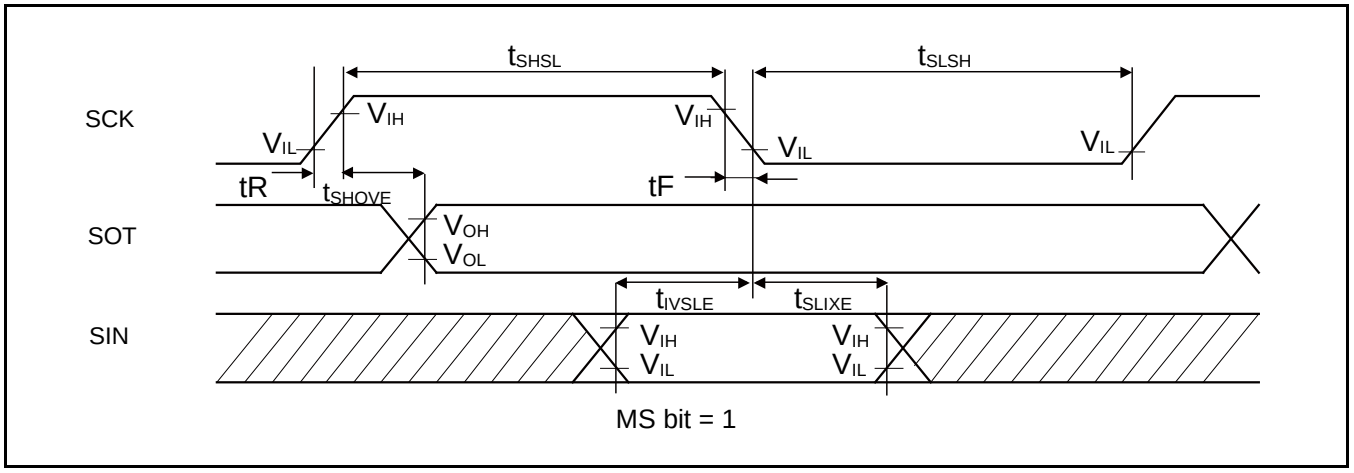


■When RDY is released





MS bit = 0



MS bit = 1

High-Speed Synchronous Serial (SPI = 0, SCINV = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↑→SOT delay time	t_{SHOVI}	SCKx, SOTx		- 10	+ 10	- 10	+ 10	ns
SIN→SCK↓ setup time	t_{IVSLI}	SCKx, SINx		14 12.5*	-	12.5	-	ns
SCK↓→SIN hold time	t_{SLIXI}	SCKx, SINx		5	-	5	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 5	-	$2t_{CYCP}$ - 5	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↑→SOT delay time	t_{SHOVE}	SCKx, SOTx		-	15	-	15	ns
SIN→SCK↓ setup time	t_{IVSLE}	SCKx, SINx		5	-	5	-	ns
SCK↓→SIN hold time	t_{SLIXE}	SCKx, SINx		5	-	5	-	ns
SCK fall time	t_F	SCKx		-	5	-	5	ns
SCK rise time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.*
- *These characteristics only guarantee the following pins:*

  No chip select: SIN4_0, SOT4_0, SCK4_0

  Chip select: SIN6_0, SOT6_0, SCK6_0, SCS60_0, SCS61_0, SCS62_0, SCS63_0
- *When the external load capacitance C_L = 30 pF. (For *, when C_L = 10 pF)*

High-Speed Synchronous Serial (SPI = 1, SCINV = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↑→SOT delay time	t_{SHOVI}	SCKx, SOTx		- 10	+ 10	- 10	+ 10	ns
SIN→SCK↓ setup time	t_{IVSLI}	SCKx, SINx		14 12.5*	-	12.5	-	ns
SCK↓→SIN hold time	t_{SLIXI}	SCKx, SINx		5	-	5	-	ns
SOT→SCK↓ delay time	t_{SOVLI}	SCKx, SOTx		$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 5	-	$2t_{CYCP}$ - 5	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↑→SOT delay time	t_{SHOVE}	SCKx, SOTx		-	15	-	15	ns
SIN→SCK↓ setup time	t_{IVSLE}	SCKx, SINx		5	-	5	-	ns
SCK↓→SIN hold time	t_{SLIXE}	SCKx, SINx		5	-	5	-	ns
SCK fall time	t_F	SCKx		-	5	-	5	ns
SCK rise time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.*
- *These characteristics only guarantee the following pins:*

  No chip select: SIN4_0, SOT4_0, SCK4_0

  Chip select: SIN6_0, SOT6_0, SCK6_0, SCS60_0, SCS61_0, SCS62_0, SCS63_0
- *When the external load capacitance C_L = 30 pF. (for *, when C_L = 10 pF)*

12.4.13 External Input Timing

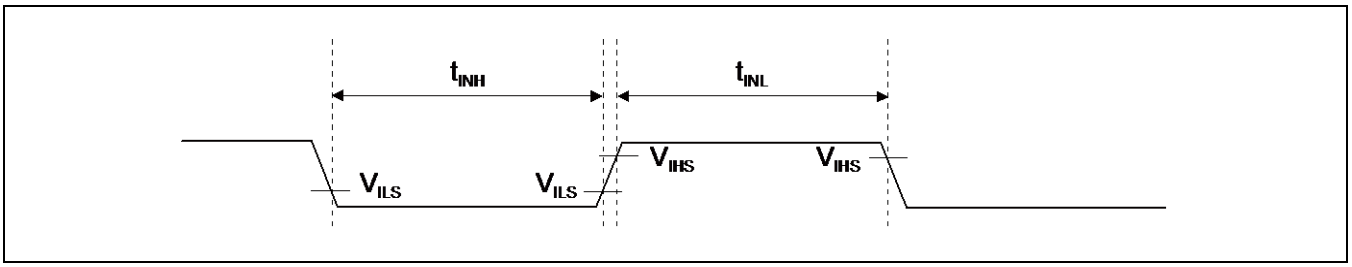
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{INH}, t_{INL}	ADTGx	-	$2t_{CYCP}$*1	-	ns	A/D converter trigger input
		FRCKx					Free-run timer input clock
		ICxx					Input capture
		DTTIxX	-	$2t_{CYCP}$*1	-	ns	Waveform generator
		INT00 to INT31, NMIX	-	$2t_{CYCP}$ + 100*1	-	ns	External interrupt, NMI
				500*2	-	ns	
		WKUPx	-	500*3	-	ns	Deep standby wake up

1: t_{CYCP} indicates the APB bus clock cycle time except stop when in Stop mode, in Timer mode. For more information about the APB bus number to which the A/D converter, multi-function timer, and external interrupt are connected, see 8. Block Diagram in this data sheet.

2: When in Stop mode, in Timer mode

3: When in Deep Standby RTC mode, in Deep Standby Stop mode



12.4.16 SD Card Interface Timing

Default-Speed Mode

■Clock CLK (All values are referenced to V_{IH} and V_{IL} transition points)

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Clock frequency Data Transfer Mode	f_{PP}	S_CLK	C_{CARD} ≤ 10 pF (1card)	0	25	MHz
Clock frequency Identification Mode	f_{OD}	S_CLK		0/100	400	kHz
Clock low time	t_{WL}	S_CLK		10	-	ns
Clock high time	t_{WH}	S_CLK		10	-	ns
Clock rise time	t_{TLH}	S_CLK		-	10	ns
Clock fall time	t_{THL}	S_CLK		-	10	ns

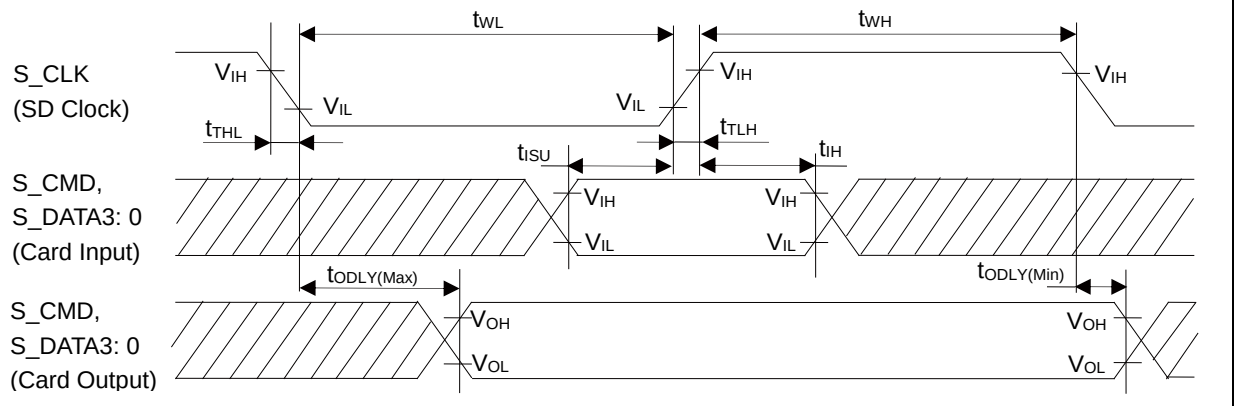
* 0 Hz means to stop the clock. The given minimum frequency range is for cases where a continuous clock is required.

■Card Inputs CMD, DAT (referenced to Clock CLK)

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Input set-up time	t_{ISU}	S_CMD, S_DATA3: 0	C_{CARD} ≤ 10 pF (1card)	5	-	ns
Input hold time	t_{IH}	S_CMD, S_DATA3: 0		5	-	ns

■Card Outputs CMD, DAT (referenced to Clock CLK)

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Output Delay time during Data Transfer Mode	t_{ODLY}	S_CMD, S_DATA3: 0	C_{CARD} ≤ 40 pF (1card)	0	14	ns
Output Delay time during Identification Mode	t_{ODLY}	S_CMD, S_DATA3: 0		0	50	ns



Default-Speed Mode

Notes:

- *The Card Input corresponds to the Host Output and the Card Output corresponds to the Host Input because this model is the Host.*
- *For more information about clock frequency (f_{PP}), see Chapter 15: SD card Interface in FM4 Family Peripheral Manual Main Part (002-04856).*

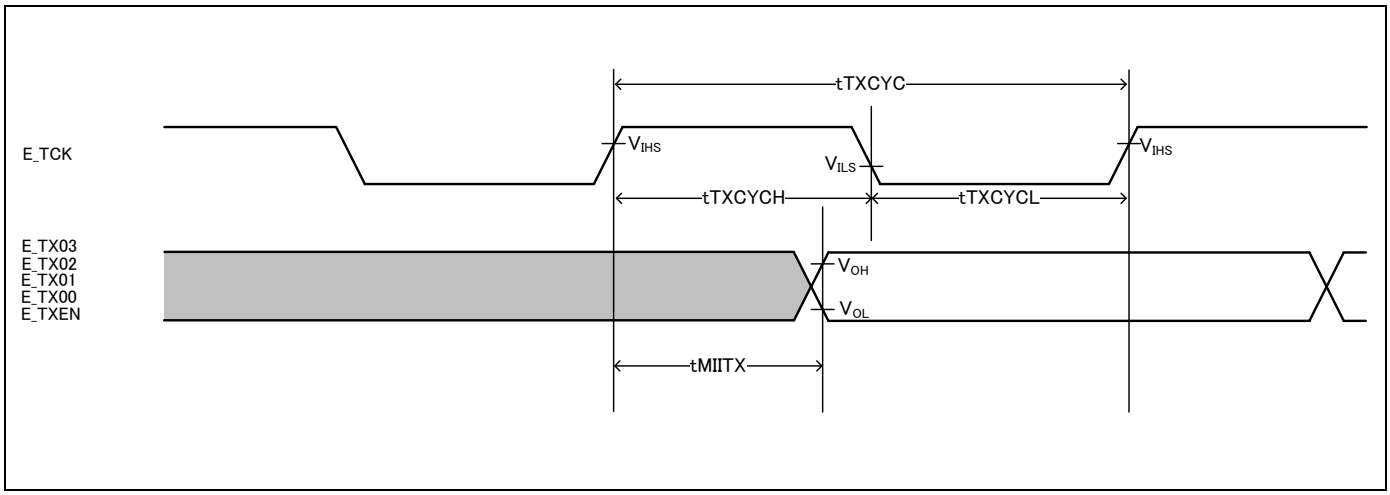
MII Transmission (100 Mbps/10 Mbps)

($ETHV_{CC}$ = 3.0V to 3.6V, 4.5V to 5.5V*1, V_{SS} = 0V, C_L = 25 pF)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Transmission clock Cycle time*2	t_{TXCYC}	E_TCK	100 Mbps 40 ns (typical)	-	-	ns
			100 Mbps 400 ns (typical)	-	-	ns
Transmission clock High-pulse-width duty cycle	t_{TXCYCH}	E_TCK	t_{TXCYCH}/t_{TXCYC}	35	65	%
Transmission clock Low-pulse-width duty cycle	t_{TXCYCL}	E_TCK	t_{TXCYCL}/t_{TXCYC}	35	65	%
TXCK ↑ → Transmitted data delay time	t_{MIITX}	E_TX03, E_TX02, E_TX01, E_TX00, E_TXEN	-	-	24	ns

*1: When ETHV = 4.5V to 5.5V, it is recommended to add a series resistor at the output pin to suppress the output current.

*2: The transmission clock is fixed to 25 MHz or 2.5 MHz in the MII specifications. The clock accuracy should meet the PHY-device specifications.



12.11 Standby Recovery Time

12.11.1 Recovery Cause: Interrupt/WKUP

The time from the interrupt occurring to the time of program operation start is shown.

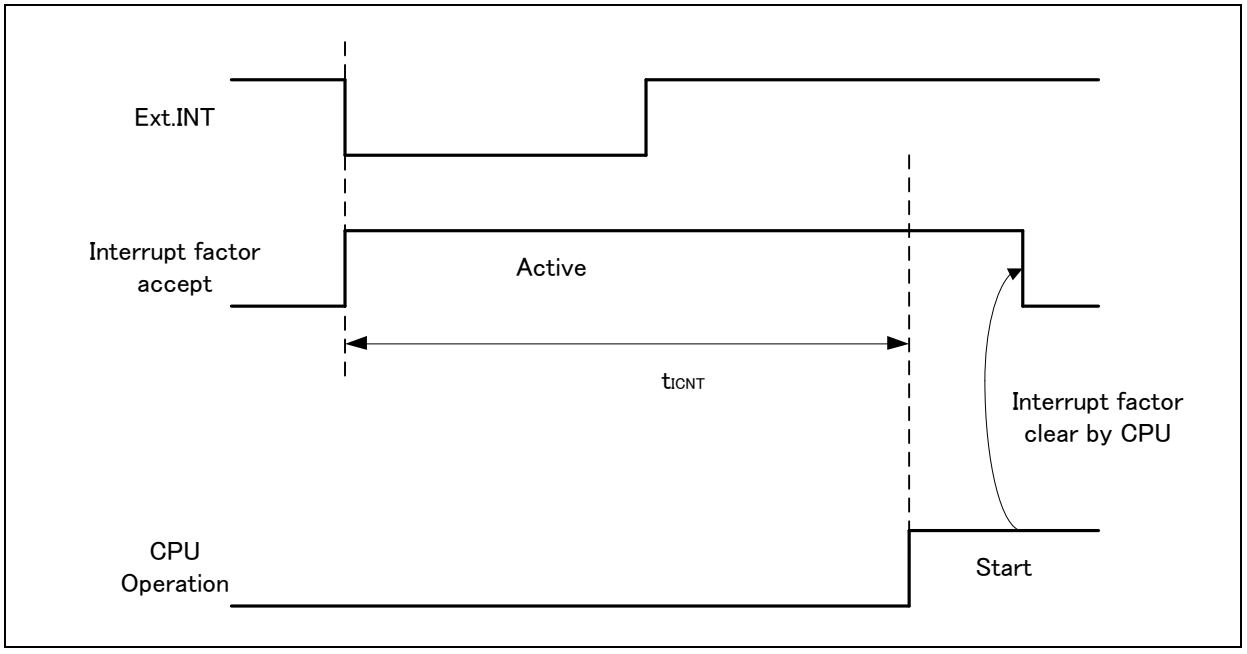
Recovery Count Time

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
Sleep mode	t_{ICNT}	HCLK×1		µs	
High-speed CR Timer mode Main Timer mode PLL Timer mode		40	80	µs	
Low-speed CR Timer mode		450	900	µs	
Sub Timer mode		896	1136	µs	
RTC mode Stop mode (High-speed CR/Main/PLL Run mode return)		316	581	µs	
RTC mode Stop mode (Low-speed CR/sub Run mode return)		270	540	µs	
Deep Standby RTC mode with RAM retention		365	667	µs	without RAM retention
Deep Standby Stop mode with RAM retention		365	667	µs	with RAM retention

*: The maximum value depends on the built-in CR accuracy.

Example of Standby Recovery Operation (when in External Interrupt Recovery*)



*: External interrupt is set to detecting fall edge.

13. Ordering Information

Part Number	Flash	RAM	Crypto	Package
S6E2C28H0AGV2000A	1 MB	128 KB	N/A	Plastic LQFP (0.5 mm pitch), 144 pin (LQS144)
S6E2C29H0AGV2000A	1.5 MB	192 KB	N/A	
S6E2C2AH0AGV2000A	2 MB	256 KB	N/A	
S6E2C28HHAGV2000A	1 MB	128 KB	Yes	
S6E2C29HHAGV2000A	1.5 MB	192 KB	Yes	
S6E2C2AHHAGV2000A	2 MB	256 KB	Yes	
S6E2C28J0AGV2000A	1 MB	128 KB	N/A	Plastic LQFP (0.5 mm pitch), 176 pin (LQP176)
S6E2C29J0AGV2000A	1.5 MB	192 KB	N/A	
S6E2C2AJ0AGV2000A	2 MB	256 KB	N/A	
S6E2C28JHAGV2000A	1 MB	128 KB	Yes	
S6E2C29JHAGV2000A	1.5 MB	192 KB	Yes	
S6E2C2AJHAGV2000A	2 MB	256 KB	Yes	
S6E2C28J0AGB1000A	1 MB	128 KB	N/A	Plastic FBGA (0.8 mm pitch), 192 pin (LBE192)
S6E2C29J0AGB1000A	1.5 MB	192 KB	N/A	
S6E2C2AJ0AGB1000A	2 MB	256 KB	N/A	
S6E2C28JHAGB1000A	1 MB	128 KB	Yes	
S6E2C29JHAGB1000A	1.5 MB	192 KB	Yes	
S6E2C2AJHAGB1000A	2 MB	256 KB	Yes	
S6E2C28L0AGL2000A	1 MB	128 KB	N/A	Plastic LQFP (0.4 mm pitch), 216 pin (LQQ216)
S6E2C29L0AGL2000A	1.5 MB	192 KB	N/A	
S6E2C2AL0AGL2000A	2 MB	256 KB	N/A	
S6E2C28LHAGL2000A	1 MB	128 KB	Yes	
S6E2C29LHAGL2000A	1.5 MB	192 KB	Yes	
S6E2C2ALHAGL2000A	2 MB	256 KB	Yes	

				S6E2C28LHAGL2000A, S6E2C29LHAGL2000A, S6E2C2ALHAGL2000A Deleted Baud rate spec for High-Speed Synchronous Serial in “12.4.12 CSIO(SPI) Timing”(Page 146-152) Modified the expression of the “Built-in CR” and add Note in the “1. Product Lineup”(Page 9) Modified typo(SCLKx_0 -> SCKx_0)(Page 130, 132, 134, 136) Change the name from “USB Function” to “USB Device” (Page 1, 8, 59) Added Maximum Access size in “Features”(Page 1) Updated IO circuit (type A) (Page 63)