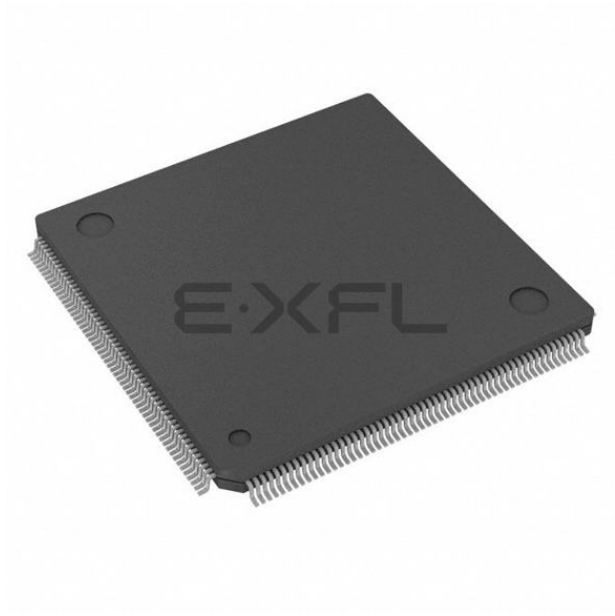

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CSIO, EBI/EMI, Ethernet, I²C, LINbus, SD, SPI, UART/USART, USB
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	190
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	216-LQFP
Supplier Device Package	216-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2c28l0agl2000a

Multi-function Serial Interface (Max 16 channels)

- Separate 64 byte receive and transmit FIFO buffers for channels 0 to 7.
- Operation mode is selectable for each channel from the following:
  - UART
  - CSIO (SPI)
  - LIN
  - I^2C
- UART
  - Full-duplex double buffer
  - Selection with or without parity supported
  - Built-in dedicated baud rate generator
  - External clock available as a serial clock
  - Various error detect functions available (parity errors, framing errors, and overrun errors)
- CSIO (SPI)
  - Full-duplex double buffer
  - Built-in dedicated baud rate generator
  - Overrun error detect function available
  - Serial chip select function (ch 6 and ch 7 only)
  - Supports high-speed SPI (ch 4 and ch 6 only)
  - Data length 5 to 16-bit
- LIN
  - LIN protocol Rev.2.1 supported
  - Full-duplex double buffer
  - Master/slave mode supported
  - LIN break field generation (can change to 13- to 16-bit length)
  - LIN break delimiter generation (can change to 1- to 4-bit length)
  - Various error detect functions available (parity errors, framing errors, and overrun errors)
- I^2C
  - Standard mode (Max 100 kbps)/Fast mode (Max 400 kbps) supported
  - Fast mode Plus (Fm+) (Max 1000 kbps, only for ch 3 = ch A and ch 7 = ch B) supported

DMA Controller (Eight channels)

DMA controller has an independent bus, so the CPU and DMA controller can process simultaneously.

- Eight independently configured and operated channels
- Transfer can be started by software or request from the built-in peripherals
- Transfer address area: 32-bit (4 GB)
- Transfer mode: Block transfer/Burst transfer/Demand transfer
- Transfer data type: bytes/half-word/word
- Transfer block count: 1 to 16
- Number of transfers: 1 to 65536

DSTC (Descriptor System data Transfer Controller; 256 Channels)

The DSTC can transfer data at high-speed without going via the CPU. The DSTC adopts the descriptor system and, following the specified contents of the descriptor that has already been constructed on the memory, can access directly the memory/peripheral device and perform the data-transfer operation.

It supports the software activation, the hardware activation, and the chain activation functions.

A/D Converter (Max 32 channels)

- 12-bit A/D Converter
  - Successive approximation type
  - Built-in three units
  - Conversion time: 0.5 µs at 5 V
  - Priority conversion available (priority at two levels)
  - Scanning conversion mode
  - Built-in FIFO for conversion data storage (for SCAN conversion: 16 steps, for priority conversion: 4 steps)

D/A Converter (Max 2 Channels)

- R-2R type
- 12-bit resolution

Base Timer (Max 16 Channels)

Operation mode is selected from the following for each channel:

- 16-bit PWM timer
- 16-bit PPG timer
- 16-/32-bit reload timer
- 16-/32-bit PWC timer

General Purpose I/O Port

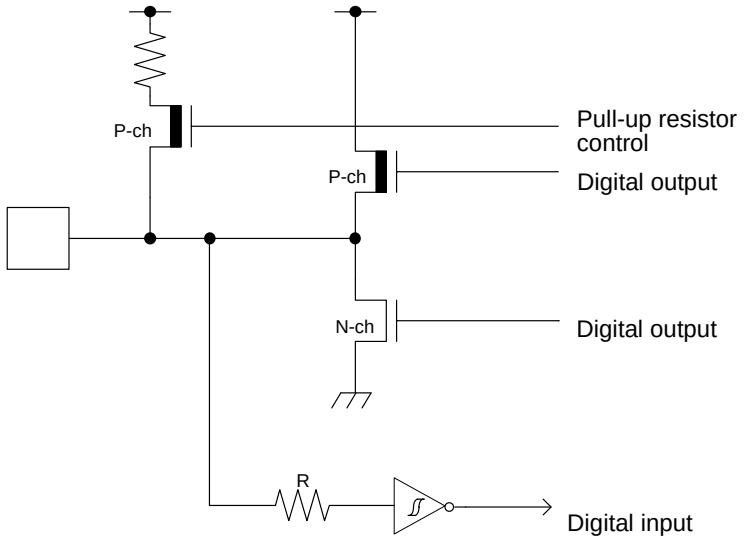
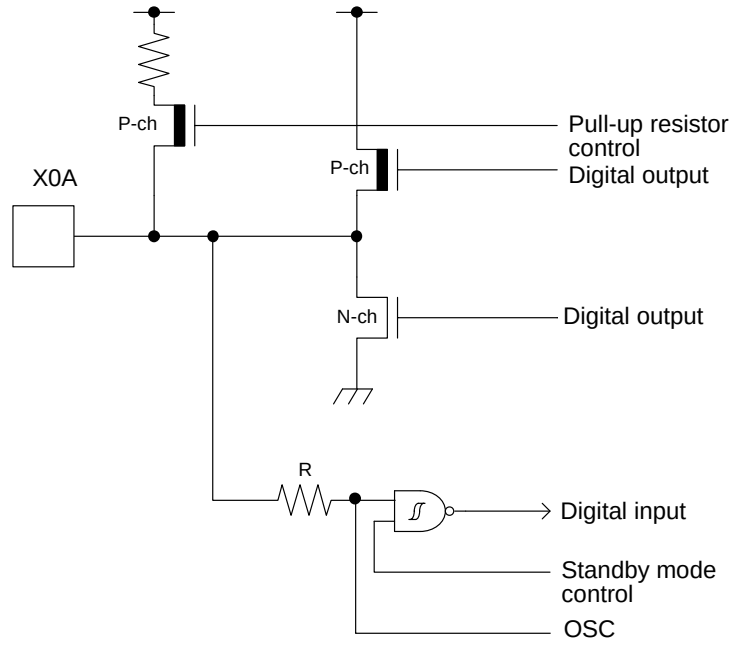
This series can use its pins as general purpose I/O ports when they are not used for external bus or peripherals; moreover, the port relocate function is built in. It can set the I/O port to which the peripheral function can be allocated.

- Capable of pull-up control per pin
- Capable of reading pin level directly
- Built-in port-relocate function
- Up to 120 high-speed general-purpose I/O ports in 144 pin package
- Some pins 5V tolerant I/O.
  See 4. Pin Descriptions and 5. I/O Circuit Type for the corresponding pins.

Table of Contents

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Debugger	SWCLK	Serial wire debug interface clock input pin	165	135	111	A12
	SWDIO	Serial wire debug interface data input/ output pin	167	137	113	B12
	SWO	Serial wire viewer output pin	168	138	114	B11
	TCK	JTAG test clock input pin	165	135	111	A12
	TDI	JTAG test data input pin	166	136	112	C12
	TDO	JTAG debug data output pin	168	138	114	B11
	TMS	JTAG test mode state input/output pin	167	137	113	B12
	TRACECLK	Trace CLK output pin of ETM/HTM	131	107	87	H12
	TRACED0	Trace data output pin of ETM/ Trace data output pin of HTM	132	108	88	H14
	TRACED1		133	109	89	G14
	TRACED2		134	110	90	H13
	TRACED3		135	111	91	H11
	TRACED4	Trace data output pin of HTM	138	112	-	G13
	TRACED5		139	113	-	F14
	TRACED6		140	114	-	G12
	TRACED7		141	115	-	G11
	TRACED8		119	-	-	-
	TRACED9		120	-	-	-
	TRACED10		121	-	-	-
	TRACED11		122	-	-	-
	TRACED12		148	-	-	-
	TRACED13		149	-	-	-
	TRACED14		150	-	-	-
	TRACED15		151	-	-	-
	TRSTX	JTAG test reset Input pin	164	134	110	B13

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Multi-Function Serial 5	SIN5_0	Multi-function serial interface ch 5 input pin	147	121	97	F13
	SIN5_1		170	140	-	D11
	SOT5_0 (SDA5_0)	Multi-function serial interface ch 5 output pin. This pin operates as SOT5 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA5 when it is used in an I²C (operation mode 4).	146	120	96	F12
	SOT5_1 (SDA5_1)		171	141	-	B10
	SCK5_0 (SCL5_0)	Multi-function serial interface ch 5 clock I/O pin. This pin operates as SCK5 when it is used in a CSIO (operation mode 2) and as SCL5 when it is used in an I²C (operation mode 4).	145	119	95	F11
	SCK5_1 (SCL5_1)		172	142	-	C10
	CTS5_0	Multi-function serial interface ch 5 CTS input pin	144	118	94	F10
	CTS5_1		173	143	-	D10
	RTS5_0	Multi-function serial interface ch 5 RTS output pin	143	117	93	G9
	RTS5_1		174	144	-	B9
Multi-Function Serial 6	SIN6_0	Multi-function serial interface ch 6 input pin	96	79	63	L10
	SIN6_1		117	97	81	K14
	SOT6_0 (SDA6_0)	Multi-function serial interface ch 6 output pin. This pin operates as SOT6 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA6 when it is used in an I²C (operation mode 4).	97	80	64	K10
	SOT6_1 (SDA6_1)		118	98	82	K11
	SCK6_0 (SCL6_0)	Multi-function serial interface ch 6 clock I/O pin. This pin operates as SCK6 when it is used in a CSIO (operation mode 2) and as SCL6 when it is used in an I²C (operation mode 4).	98	81	65	M10
	SCK6_1 (SCL6_1)		126	102	-	J10
	SCS60_0	Multi-function serial interface ch 6 chip select 0 input/output pin	99	82	66	N11
	SCS60_1		127	103	-	J9
	SCS61_0	Multi-function serial interface ch 6 chip select1 input/output pin	100	83	67	M11
	SCS61_1		128	104	-	H10
	SCS62_0	Multi-function serial interface ch 6 chip select2 input/output pin	79	64	-	K6
	SCS62_1		129	105	-	J14
	SCS63_0	Multi-function serial interface ch 6 chip select3 input/output pin	78	63	-	K5
	SCS63_1		119	-	-	-

Type	Circuit	Remarks
O		・ CMOS level output ・ CMOS level hysteresis input ・ 5V tolerant ・ Pull-up resistor control ・ Pull-up resistor: approximately 50 kΩ ・ I_{OH} = -4 mA, I_{OL} = 4 mA ・ Available to control of PZR register (pseudo-open drain control) ・ For PZR registers, refer to GPIO in the “FM4 Family Peripheral Manual Main Part (002-04856)”. ・ For I/O setting, refer to VBAT Domain in the "FM4 Family Peripheral Manual Main Part (002-04856).”
P		・ CMOS level output ・ CMOS level hysteresis input ・ Pull-up resistor control ・ Pull-up resistor: approximately 50 kΩ ・ I_{OH} = -4 mA, I_{OL} = 4 mA ・ For I/O setting, refer to VBAT Domain in the "FM4 Family Peripheral Manual Main Part (002-04856).”

Notes on Power-on

Turn power on/off in the following order or at the same time. The device operates normally after all power on.

VBAT only Power-on is possible when VBAT and VCC turns Power-on and Hibernation control is setting and then VCC turns Power-off. About Hibernation control, see Chapter 7-2: VBAT Domain(B) in FM4 Family Peripheral Manual Main Part(002-04856).

Turning on:	VBAT → VCC → USBVCC0
	VBAT → VCC → USBVCC1
	VBAT →VCC →ETHVCC
	VCC → AVCC → AVRH
Turning off:	AVRH → AVCC → VCC
	ETHVCC → VCC → VBAT
	USBVCC1 → VCC → VBAT
	USBVCC0 → VCC → VBAT

Serial Communication

There is a possibility of receiving incorrect data as a result of noise or other issues introduced by the serial communication. Take care to design the printed circuit board to minimize noise.

Consider the case of introducing error as a result of noise, perform error detection such as by applying a checksum of data at the end. If an error is detected, retransmit the data.

Differences in Characteristics within the Product Line

The electric characteristics including power consumption, ESD, latch-up, noise, and oscillation differ among members of the product line because chip layout and memory structures are not the same; for example, different sizes, flash versus ROM, etc. If you are switching to a different product of the same series, please make sure to evaluate the electric characteristics.

Pull-Up Function of 5 V Tolerant I/O

Please do not input the signal more than VCC voltage at the time of Pull-Up function use of 5 V tolerant I/O.

Pin Doubled As Debug Function

The pin doubled as TDO/TMS/TDI/TCK/TRSTX, SWO/SWDIO/SWCLK should be used as output only. Do not use as input.

12. Electrical Characteristics

12.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage *1,*2	V_{CC}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Power supply voltage (for USB) *1,*3	$USBV_{CC}0$	V_{SS} - 0.5	V_{SS} + 6.5	V	
Power supply voltage (for USB) *1,*3	$USBV_{CC}1$	V_{SS} - 0.5	V_{SS} + 6.5	V	
Power supply voltage (for Ethernet-MAC) *1, *4	$ETHV_{CC}$	V_{SS} - 0.5	V_{SS} + 6.5	V	
Power supply voltage (VBAT) *1 ,*5	V_{BAT}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Analog power supply voltage *1 ,*6	AV_{CC}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Analog reference voltage *1 ,*6	AVRH	V_{SS} - 0.5	V_{SS} + 6.5	V	
Input voltage *1	V_I	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 6.5 V)	V	Except for USB and Ethernet-MAC pin
		V_{SS} - 0.5	$USBV_{CC}0$ + 0.5 (≤ 6.5 V)	V	USB ch 0 pin
		V_{SS} - 0.5	$USBV_{CC}1$ + 0.5 (≤ 6.5 V)	V	USB ch 1 pin
		V_{SS} - 0.5	$ETHV_{CC}$ + 0.5 (≤ 6.5 V)	V	Ethernet-MAC Pin
		V_{SS} - 0.5	V_{SS} + 6.5	V	5V tolerant
Analog pin input voltage *1	V_{IA}	V_{SS} - 0.5	AV_{CC} + 0.5 (≤ 6.5 V)	V	
Output voltage *1	V_O	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 6.5 V)	V	
L level maximum output current *7	I_{OL}	-	10	mA	4 mA type
			20	mA	8 mA type
			20	mA	10 mA type
			20	mA	12 mA type
			22.4	mA	I^2C Fm+
L level average output current *8	I_{OLAV}	-	4	mA	4 mA type
			8	mA	8 mA type
			10	mA	10 mA type
			12	mA	12 mA type
			20	mA	I^2C Fm+
L level total maximum output current	$\sum I_{OL}$	-	100	mA	
L level total maximum output current *9	$\sum I_{OLAV}$	-	50	mA	
H level maximum output current *7	I_{OH}	-	- 10	mA	4 mA type
			-20	mA	8 mA type
			- 20	mA	10 mA type
			- 20	mA	12 mA type
H level average output current *8	I_{OHAV}	-	- 4	mA	4 mA type
			-8	mA	8 mA type
			- 10	mA	10 mA type
			- 12	mA	12 mA type
H level total maximum output current	$\sum I_{OH}$	-	- 100	mA	
H level total average output current *9	$\sum I_{OHAV}$	-	- 50	mA	
Power consumption	P_D	-	200	mW	
Storage temperature	T_{STG}	- 55	+ 150	°C	

*1: These parameters are based on the condition that $V_{SS} = AV_{SS} = 0.0$ V.

*2: V_{CC} must not drop below V_{SS} - 0.5 V.

*3: $USBV_{CC}0$, $USBV_{CC}1$ must not drop below V_{SS} - 0.5 V.

*4: $ETHV_{CC}$ must not drop below V_{SS} - 0.5 V.

*5: V_{BAT} must not drop below V_{SS} - 0.5 V.

Calculation Method of Power Dissipation (Pd)

The power dissipation is shown in the following formula.

$$Pd = V_{CC} \times I_{CC} + \Sigma (I_{OL} \times V_{OL}) + \Sigma ((V_{CC}-V_{OH}) \times (-I_{OH}))$$

I_{OL}: L level output current
I_{OH}: H level output current
V_{OL}: L level output voltage
V_{OH}: H level output voltage

I_{CC} is the current drawn by the device.
It can be analyzed as follows.

$$I_{CC} = I_{CC}(INT) + \Sigma I_{CC}(IO)$$

I_{CC} (INT): Current drawn by internal logic and memory, etc. through the regulator

ΣI_{CC} (IO): Sum of current (I/O switching current) drawn by the output pin

For I_{CC} (INT), it can be anticipated by (1) Current Rating in 12.3. DC Characteristics (This rating value does not include I_{CC} (IO) for a value at pin fixed).
For I_{CC} (IO), it depends on system used by customers.
The calculation formula is shown below.

$$I_{CC}(IO) = (C_{INT} + C_{EXT}) \times V_{CC} \times f_{SW}$$

C_{INT}: Pin internal load capacitance
C_{EXT}: External load capacitance of output pin
f_{SW}: Pin switching frequency

Parameter	Symbol	Conditions	Capacitance Value
Pin internal load capacitance	C_{INT}	4 mA type	1.93 pF
		8 mA type	3.45 pF
		12 mA type	3.42 pF

Calculate I_{CC} (Max) as follows when the power dissipation can be evaluated by yourself:

Measure current value I_{CC} (Typ) at normal temperature (+25°C).

Add maximum leakage current value I_{CC} (leak_max) at operating on a value in (1).

$$I_{CC}(Max) = I_{CC}(Typ) + I_{CC}(leak\_max)$$

Parameter	Symbol	Conditions	Current Value
Maximum leakage current at operating	I_{CC} (leak_max)	T_J = +125°C	79.2 mA
		T_J = +105°C	39.4 mA
		T_J = +85°C	26.5 mA

12.3 DC Characteristics

12.3.1 Current Rating

Table 12-1 Typical and Maximum Current Consumption in Normal Operation (PLL), Code Running from Flash Memory (Flash Accelerator Mode and Trace Buffer Function Enabled)

Parameter	Symbol	Pin Name	Conditions		Frequency*4	Value		Unit	Remarks
						Typ*1	Max*2		
Power supply current	I_{CC}	VCC	Normal operation *7,*8 (PLL)	*5	200 MHz	117	224	mA	*3 When all peripheral clocks are on
					192 MHz	113	219	mA	
					180 MHz	106	211	mA	
				*6	160 MHz	95	197	mA	
					144 MHz	86	186	mA	
					120 MHz	73	169	mA	
					100 MHz	61	155	mA	
					80 MHz	50	140	mA	
					60 MHz	39	126	mA	
					40 MHz	27	112	mA	
					20 MHz	16	97	mA	
					8 MHz	8.7	88.9	mA	
					4 MHz	6.4	86.1	mA	
				*5	200 MHz	71	168	mA	*3 When all peripheral clocks are off
					192 MHz	68	165	mA	
					180 MHz	64	159	mA	
				*6	160 MHz	58	151	mA	
					144 MHz	52	144	mA	
					120 MHz	44	134	mA	
					100 MHz	38	126	mA	
					80 MHz	31	117	mA	
					60 MHz	24	109	mA	
					40 MHz	17	100	mA	
					20 MHz	10	91	mA	
					8 MHz	6.3	86.1	mA	
					4 MHz	5.0	84.5	mA	

*1: T_A = +25°C, V_{CC} = 3.3 V

*2: T_J = +125°C, V_{CC} = 5.5 V

*3: When all ports are fixed

*4: Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK

*5: When stopping flash accelerator mode and trace buffer function (FRWTR.RWT = 11, FBFCR.BE = 1)

*6: When stopping flash accelerator mode and trace buffer function (FRWTR.RWT = 10, FBFCR.BE = 1)

*7: Firmware being executed during data collection for this table is not being accessed from the MainFlash memory."

*8: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

Table 12-10 Typical and Maximum Current Consumption in Low-voltage Detection Circuit, Main Flash Memory Write/erase

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Low-voltage detection circuit (LVD) power supply current	I_{CCLVD}	VCC	At operation	-	4	7	µA	For occurrence of interrupt
MainFlash memory write/erase current	$I_{CCFLASH}$		At write/erase	-	13.4	15.9	mA	*1

*1: When programming or erase in flash memory, Flash Memory Write/Erase current ($I_{CCFLASH}$) is added to the Power supply current (I_{CC}).

Peripheral Current Dissipation

Clock system	Peripheral	Unit	Frequency (MHz)			Unit	Remarks
			50	100	200		
HCLK	GPIO	All ports	0.39	0.81	1.56	mA	
	DMAC	-	0.99	1.97	3.82		
	DSTC	-	0.73	1.49	2.86		
	External bus I/F	-	0.25	0.48	0.97		
	SD card I/F	-	0.74	1.47	2.90		
	USB	1 ch	0.48	0.95	1.89		
	Ethernet-MAC	-	1.85	3.63	7.20		
	I^2S	-	0.51	1.02	1.99		
	High-Speed Quad SPI	-	0.48	0.97	1.49		
	Programmable CRC	-	0.05	0.10	0.22		
PCLK1	Base timer	4 ch	0.21	0.42	0.83	mA	
	Multi-functional timer/PPG	1 unit/4 ch	0.83	1.65	3.25		
	Quadrature position/revolution counter	1 unit	0.07	0.13	0.27		
	A/D converter	1 unit	0.31	0.60	1.17		
PCLK2	Multi-function serial	1 ch	0.41	0.81	-	mA	

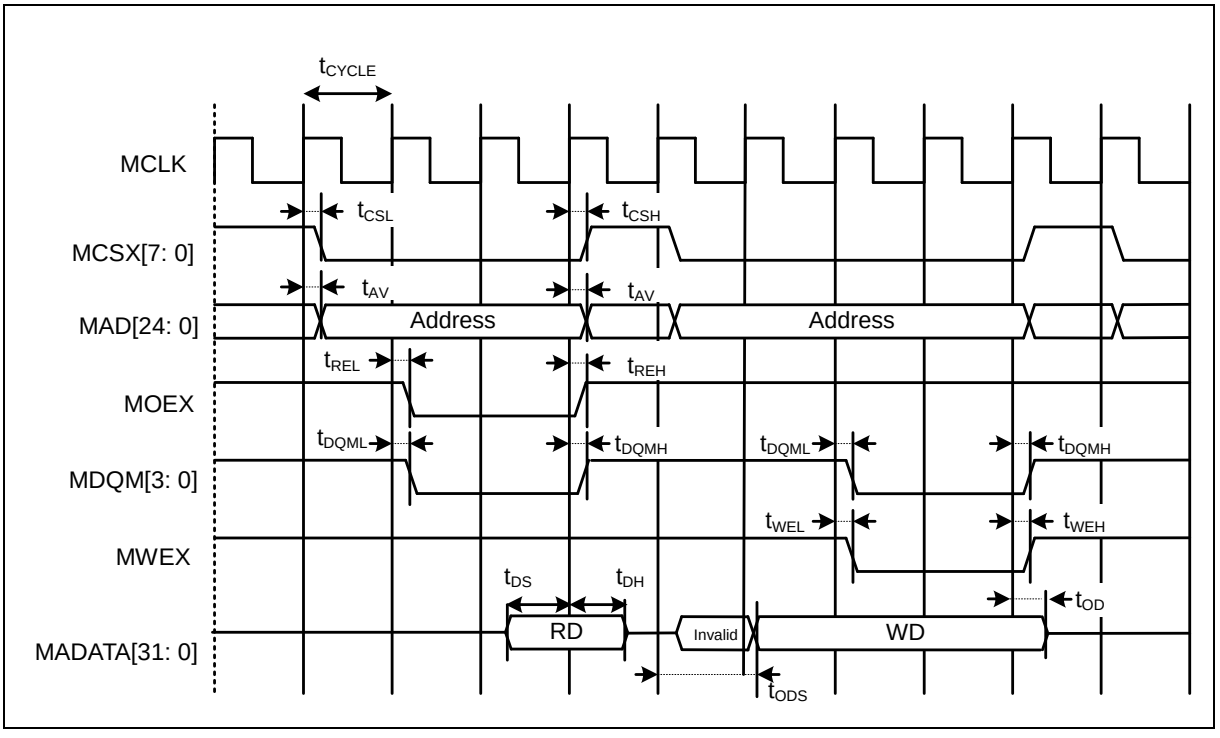
Separate Bus Access Synchronous SRAM Mode

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

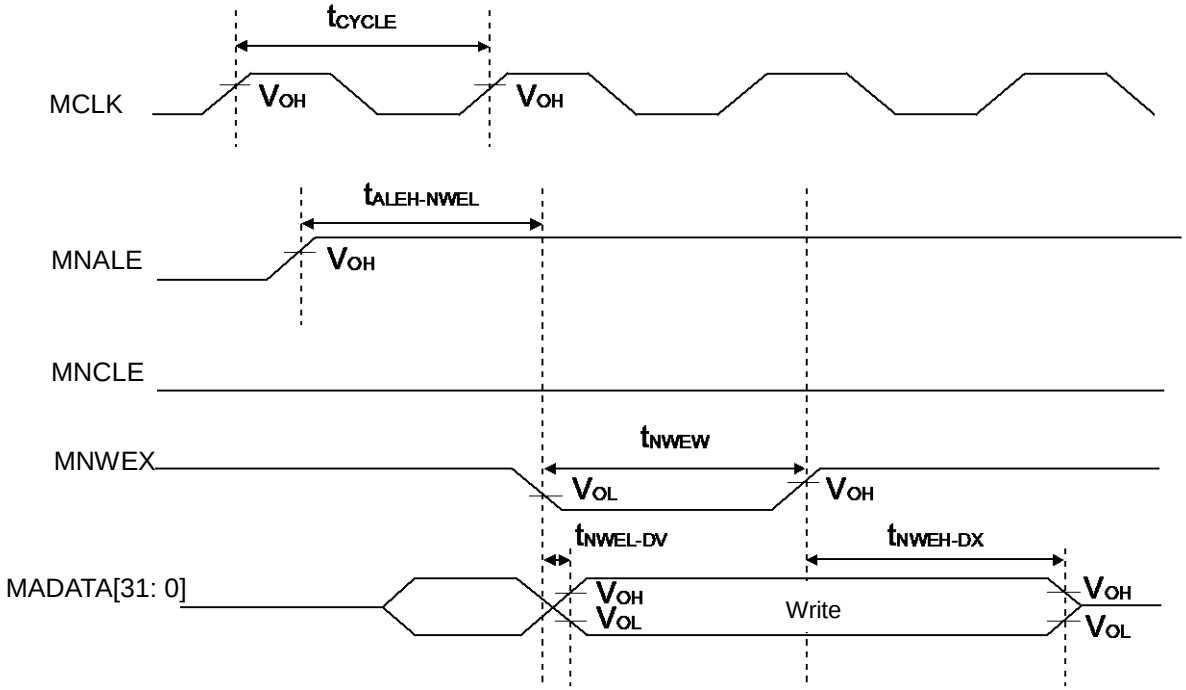
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Address delay time	t_{AV}	MCLK, MAD[24: 0]	-	1	9	ns	
MCSX delay time	t_{CSL}	MCLK, MCSX[7: 0]	-	1	9	ns	
	t_{CSH}		-	1	9	ns	
MOEX delay time	t_{REL}	MCLK, MOEX	-	1	9	ns	
	t_{REH}		-	1	9	ns	
Data set up →MCLK ↑ time	t_{DS}	MCLK, MADATA[31: 0]	-	19	-	ns	
MCLK ↑ → Data hold time	t_{DH}	MCLK, MADATA[31: 0]	-	0	-	ns	
MWEX delay time	t_{WEL}	MCLK, MWEX	-	1	9	ns	
	t_{WEH}		-	1	9	ns	
MDQM[1: 0] delay time	t_{DQML}	MCLK, MDQM[3: 0]	-	1	9	ns	
	t_{DQMH}		-	1	9	ns	
MCLK ↑ → Data output time	t_{ODS}	MCLK, MADATA[31: 0]	-	MCLK+1	MCLK+18	ns	
MCLK ↑ → Data hold time	t_{OD}	MCLK, MADATA[31: 0]	-	1	18	ns	

Note:

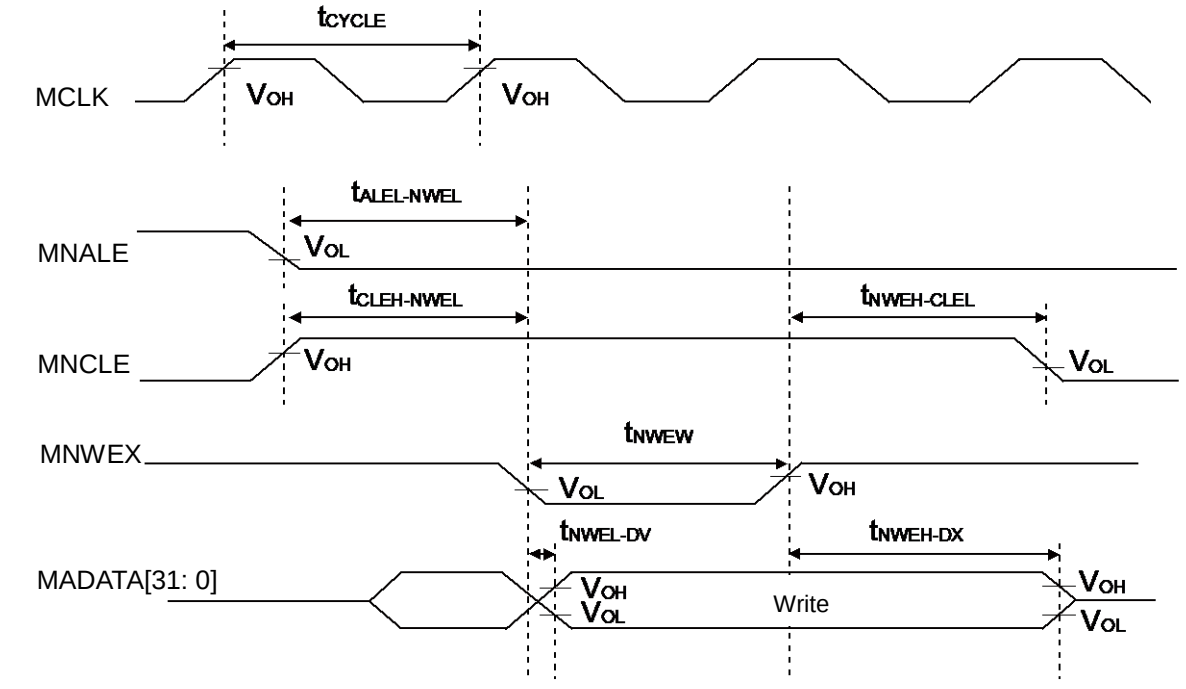
- *When the external load capacitance C_L = 30 pF*

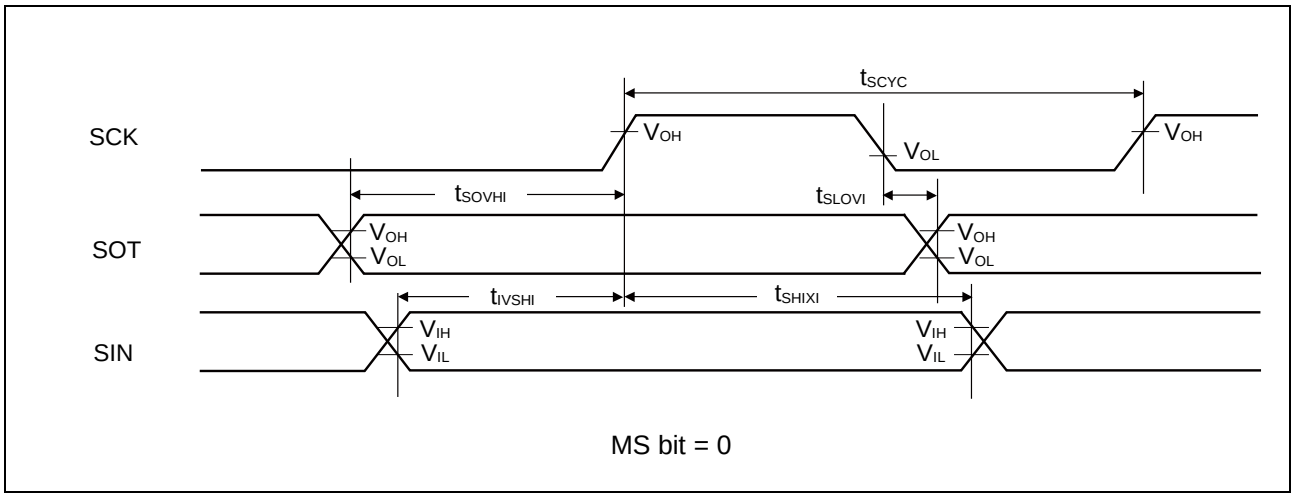


NAND Flash Address Write

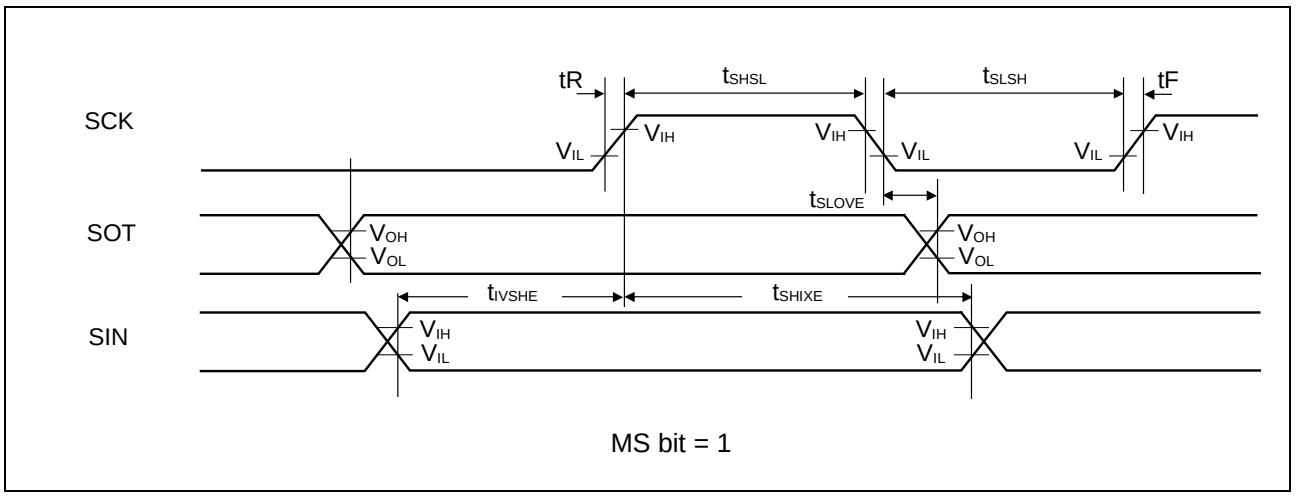


NAND Flash Command Write





MS bit = 0



MS bit = 1

When Using Synchronous Serial Chip Select (SCINV = 0, CSLVL = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↓ setup time	t_{CSSI}	Internal shift clock operation	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↑→SCS↑ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	ns
SCS↓→SCK↓ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCK↑→SCS↑ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCS↓→SOT delay time	t_{DSE}		-	40	-	40	ns
SCS ↑ →SOT delay time	t_{DEE}		0	-	0	-	ns

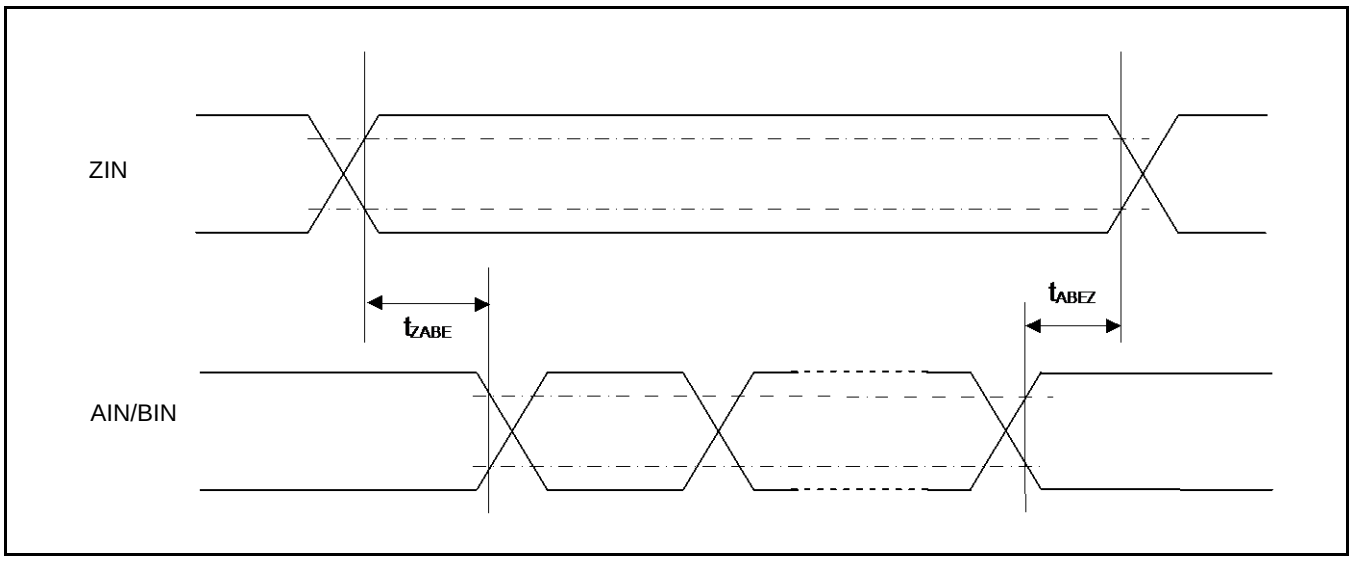
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.*
- *For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*


ZIN
AIN/BIN
tZABE
tABEZ

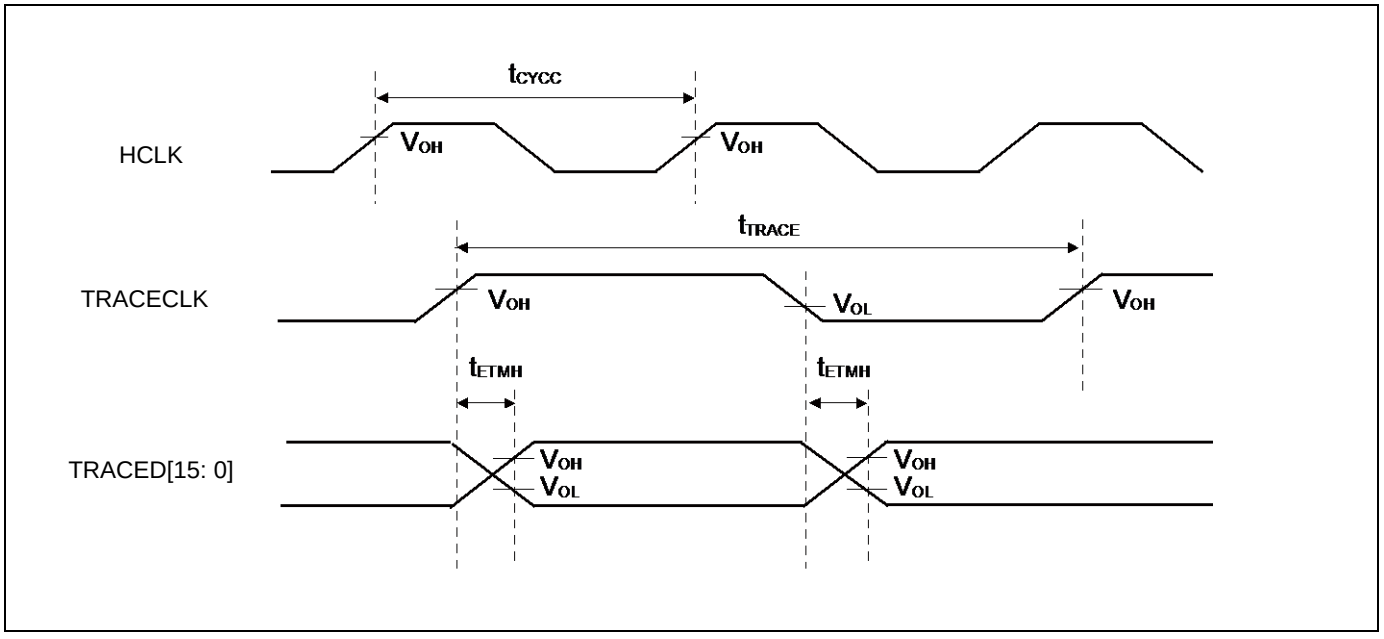
12.4.17 ETM/ HTM Timing

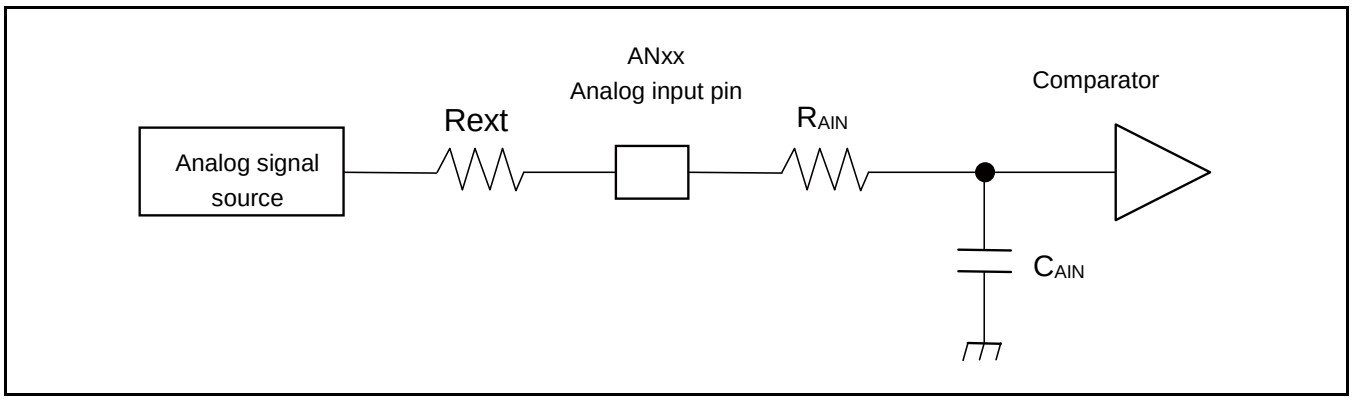
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Data hold	t_{ETMH}	TRACECLK, TRACED[15: 0]	$V_{CC} \geq 4.5$ V	2	9	ns	
			$V_{CC} < 4.5$ V	2	15		
TRACECLK frequency	$1/t_{TRACE}$	TRACECLK	$V_{CC} \geq 4.5$ V		50	MHz	
			$V_{CC} < 4.5$ V		32	MHz	
TRACECLK clock cycle	t_{TRACE}		$V_{CC} \geq 4.5$ V	20	-	ns	
			$V_{CC} < 4.5$ V	31.25	-	ns	

Note:

- *When the external load capacitance C_L = 30 pF.*





(Equation 1) $t_S \geq (R_{AIN} + R_{ext}) \times C_{AIN} \times 9$

t_S: Sampling time

R_{AIN}: Input resistance of A/D = 1.2 kΩ at 4.5 V ≤ AV_{CC} ≤ 5.5 V

Input resistance of A/D = 1.8 kΩ at 2.7 V ≤ AV_{CC} < 4.5 V

C_{AIN}: Input capacity of A/D = 12.05 pF at 2.7 V ≤ AV_{CC} ≤ 5.5 V

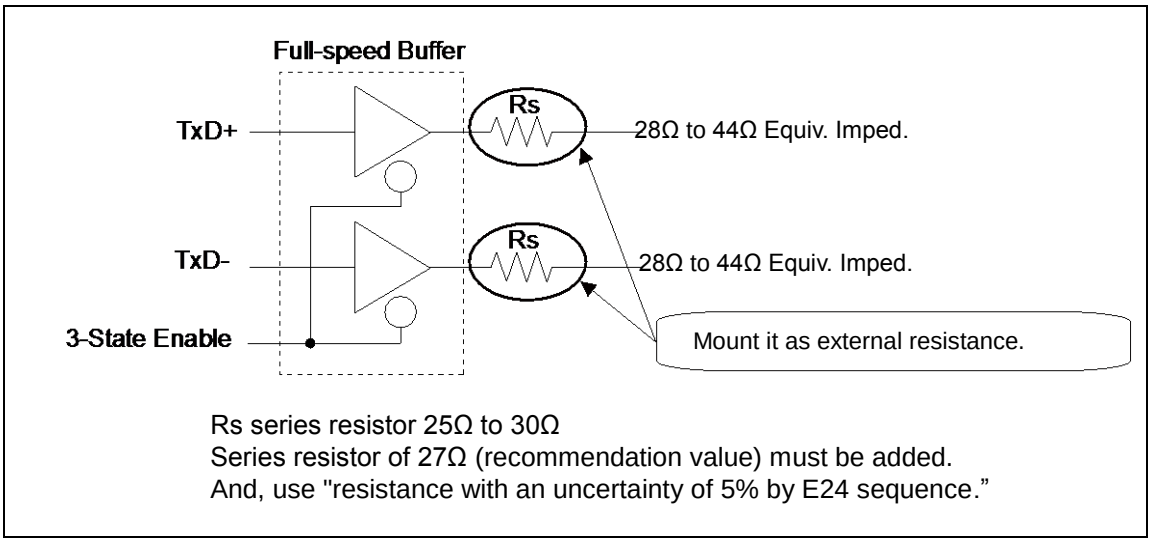
R_{ext}: Output impedance of external circuit

(Equation 2) $t_C = t_{CCK} \times 14$

t_C: Compare time

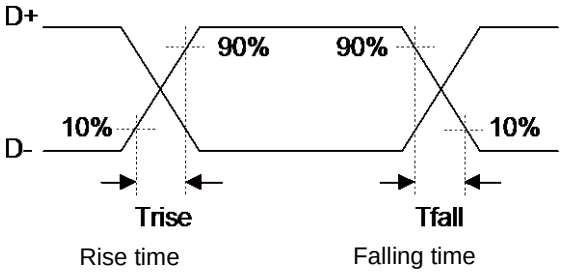
t_{CCK}: Compare clock cycle

*6: USB Full-speed connection is performed via twisted-pair cable shield with 90 Ω ± 15% characteristic impedance (differential mode).
USB standard defines that the output impedance of the USB driver must be in the range from 28 Ω to 44 Ω.
So, a discrete series resistor (Rs) addition is defined in order to satisfy the above definition and keep balance.
When using this USB I/O, use it with 25 Ω to 30 Ω (recommended value 27 Ω) series resistor Rs.



Rs series resistor 25Ω to 30Ω
Series resistor of 27Ω (recommendation value) must be added.
And, use "resistance with an uncertainty of 5% by E24 sequence."

*7: They indicate rise time (T_{RISE}) and fall time (T_{FALL}) of the low-speed differential data signal.
They are defined by the time between 10% and 90% of the output signal voltage.



Note:

- *See Low-Speed Load (Compliance Load) for conditions of external load.*

12.11 Standby Recovery Time

12.11.1 Recovery Cause: Interrupt/WKUP

The time from the interrupt occurring to the time of program operation start is shown.

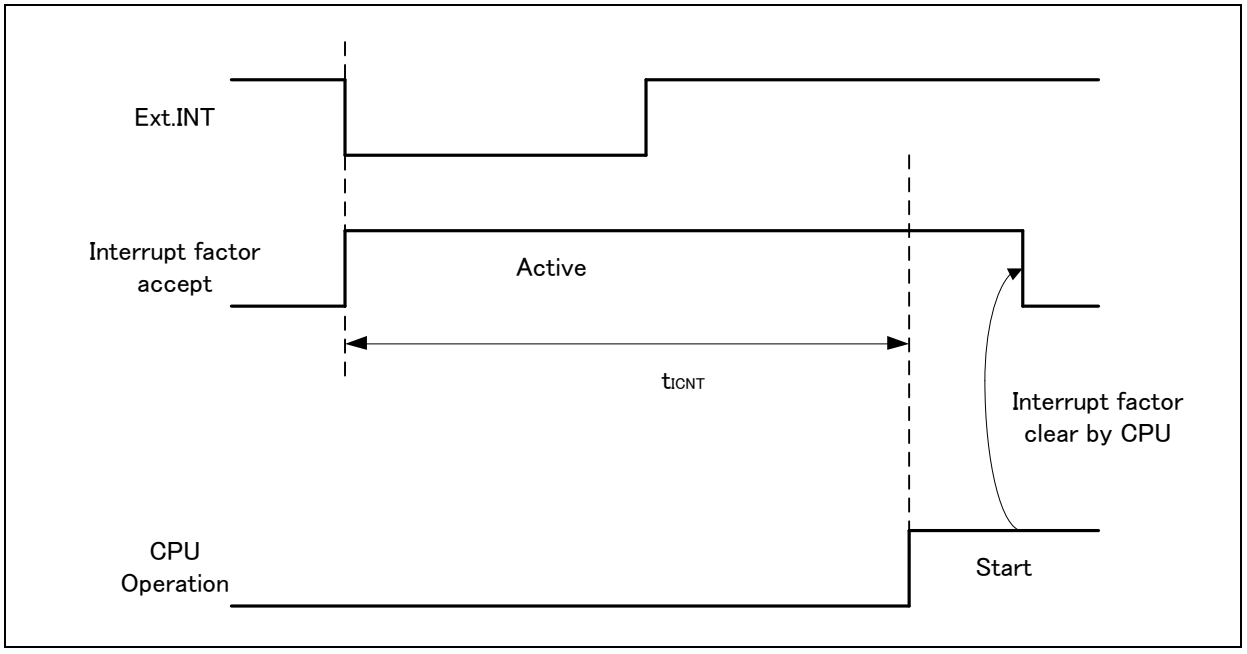
Recovery Count Time

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
Sleep mode	t_{ICNT}	HCLK×1		µs	
High-speed CR Timer mode Main Timer mode PLL Timer mode		40	80	µs	
Low-speed CR Timer mode		450	900	µs	
Sub Timer mode		896	1136	µs	
RTC mode Stop mode (High-speed CR/Main/PLL Run mode return)		316	581	µs	
RTC mode Stop mode (Low-speed CR/sub Run mode return)		270	540	µs	
Deep Standby RTC mode with RAM retention		365	667	µs	without RAM retention
Deep Standby Stop mode with RAM retention		365	667	µs	with RAM retention

*: The maximum value depends on the built-in CR accuracy.

Example of Standby Recovery Operation (when in External Interrupt Recovery*)



*: External interrupt is set to detecting fall edge.

13. Ordering Information

Part Number	Flash	RAM	Crypto	Package
S6E2C28H0AGV2000A	1 MB	128 KB	N/A	Plastic LQFP (0.5 mm pitch), 144 pin (LQS144)
S6E2C29H0AGV2000A	1.5 MB	192 KB	N/A	
S6E2C2AH0AGV2000A	2 MB	256 KB	N/A	
S6E2C28HHAGV2000A	1 MB	128 KB	Yes	
S6E2C29HHAGV2000A	1.5 MB	192 KB	Yes	
S6E2C2AHHAGV2000A	2 MB	256 KB	Yes	
S6E2C28J0AGV2000A	1 MB	128 KB	N/A	Plastic LQFP (0.5 mm pitch), 176 pin (LQP176)
S6E2C29J0AGV2000A	1.5 MB	192 KB	N/A	
S6E2C2AJ0AGV2000A	2 MB	256 KB	N/A	
S6E2C28JHAGV2000A	1 MB	128 KB	Yes	
S6E2C29JHAGV2000A	1.5 MB	192 KB	Yes	
S6E2C2AJHAGV2000A	2 MB	256 KB	Yes	
S6E2C28J0AGB1000A	1 MB	128 KB	N/A	Plastic FBGA (0.8 mm pitch), 192 pin (LBE192)
S6E2C29J0AGB1000A	1.5 MB	192 KB	N/A	
S6E2C2AJ0AGB1000A	2 MB	256 KB	N/A	
S6E2C28JHAGB1000A	1 MB	128 KB	Yes	
S6E2C29JHAGB1000A	1.5 MB	192 KB	Yes	
S6E2C2AJHAGB1000A	2 MB	256 KB	Yes	
S6E2C28L0AGL2000A	1 MB	128 KB	N/A	Plastic LQFP (0.4 mm pitch), 216 pin (LQQ216)
S6E2C29L0AGL2000A	1.5 MB	192 KB	N/A	
S6E2C2AL0AGL2000A	2 MB	256 KB	N/A	
S6E2C28LHAGL2000A	1 MB	128 KB	Yes	
S6E2C29LHAGL2000A	1.5 MB	192 KB	Yes	
S6E2C2ALHAGL2000A	2 MB	256 KB	Yes	