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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CSIO, EBI/EMI, Ethernet, I²C, LINbus, SD, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	120
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2c29h0agv2000a

Multi-function Serial Interface (Max 16 channels)

- Separate 64 byte receive and transmit FIFO buffers for channels 0 to 7.
- Operation mode is selectable for each channel from the following:
  - UART
  - CSIO (SPI)
  - LIN
  - I^2C
- UART
  - Full-duplex double buffer
  - Selection with or without parity supported
  - Built-in dedicated baud rate generator
  - External clock available as a serial clock
  - Various error detect functions available (parity errors, framing errors, and overrun errors)
- CSIO (SPI)
  - Full-duplex double buffer
  - Built-in dedicated baud rate generator
  - Overrun error detect function available
  - Serial chip select function (ch 6 and ch 7 only)
  - Supports high-speed SPI (ch 4 and ch 6 only)
  - Data length 5 to 16-bit
- LIN
  - LIN protocol Rev.2.1 supported
  - Full-duplex double buffer
  - Master/slave mode supported
  - LIN break field generation (can change to 13- to 16-bit length)
  - LIN break delimiter generation (can change to 1- to 4-bit length)
  - Various error detect functions available (parity errors, framing errors, and overrun errors)
- I^2C
  - Standard mode (Max 100 kbps)/Fast mode (Max 400 kbps) supported
  - Fast mode Plus (Fm+) (Max 1000 kbps, only for ch 3 = ch A and ch 7 = ch B) supported

DMA Controller (Eight channels)

DMA controller has an independent bus, so the CPU and DMA controller can process simultaneously.

- Eight independently configured and operated channels
- Transfer can be started by software or request from the built-in peripherals
- Transfer address area: 32-bit (4 GB)
- Transfer mode: Block transfer/Burst transfer/Demand transfer
- Transfer data type: bytes/half-word/word
- Transfer block count: 1 to 16
- Number of transfers: 1 to 65536

DSTC (Descriptor System data Transfer Controller; 256 Channels)

The DSTC can transfer data at high-speed without going via the CPU. The DSTC adopts the descriptor system and, following the specified contents of the descriptor that has already been constructed on the memory, can access directly the memory/peripheral device and perform the data-transfer operation.

It supports the software activation, the hardware activation, and the chain activation functions.

A/D Converter (Max 32 channels)

- 12-bit A/D Converter
  - Successive approximation type
  - Built-in three units
  - Conversion time: 0.5 µs at 5 V
  - Priority conversion available (priority at two levels)
  - Scanning conversion mode
  - Built-in FIFO for conversion data storage (for SCAN conversion: 16 steps, for priority conversion: 4 steps)

D/A Converter (Max 2 Channels)

- R-2R type
- 12-bit resolution

Base Timer (Max 16 Channels)

Operation mode is selected from the following for each channel:

- 16-bit PWM timer
- 16-bit PPG timer
- 16-/32-bit reload timer
- 16-/32-bit PWC timer

General Purpose I/O Port

This series can use its pins as general purpose I/O ports when they are not used for external bus or peripherals; moreover, the port relocate function is built in. It can set the I/O port to which the peripheral function can be allocated.

- Capable of pull-up control per pin
- Capable of reading pin level directly
- Built-in port-relocate function
- Up to 120 high-speed general-purpose I/O ports in 144 pin package
- Some pins 5V tolerant I/O.
  See 4. Pin Descriptions and 5. I/O Circuit Type for the corresponding pins.

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
10	10	-	E2	P50 SCS72_0 RTO00_1 (PPG00_1) TIOA8_2 MADATA16_0	E	I
11	11	-	E3	P51 SCS73_0 RTO01_1 (PPG00_1) TIOB8_2 MADATA17_0	E	I
12	12	-	E4	P52 RTO02_1 (PPG02_1) TIOA9_2 MADATA18_0	E	I
13	-	-	-	P53 RTO03_1 (PPG02_1) TIOB9_2 MADATA19_0	E	I
14	13	10	E5	PA8 SIN7_0 IC21_0 INT02_0 WKUP1 MADATA08_0	I	Q
15	14	11	F1	PA9 SOT7_0 (SDA7_0) IC22_0 MADATA09_0	N	I
16	15	12	F2	PAA SCK7_0 (SCL7_0) IC23_0 MADATA10_0	N	I
17	16	13	F3	PAB SCS70_0 FRCK2_0 INT03_0 MADATA11_0	E	K
18	17	14	F4	PAC SCS71_0 TIOB8_0 AIN3_0 MADATA12_0	E	I
19	-	-	-	P54 SIN15_1 RTO04_1 (PPG04_1) TIOA10_2 INT00_2 MADATA20_0	E	K

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
42	32	27	J5	P36 IC01_0 INT02_1 S_DATA3_0	L	K
43	33	28	J4	P37 IC00_0 INT03_1 S_DATA2_0	L	K
44	34	29	J3	P38 ADTG_2 DTTI0X_0 S_WP_0	E	I
45	35	30	J2	P39 SIN2_1 RTO00_0 (PPG00_0) TIOA0_1 AIN3_1 INT16_1 S_CD_0 MAD24_0	G	K
46	36	31	K1	P3A SOT2_1 (SDA2_1) RTO01_0 (PPG00_0) TIOA1_1 BIN3_1 INT17_1 MAD23_0	G	K
47	37	32	K2	P3B SCK2_1 (SCL2_1) RTO02_0 (PPG02_0) TIOA2_1 ZIN3_1 INT18_1 MAD22_0 MNALE_0	G	K
48	38	33	K3	P3C SIN13_0 RTO03_0 (PPG02_0) TIOA3_1 INT19_1 MAD21_0 MNCLE_0	G	K
49	39	34	K4	P3D SOT13_0 (SDA13_0) RTO04_0 (PPG04_0) TIOA4_1 MAD20_0 MNWEX_0	G	I

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
97	80	64	K10	P79 SOT6_0 (SDA6_0) IC11_0 MAD08_0	L	I
98	81	65	M10	P7A SCK6_0 (SCL6_0) IC12_0 MAD09_0	L	I
99	82	66	N11	P7B DA1 SCS60_0 IC13_0 INT22_0	R	J
100	83	67	M11	P7C DA0 SCS61_0 INT04_1	R	J
101	-	-	-	PFA SCK7_1 (SCL7_1) IC11_1 ZIN1_1	E	I
102	-	-	-	PFB SOT7_1 (SDA7_1) IC12_1 INT07_2	E	K
103	-	-	-	PFC SIN7_1 IC13_1 INT06_2	E	K
104	84	68	N13	PE0 MD1	C	E
105	85	69	N12	MD0	J	D
106	86	70	P12	PE2 X0	A	A
107	87	71	P13	PE3 X1	A	B
108	88	72	N14	VSS	-	-
109	89	73	M14	VCC	-	-
110	90	74	M13	AVCC	-	-
111	91	75	M12	AVSS	-	-
112	92	76	L13	AVRL	-	-
113	93	77	L12	AVRH	-	-
114	94	78	L11	P10 AN00 SIN10_0 TIOA0_2 AIN0_2 INT08_0	F	M

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
125	101	85	J11	P17 AN07 SCK11_0 (SCL11_0) TIOB2_2 ZIN1_2	F	L
126	102	-	J10	PB0 AN16 SCK6_1 (SCL6_1) TIOA9_1	F	L
127	103	-	J9	PB1 AN17 SCS60_1 TIOB9_1 INT08_1	F	M
128	104	-	H10	PB2 AN18 SCS61_1 TIOA10_1 INT09_1	F	M
129	105	-	J14	PB3 AN19 SCS62_1 TIOB10_1	F	L
130	106	86	H9	P18 AN08 SIN2_0 TIOA3_2 INT10_0	F	M
131	107	87	H12	P19 AN09 SOT2_0 (SDA2_0) TIOB3_2 INT24_1 TRACECLK	F	O
132	108	88	H14	P1A AN10 SCK2_0 (SCL2_0) TIOA4_2 TRACED0	F	N
133	109	89	G14	P1B AN11 SIN12_0 TIOB4_2 INT11_0 TRACED1	F	O
134	110	90	H13	P1C AN12 SOT12_0 (SDA12_0) TIOA5_2 TRACED2	F	N

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
GPIO	P30	General-purpose I/O port 3	34	24	-	G6
	P31		35	25	-	H4
	P32		36	26	21	H2
	P33		37	27	22	J1
	P34		38	28	23	H3
	P35		41	31	26	H6
	P36		42	32	27	J5
	P37		43	33	28	J4
	P38		44	34	29	J3
	P39		45	35	30	J2
	P3A		46	36	31	K1
	P3B		47	37	32	K2
	P3C		48	38	33	K3
	P3D		49	39	34	K4
	P3E		50	40	35	L1
	P40	General-purpose I/O port 4	56	46	38	N2
	P41		57	47	39	N3
	P42		58	48	40	M3
	P43		59	49	41	L4
	P44		60	50	42	M4
	P45		61	51	43	N4
	P46		73	58	50	P5
	P47		74	59	51	P6
	P48		76	61	53	N6
	P49		77	62	54	M6
	P4A		65	-	-	-
	P4B		66	-	-	-
	P4C		67	-	-	-
	P4D		68	-	-	-
	P4E		69	-	-	-

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Multi-Function Serial 3	SIN3_0	Multi-function serial interface ch 3 input pin	25	20	17	G2
	SIN3_1		56	46	38	N2
	SOT3_0 (SDA3_0)	Multi-function serial interface ch 3 output pin. This pin operates as SOT3 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA3 when it is used in an I^2C (operation mode 4).	24	19	16	F6
	SOT3_1 (SDA3_1)		57	47	39	N3
	SCK3_0 (SCL3_0)	Multi-function serial interface ch 3 clock I/O pin. This pin operates as SCK3 when it is used in a CSIO (operation modes 2) and as SCL3 when it is used in an I^2C (operation mode 4).	23	18	15	F5
	SCK3_1 (SCL3_1)		58	48	40	M3
Multi-Function Serial 4	SIN4_0	Multi-function serial interface ch 4 input pin	212	172	140	B3
	SIN4_1		193	161	131	D7
	SOT4_0 (SDA4_0)	Multi-function serial interface ch 4 output pin. This pin operates as SOT4 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA4 when it is used in an I^2C (operation mode 4).	211	171	139	C4
	SOT4_1 (SDA4_1)		192	160	130	A6
	SCK4_0 (SCL4_0)	Multi-function serial interface ch 4 clock I/O pin. This pin operates as SCK4 when it is used in a CSIO (operation mode 2) and as SCL4 when it is used in an I^2C (operation mode 4).	210	170	138	B4
	SCK4_1 (SCL4_1)		198	166	136	D6
	CTS4_0	Multi-function serial interface ch 4 CTS input pin	208	168	-	B5
	CTS4_1		197	165	135	C6
	RTS4_0	Multi-function serial interface ch 4 RTS output pin	209	169	137	C5
	RTS4_1		194	162	132	E7

Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent this, do the following:

1. Avoid exposure to rapid temperature changes, which can cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
3. When Dry Packages are opened, it is recommended to have humidity between 40% and 70%.
4. When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in these aluminum laminate bags for storage.
5. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

1. Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons, and peripheral equipment.
3. Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ). Wearing of conductive clothing and shoes, and the use of conductive floor mats and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments, or protect with anti-static measures.
5. Avoid the use of Styrofoam or other highly static-prone materials for storage of completed board assemblies.

Table 12-4 Typical and Maximum Current Consumption in Normal Operation (Other Than PLL), Code with Data Accessing Running from Flash Memory (Flash 0 Wait-cycle Mode and Read Access 0 Wait)

Parameter	Symbol	Pin Name	Conditions		Frequency*4	Value		Unit	Remarks
						Typ*1	Max*2		
Power supply current	I_{CC}	VCC	Normal operation *6, *7 (main oscillation)	*5	4 MHz	4.7	84.9	mA	*3 When all peripheral clocks are on
						3.9	83.8	mA	*3 When all peripheral clocks are off
			Normal operation *6 (built-in High-speed CR)	*5	4 MHz	3.0	83.2	mA	*3 When all peripheral clocks are on
						2.1	82.0	mA	*3 When all peripheral clocks are off
			Normal operation *6, *8 (sub oscillation)	*5	32 kHz	0.78	80.37	mA	*3 When all peripheral clocks are on
						0.77	80.36	mA	*3 When all peripheral clocks are off
			Normal operation *6 (built-in low-speed CR)	*5	100 kHz	0.81	80.39	mA	*3 When all peripheral clocks are on
						0.78	80.38	mA	*3 When all peripheral clocks are off

*1: T_A = +25°C, V_{CC} = 3.3 V

*2: T_J = +125°C, V_{CC} = 5.5 V

*3: When all ports are fixed

*4: Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK/2

*5: When operating flash 0 wait-cycle mode and read access 0 wait (FRWTR.RWT = 00, FBFCR.SD = 000)

*6: With data access to a MainFlash memory.

*7: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

*8: When using the crystal oscillator of 32 Hz (including the current consumption of the oscillation circuit)

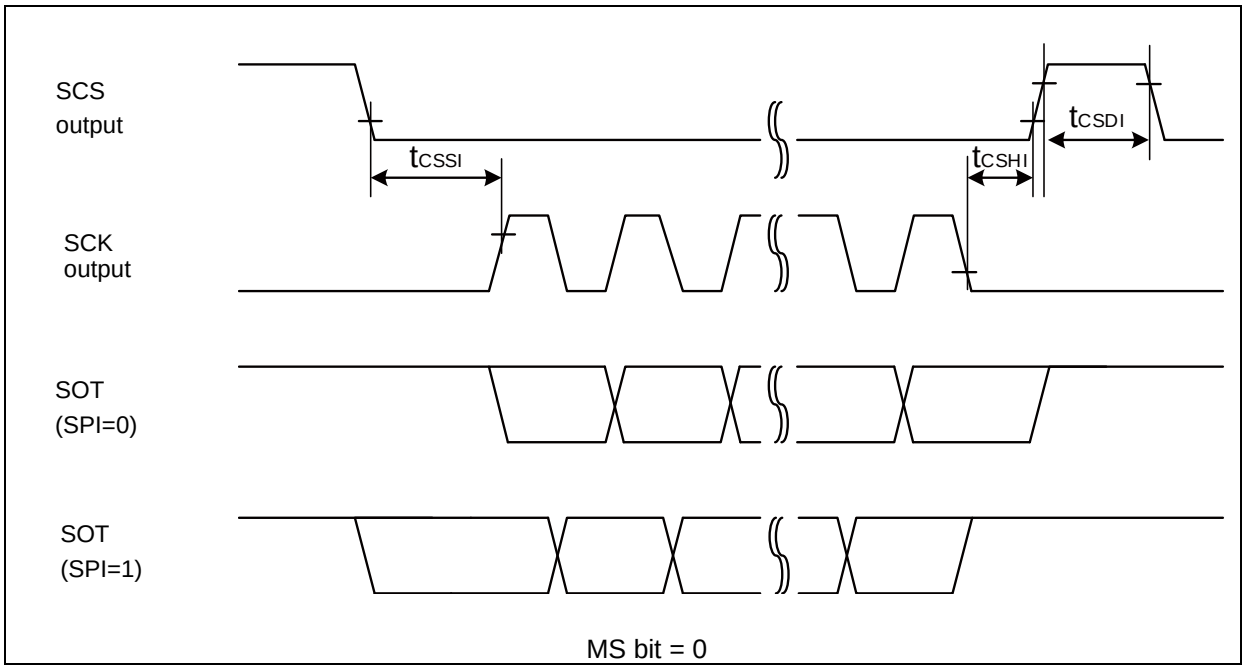
Separate Bus Access Asynchronous SRAM Mode

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

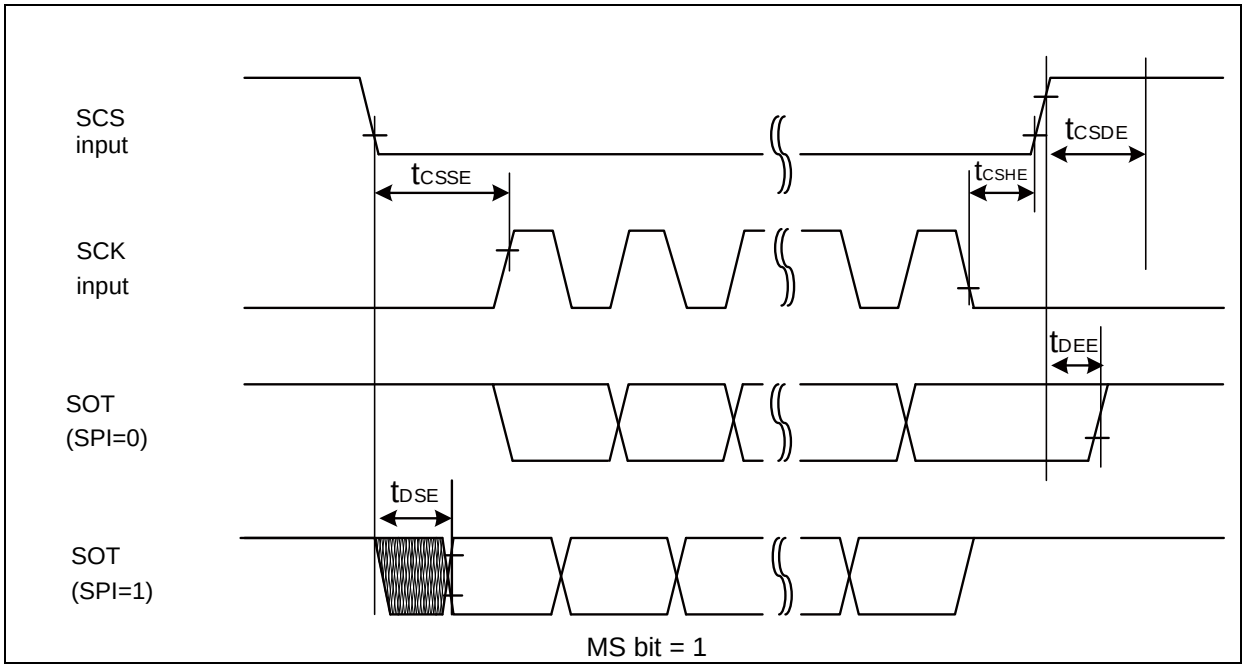
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
MOEX Minimum pulse width	t_{OEW}	MOEX	-	MCLK×n-3	-	ns	
MCSX ↓ →Address output delay time	$t_{CSL - AV}$	MCSX[7: 0], MAD[24: 0]	-	-9	+9	ns	
MOEX ↑ →Address hold time	$t_{OEH - AX}$	MOEX, MAD[24: 0]	-	0	MCLK×m+9	ns	
MCSX ↓ → MOEX ↓ delay time	$t_{CSL - OEL}$	MOEX, MCSX[7: 0]	-	MCLK×m-9	MCLK×m+9	ns	
MOEX ↑ → MCSX ↑ time	$t_{OEH - CSH}$		-	0	MCLK×m+9	ns	
MCSX ↓ → MDQM ↓ delay time	$t_{CSL - RDQML}$	MCSX, MDQM[3: 0]	-	MCLK×m-9	MCLK×m+9	ns	
Data set up→MOEX ↑ time	$t_{DS - OE}$	MOEX, MADATA[31: 0]	-	20	-	ns	
MOEX ↑ → Data hold time	$t_{DH - OE}$	MOEX, MADATA[31: 0]	-	0	-	ns	
MWEX Minimum pulse width	t_{WEW}	MWEX	-	MCLK×n-3	-	ns	
MWEX ↑ →Address output delay time	$t_{WEH - AX}$	MWEX, MAD[24: 0]	-	0	MCLK×m+9	ns	
MCSX ↓ → MWEX ↓ delay time	$t_{CSL - WEL}$	MWEX, MCSX[7: 0]	-	MCLK×n-9	MCLK×n+9	ns	
MWEX ↑ → MCSX ↑ delay time	$t_{WEH - CSH}$		-	0	MCLK×m+9	ns	
MCSX ↓ → MDQM ↓ delay time	$t_{CSL-WDQML}$	MCSX, MDQM[3: 0]	-	MCLK×n-9	MCLK×n+9	ns	
MCSX ↓ → Data output time	t_{CSL-DX}	MCSX, MADATA[31: 0]	-	MCLK-9	MCLK+9	ns	
MWEX ↑ → Data hold time	$t_{WEH - DX}$	MWEX, MADATA[31: 0]	-	0	MCLK×m+9	ns	

Note:

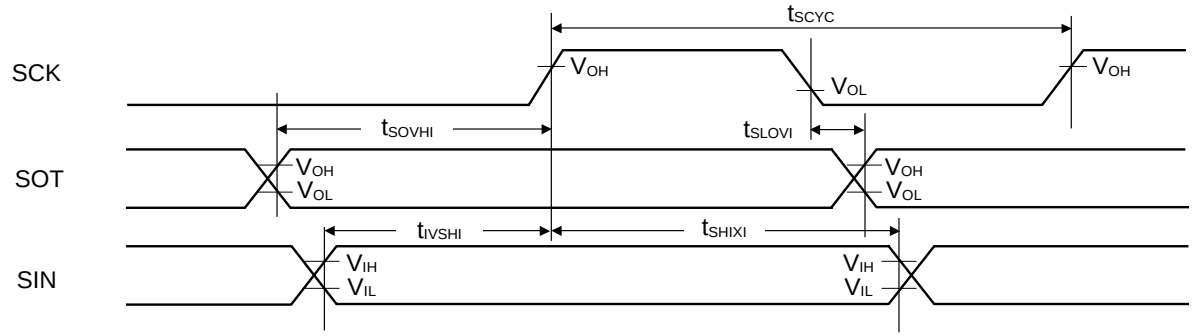
- *When the external load capacitance C_L = 30 pF (m = 0 to 15, n = 1 to 16)*



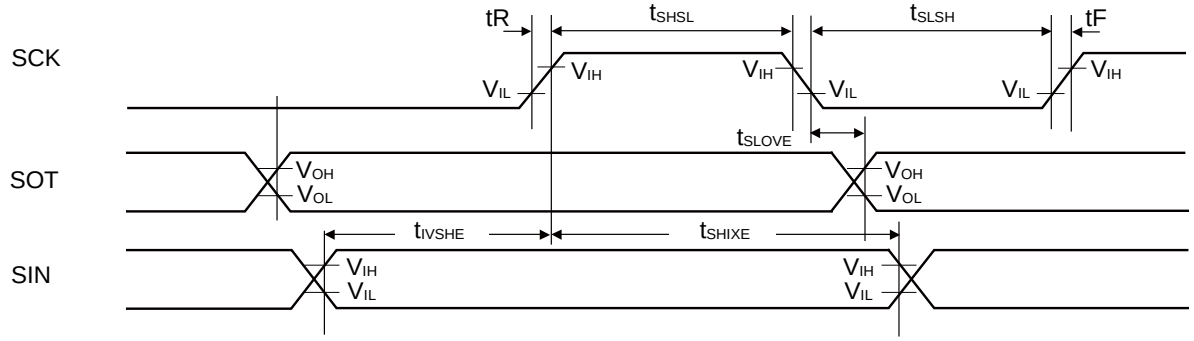
MS bit = 0



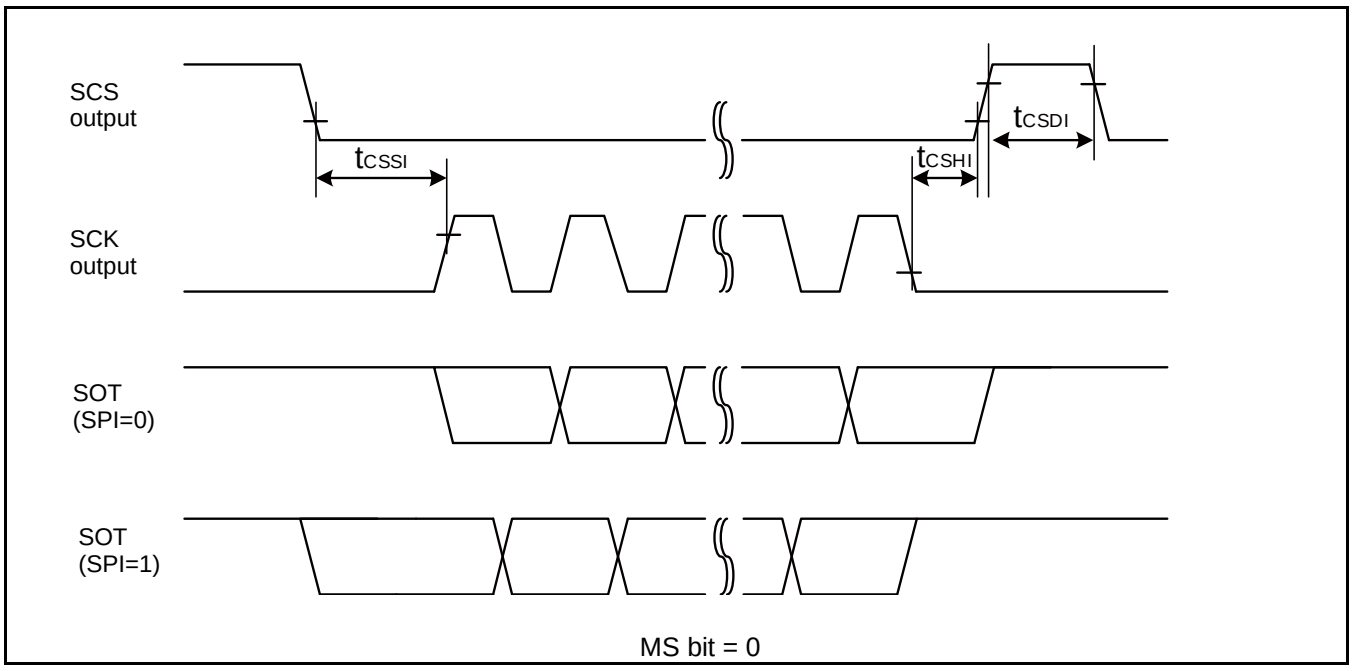
MS bit = 1



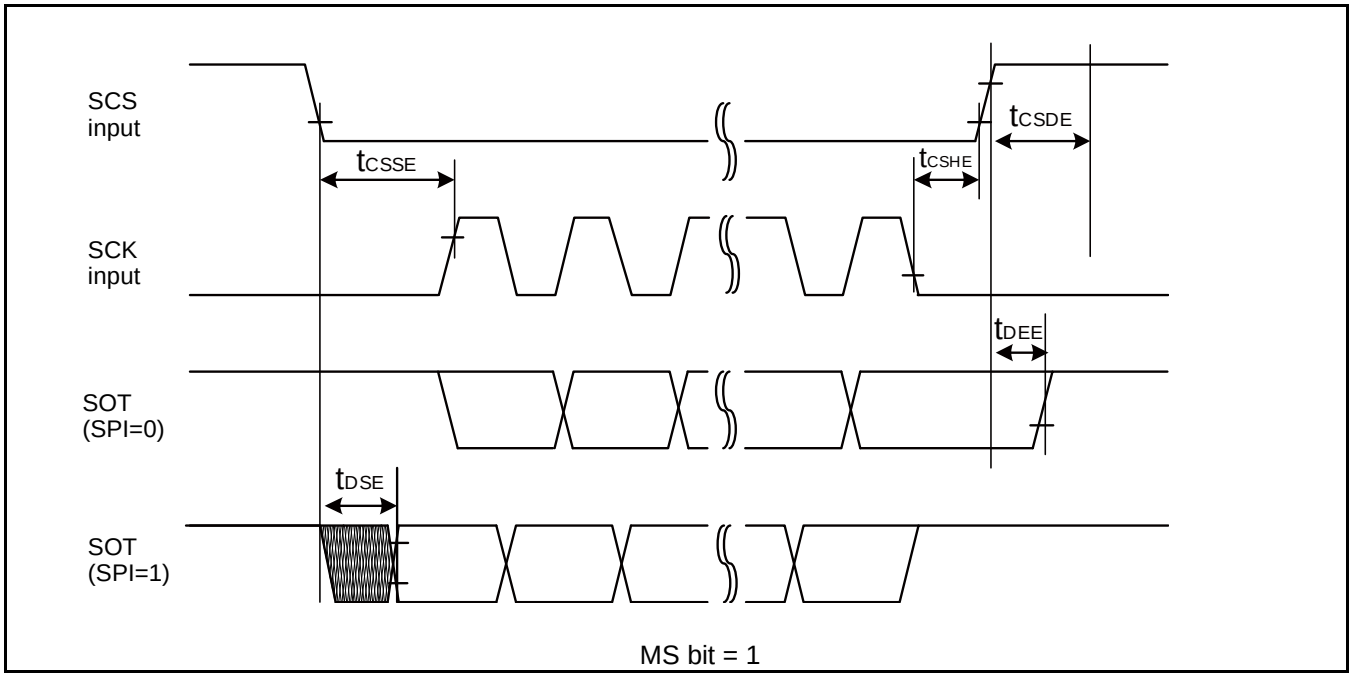
MS bit = 0



MS bit = 1



MS bit = 0

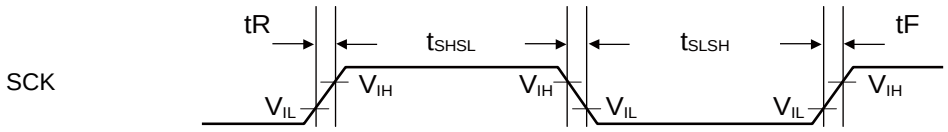


MS bit = 1

External clock (EXT = 1): When in Asynchronous Mode Only

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
Serial clock L pulse width	t_{SLSH}	C_L = 30 pF	t_{CYCP} + 10	-	ns	
Serial clock H pulse width	t_{SHSL}		t_{CYCP} + 10	-	ns	
SCK fall time	t_F		-	5	ns	
SCK rise time	t_R		-	5	ns	



12.4.13 External Input Timing

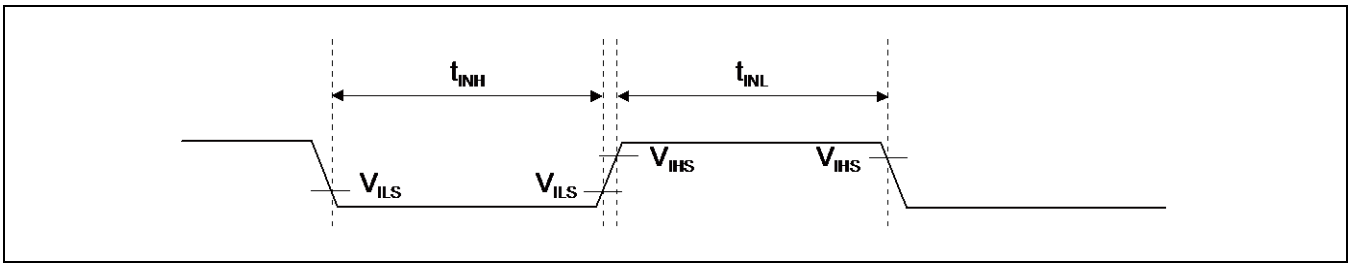
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{INH}, t_{INL}	ADTGx	-	$2t_{CYCP}$*1	-	ns	A/D converter trigger input
		FRCKx					Free-run timer input clock
		ICxx					Input capture
		DTTIxX	-	$2t_{CYCP}$*1	-	ns	Waveform generator
		INT00 to INT31, NMIX	-	$2t_{CYCP}$ + 100*1	-	ns	External interrupt, NMI
				500*2	-	ns	
		WKUPx	-	500*3	-	ns	Deep standby wake up

1: t_{CYCP} indicates the APB bus clock cycle time except stop when in Stop mode, in Timer mode. For more information about the APB bus number to which the A/D converter, multi-function timer, and external interrupt are connected, see 8. Block Diagram in this data sheet.

2: When in Stop mode, in Timer mode

3: When in Deep Standby RTC mode, in Deep Standby Stop mode



12.4.15 I²C Timing

Standard-mode, Fast-mode

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Standard-mode		Fast-mode		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	f_{SCL}	C_L = 30 pF, R = (Vp/I_{OL})*1	0	100	0	400	kHz	
(Repeated) START condition hold time SDA ↓ → SCL ↓	t_{HDSTA}		4.0	-	0.6	-	µs	
SCL clock L width	t_{LOW}		4.7	-	1.3	-	µs	
SCL clock H width	t_{HIGH}		4.0	-	0.6	-	µs	
(Repeated) START condition setup time SCL ↑ → SDA ↓	t_{SUSTA}		4.7	-	0.6	-	µs	
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	3.45*2	0	0.9*3	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		250	-	100	-	ns	
Stop condition setup time SCL ↑ → SDA ↑	t_{SUSTO}		4.0	-	0.6	-	µs	
Bus free time between "Stop condition" and "START condition"	t_{BUF}		4.7	-	1.3	-	µs	
Noise filter	t_{SP}	2 MHz ≤ t_{CYCP} < 40 MHz	2 t_{CYCP}*4	-	2 t_{CYCP}*4	-	ns	*5
		40 MHz ≤ t_{CYCP} < 60 MHz	4 t_{CYCP}*4	-	4 t_{CYCP}*4	-	ns	
		60 MHz ≤ t_{CYCP} < 80 MHz	6 t_{CYCP}*4	-	6 t_{CYCP}*4	-	ns	
		80 MHz ≤ t_{CYCP} ≤ 100 MHz	8 t_{CYCP}*4	-	8 t_{CYCP}*4	-	ns	

*1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively. V_p indicates the power supply voltage of the pull-up resistance and I_{OL} indicates V_{OL} guaranteed current.

*2: The maximum t_{HDDT} must not extend beyond the low period (t_{LOW}) of the device's SCL signal.

*3: Fast-mode I²C bus device can be used on a Standard-mode I²C bus system as long as the device satisfies the requirement of "t_{SUDAT} ≥ 250 ns."

*4: t_{CYCP} is the APB bus clock cycle time. For more information about the APB bus number to which the I²C is connected, see "8.Block Diagram" in this data sheet.
When using Standard-mode, the peripheral bus clock must be set more than 2 MHz.
When using Fast-mode, the peripheral bus clock must be set more than 8 MHz.

*5: The noise filter time can be changed by register settings. Change the number of the noise filter steps according to the APB bus clock frequency.

12.4.20 I²S Timing

Master Mode Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Output frequency	f_{MCYC}	I2SCK	-	-	12.288	MHz	
Output clock pulse width	t_{MHW}	I2SCK	-	45	55	%	
	t_{MLW}			45	55	%	
I2SCK→I2SWS delay time	t_{DFS}	I2SCK, I2SWS	-	0	24.0	ns	
I2SCK→I2SDO delay time*	t_{DDO}	I2SCK, I2SDO	-	0	24.0	ns	
I2SDI→I2SCK setup time	t_{HSDI}	I2SCK, I2SDI	-	25.0	-	ns	
I2SDI→I2SCK hold time	t_{HDI}		-	0	-	ns	
Input signal rise time	t_{FI}	I2SDI	-	-	5	ns	
Input signal fall time	t_{FI}		-	-	5	ns	

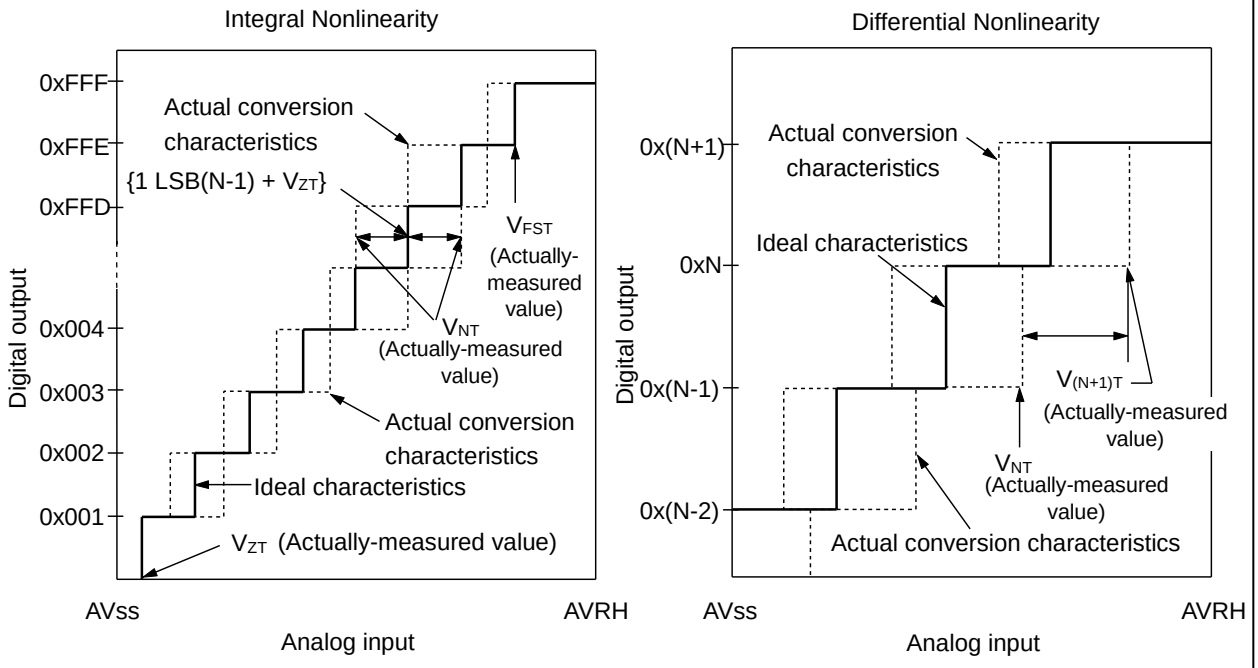
*: Except for the first bit of transmission frame

Note:

- *When the external load capacitance C_L = 20 pF*
- *When I2SWS = 48 kHz, I2MCLK = 256 × I2SWS*
  Frame synchronization signal (I2SWS) is settable to 48 kHz, 32 kHz, 16 kHz.
  See CHAPTER 7-2: I²S (Inter-IC Sound bus) Interface in FM4 Family Peripheral Manual Communication Macro Part (002-04862) for the details.

Definition of 12-bit A/D Converter Terms

- Resolution: Analog variation that is recognized by an A/D converter.
- Integral Nonlinearity: Deviation of the line between the zero-transition point (0b000000000000 ⟷ 0b000000000001) and the full-scale transition point (0b111111111110 ⟷ 0b111111111111) from the actual conversion characteristics.
- Differential Nonlinearity: Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



$$\text{Integral Nonlinearity of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{ZT}\}}{1LSB} \text{ [LSB]}$$

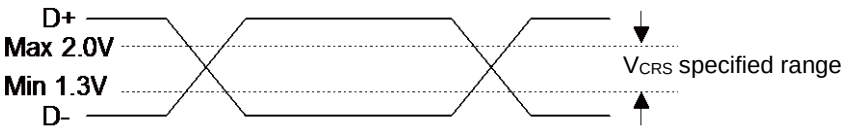
$$\text{Differential Nonlinearity of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{ZT}}{4094}$$

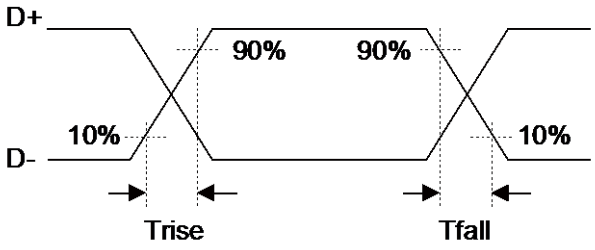
N: A/D converter digital output value.
V_{ZT}: Voltage at which the digital output changes from 0x000 to 0x001.
V_{FST}: Voltage at which the digital output changes from 0xFFE to 0xFFF.
V_{NT}: Voltage at which the digital output changes from 0x(N − 1) to 0xN.

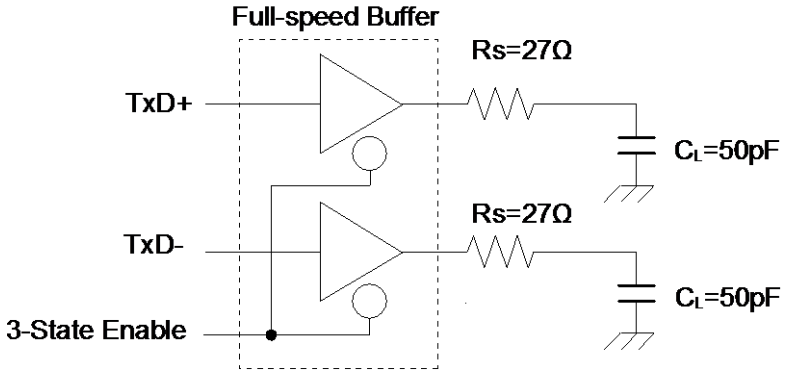
*3: The output drive capability of the driver is below 0.3 V at low state (V_{OL}) (to 3.6 V and 1.5 kΩ load), and 2.8 V or above (to the VSS and 1.5 kΩ load) at high state (V_{OH}).

*4: The cross voltage of the external differential output signal (D +/D −) of USB I/O buffer is within 1.3 V to 2.0 V.

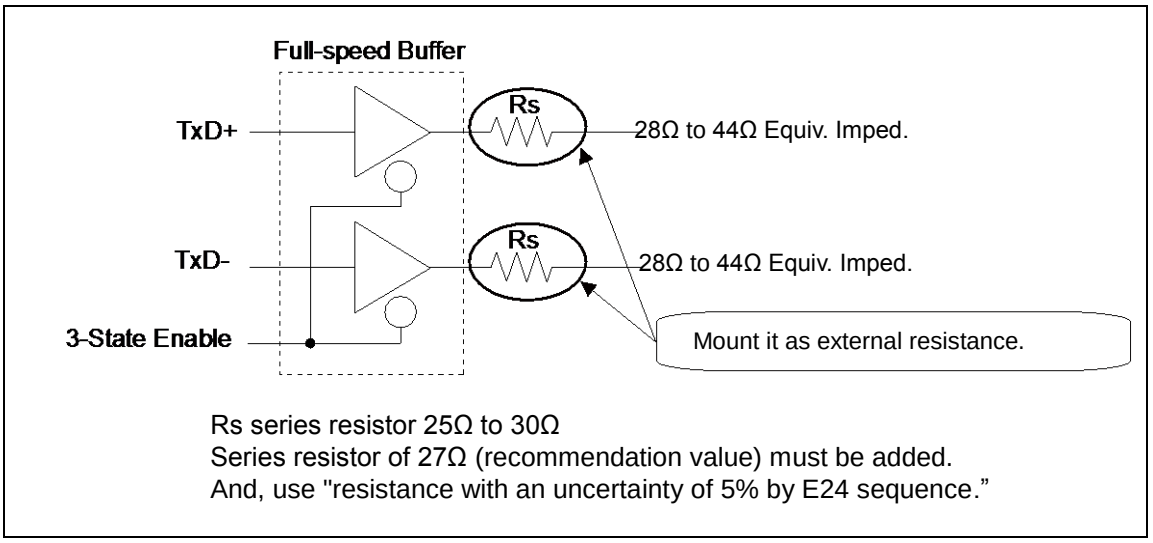


*5: They indicate rise time (T_{RISE}) and fall time (T_{FALL}) of the full-speed differential data signal.
They are defined by the time between 10% and 90% of the output signal voltage.
For full-speed buffer, t_R/t_F ratio is regulated as within ± 10% to minimize RFI emission.



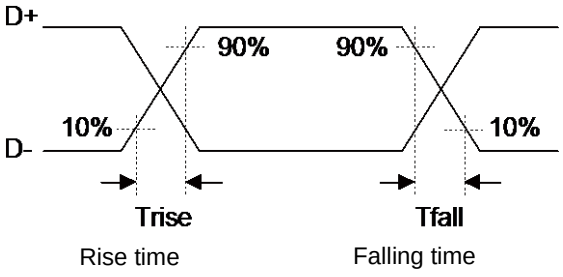


*6: USB Full-speed connection is performed via twisted-pair cable shield with 90 Ω ± 15% characteristic impedance (differential mode).
USB standard defines that the output impedance of the USB driver must be in the range from 28 Ω to 44 Ω.
So, a discrete series resistor (Rs) addition is defined in order to satisfy the above definition and keep balance.
When using this USB I/O, use it with 25 Ω to 30 Ω (recommended value 27 Ω) series resistor Rs.



Rs series resistor 25Ω to 30Ω
Series resistor of 27Ω (recommendation value) must be added.
And, use "resistance with an uncertainty of 5% by E24 sequence."

*7: They indicate rise time (T_{RISE}) and fall time (T_{FALL}) of the low-speed differential data signal.
They are defined by the time between 10% and 90% of the output signal voltage.



Note:

- *See Low-Speed Load (Compliance Load) for conditions of external load.*