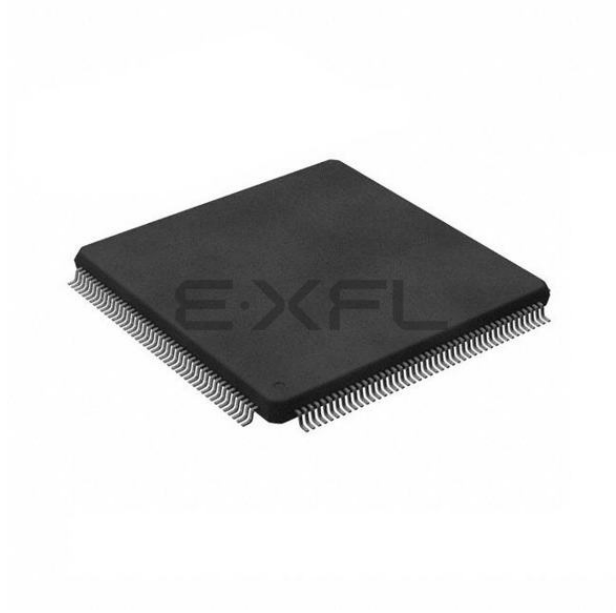

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CSIO, EBI/EMI, Ethernet, I²C, LINbus, SD, SPI, UART/USART, USB
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	152
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2c29j0agv2000a

1. Product Lineup

Memory Size

Product Name		S6E2C28H/J/L	S6E2C29H/J/L	S6E2C2AH/J/L
On-chip flash memory		1024 Kbytes	1536 Kbytes	2048 Kbytes
On-chip	SRAM	128 Kbytes	192 Kbytes	256 Kbytes
	SRAM0	64 Kbytes	128 Kbytes	192 Kbytes
	SRAM1	32 Kbytes	32 Kbytes	32 Kbytes
	SRAM2	32 Kbytes	32 Kbytes	32 Kbytes

Function

Product Name			S6E2C28H0A S6E2C29H0A S6E2C2AH0A S6E2C28HHA S6E2C29HHA S6E2C2AHHA	S6E2C28J0A S6E2C29J0A S6E2C2AJ0A S6E2C28JHA S6E2C29JHA S6E2C2AJHA	S6E2C28L0A S6E2C29L0A S6E2C2AL0A S6E2C28JHA S6E2C29JHA S6E2C2AJHA
Pin count			144	176/192	216
CPU			Cortex-M4F, MPU, NVIC 128 ch		
	Freq.		200 MHz		
Power supply voltage range			2.7V to 5.5V		
USB2.0 (device/host)			2 ch		
Ethernet-MAC			1ch.(Max) MII: 1 ch /RMII: 1 ch (Max)		
DMAC			8ch		
DSTC			256 ch		
External bus interface			Addr: 25-bit (Max), Data: 8-/16-bit CS: 9 (Max), SRAM, NOR flash NAND flash	Addr: 25-bit (Max), Data: 8-/16-bit CS: 9 (Max), SRAM, NOR flash , NAND flash SDRAM	Addr: 25-bit (Max), Data: 8-/16-/32-bit CS: 9 (Max), SRAM, NOR flash , NAND flash, SDRAM
Multi-function serial interface (UART/CSIO/LIN/I^2C)			16ch (Max) ch 0 to ch 7 : FIFO, ch 8 to ch 15 : No FIFO		
Base timer (PWC/Reload timer/PWM/PPG)			16 ch (Max)		
MF timer	A/D activation compare	6 ch	3 units (Max)		
	Input capture	4 ch			
	Free-run timer	3 ch			
	Output compare	6 ch			
	Waveform generator	3 ch			
	PPG	3 ch			
SD card interface			1 unit		
I^2S			-	1 unit	
High-speed quad SPI			-	1 unit	
QPRC			4 ch (Max)		
Dual timer			1 unit		
Real-time clock			1 unit		
Watch counter			1 unit		
CRC accelerator			Yes (fixed, programmable)		
Watchdog timer			1 ch (SW) + 1 ch (HW)		
External interrupts			32 pins (Max)+ NMI × 1		
I/O ports			120 pins (Max)	152 pins (Max)	190 pins (Max)
12-bit A/D converter			24 ch (3 units)	32 ch (3 units)	
12-bit D/A converter			2 units (Max)		
CSV (clock supervisor)			Yes		
LVD (low-voltage detector)			2 ch		

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
42	32	27	J5	P36 IC01_0 INT02_1 S_DATA3_0	L	K
43	33	28	J4	P37 IC00_0 INT03_1 S_DATA2_0	L	K
44	34	29	J3	P38 ADTG_2 DTTI0X_0 S_WP_0	E	I
45	35	30	J2	P39 SIN2_1 RTO00_0 (PPG00_0) TIOA0_1 AIN3_1 INT16_1 S_CD_0 MAD24_0	G	K
46	36	31	K1	P3A SOT2_1 (SDA2_1) RTO01_0 (PPG00_0) TIOA1_1 BIN3_1 INT17_1 MAD23_0	G	K
47	37	32	K2	P3B SCK2_1 (SCL2_1) RTO02_0 (PPG02_0) TIOA2_1 ZIN3_1 INT18_1 MAD22_0 MNALE_0	G	K
48	38	33	K3	P3C SIN13_0 RTO03_0 (PPG02_0) TIOA3_1 INT19_1 MAD21_0 MNCLE_0	G	K
49	39	34	K4	P3D SOT13_0 (SDA13_0) RTO04_0 (PPG04_0) TIOA4_1 MAD20_0 MNWEX_0	G	I

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
59	49	41	L4	P43 SIN15_0 RTO13_0 (PPG12_0) TIOA3_0 INT04_0 MCSX4_0	G	K
60	50	42	M4	P44 SOT15_0 (SDA15_0) RTO14_0 (PPG14_0) TIOA4_0 MCSX3_0	G	I
61	51	43	N4	P45 SCK15_0 (SCL15_0) RTO15_0 (PPG14_0) TIOA5_0 MCSX2_0	G	I
62	52	44	P2	C	-	-
63	53	45	P3	VSS	-	-
64	54	46	P4	VCC	-	-
65	-	-	-	P4A SIN12_1 AIN0_1 INT04_2	E	K
66	-	-	-	P4B SOT12_1 (SDA12_1) BIN0_1	E	I
67	-	-	-	P4C SCK12_1 (SCL12_1) ZIN0_1	E	I
68	-	-	-	P4D SCS72_1 INT05_2	E	K
69	-	-	-	P4E SCS73_1	E	I
70	55	47	L5	P7D SCK1_1 (SCL1_1) DTTI1X_0 INT05_0 WKUP2 MCSX1_0	L	Q
71	56	48	M5	P7E ADTG_7 FRCK1_0 MCSX0_0	L	I
72	57	49	N5	INITX	B	C
73	58	50	P5	P46 X0A	P	S

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
161	131	107	C14	P83 UDP1	H	R
162	132	108	B14	VSS	-	-
163	133	109	A13	VCC	-	-
164	134	110	B13	P00 TRSTX	E	G
165	135	111	A12	P01 TCK SWCLK	E	G
166	136	112	C12	P02 TDI	E	G
167	137	113	B12	P03 TMS SWDIO	E	G
168	138	114	B11	P04 TDO SWO	E	G
169	139	-	C11	P90 INT12_1 Q_IO3_0	S	K
170	140	-	D11	P91 SIN5_1 INT13_1 Q_IO2_0	S	K
171	141	-	B10	P92 SOT5_1 (SDA5_1) INT14_1 Q_IO1_0	S	K
172	142	-	C10	P93 SCK5_1 (SCL5_1) INT15_1 Q_IO0_0	S	K
173	143	-	D10	P94 CTS5_1 Q_SCK_0	S	I
174	144	-	B9	P95 RTS5_1 Q_CS0_0	S	I
175	-	-	-	P96 INT12_2 Q_CS1_0	S	K
176	-	-	-	P97 INT13_2 Q_CS2_0	S	K
177	145	115	C9	PC0 E_RXER	K	V
178	146	116	B8	PC1 TIOB6_0 E_RX03	K	V
179	147	117	D9	PC2 TIOA6_0 E_RX02	K	V

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
GPIO	PA0	General-purpose I/O port A	2	2	2	B2
	PA1		3	3	3	C2
	PA2		4	4	4	C3
	PA3		5	5	5	D5
	PA4		6	6	6	D2
	PA5		7	7	7	D1
	PA6		8	8	8	D3
	PA7		9	9	9	D4
	PA8		14	13	10	E5
	PA9		15	14	11	F1
	PAA		16	15	12	F2
	PAB		17	16	13	F3
	PAC		18	17	14	F4
	PAD		23	18	15	F5
	PAE		24	19	16	F6
	PAF		25	20	17	G2
	PB0	General-purpose I/O port B	126	102	-	J10
	PB1		127	103	-	J9
	PB2		128	104	-	H10
	PB3		129	105	-	J14
	PB4		138	112	-	G13
	PB5		139	113	-	F14
	PB6		140	114	-	G12
	PB7		141	115	-	G11
	PB8		119	-	-	-
	PB9		120	-	-	-
	PBA		121	-	-	-
	PBB		122	-	-	-
	PBC		148	-	-	-
	PBD		149	-	-	-
	PBE		150	-	-	-
	PBF		151	-	-	-

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Multi-Function Serial 5	SIN5_0	Multi-function serial interface ch 5 input pin	147	121	97	F13
	SIN5_1		170	140	-	D11
	SOT5_0 (SDA5_0)	Multi-function serial interface ch 5 output pin. This pin operates as SOT5 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA5 when it is used in an I²C (operation mode 4).	146	120	96	F12
	SOT5_1 (SDA5_1)		171	141	-	B10
	SCK5_0 (SCL5_0)	Multi-function serial interface ch 5 clock I/O pin. This pin operates as SCK5 when it is used in a CSIO (operation mode 2) and as SCL5 when it is used in an I²C (operation mode 4).	145	119	95	F11
	SCK5_1 (SCL5_1)		172	142	-	C10
	CTS5_0	Multi-function serial interface ch 5 CTS input pin	144	118	94	F10
	CTS5_1		173	143	-	D10
	RTS5_0	Multi-function serial interface ch 5 RTS output pin	143	117	93	G9
	RTS5_1		174	144	-	B9
Multi-Function Serial 6	SIN6_0	Multi-function serial interface ch 6 input pin	96	79	63	L10
	SIN6_1		117	97	81	K14
	SOT6_0 (SDA6_0)	Multi-function serial interface ch 6 output pin. This pin operates as SOT6 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA6 when it is used in an I²C (operation mode 4).	97	80	64	K10
	SOT6_1 (SDA6_1)		118	98	82	K11
	SCK6_0 (SCL6_0)	Multi-function serial interface ch 6 clock I/O pin. This pin operates as SCK6 when it is used in a CSIO (operation mode 2) and as SCL6 when it is used in an I²C (operation mode 4).	98	81	65	M10
	SCK6_1 (SCL6_1)		126	102	-	J10
	SCS60_0	Multi-function serial interface ch 6 chip select 0 input/output pin	99	82	66	N11
	SCS60_1		127	103	-	J9
	SCS61_0	Multi-function serial interface ch 6 chip select1 input/output pin	100	83	67	M11
	SCS61_1		128	104	-	H10
	SCS62_0	Multi-function serial interface ch 6 chip select2 input/output pin	79	64	-	K6
	SCS62_1		129	105	-	J14
	SCS63_0	Multi-function serial interface ch 6 chip select3 input/output pin	78	63	-	K5
	SCS63_1		119	-	-	-

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Multi-Function Serial 15	SIN15_0	Multi-function serial interface ch 15 input pin	59	49	41	L4
	SIN15_1		19	-	-	-
	SOT15_0 (SDA15_0)	Multi-function serial interface ch 15 output pin. This pin operates as SOT15 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA15 when it is used in an I^2C (operation mode 4).	60	50	42	M4
	SOT15_1 (SDA15_1)		20	-	-	-
	SCK15_0 (SCL15_0)	Multi-function serial interface ch 15 clock I/O pin. This pin operates as SCK15 when it is used in a CSIO (operation mode 2) and as SCL15 when it is used in an I^2C (operation mode 4).	61	51	43	N4
	SCK15_1 (SCL15_1)		21	-	-	-

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Quadrature Position/ Revolution Counter 0	AIN0_0	QPRC ch 0 AIN input pin	56	46	38	N2
	AIN0_1		65	-	-	-
	AIN0_2		114	94	78	L11
	BIN0_0	QPRC ch 0 BIN input pin	57	47	39	N3
	BIN0_1		66	-	-	-
	BIN0_2		115	95	79	K13
	ZIN0_0	QPRC ch 0 ZIN input pin	58	48	40	M3
	ZIN0_1		67	-	-	-
	ZIN0_2		116	96	80	K12
Quadrature Position/ Revolution Counter 1	AIN1_0	QPRC ch 1 AIN input pin	91	76	60	K9
	AIN1_1		94	-	-	-
	AIN1_2		123	99	83	J13
	BIN1_0	QPRC ch 1 BIN input pin	92	77	61	P10
	BIN1_1		45	-	-	-
	BIN1_2		124	100	84	J12
	ZIN1_0	QPRC ch 1 ZIN input pin	93	78	62	N10
	ZIN1_1		101	-	-	-
	ZIN1_2		125	101	85	J11
Quadrature Position/ Revolution Counter 2	AIN2_0	QPRC ch 2 AIN input pin	2	2	2	B2
	AIN2_1		32	23	20	G5
	AIN2_2		120	-	-	-
	BIN2_0	QPRC ch 2 BIN input pin	3	3	3	C2
	BIN2_1		36	26	21	H2
	BIN2_2		121	-	-	-
	ZIN2_0	QPRC ch 2 ZIN input pin	4	4	4	C3
	ZIN2_1		37	27	22	J1
	ZIN2_2		122	-	-	-
Quadrature Position/ Revolution Counter 3	AIN3_0	QPRC ch 3 AIN input pin	18	17	14	F4
	AIN3_1		45	35	30	J2
	AIN3_2		149	-	-	-
	BIN3_0	QPRC ch 3 BIN input pin	23	18	15	F5
	BIN3_1		46	36	31	K1
	BIN3_2		150	-	-	-
	ZIN3_0	QPRC ch 3 ZIN input pin	24	19	16	F6
	ZIN3_1		47	37	32	K2
	ZIN3_2		151	-	-	-

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Ethernet	E_COL	Collision detection	186	154	124	F8
	E_COUT	Clock output for Ethernet PHY	190	158	128	A7
	E_CRS	Carrier detection	187	155	125	B7
	E_MDC	Management clock	184	152	122	E8
	E_MDIO	Management data I/O	183	151	121	D8
	E_PPS	PTP counter monitor	198	166	136	D6
	E_RX00	Received data0	181	149	119	F9
	E_RX01	Received data1	180	148	118	E9
	E_RX02	Received data2	179	147	117	D9
	E_RX03	Received data3	178	146	116	B8
	E_RXCK_REFCK	Received clock input/ Reference clock	185	153	123	A10
	E_RXDV	Received data enable	182	150	120	C8
	E_RXER	Received data error detection	177	145	115	C9
	E_TCK	Transition clock input	191	159	129	C7
	E_TX00	Transition data0	196	164	134	B6
	E_TX01	Transition data1	195	163	133	F7
	E_TX02	Transition data2	194	162	132	E7
	E_TX03	Transition data3	193	161	131	D7
	E_TXEN	Transition data enable	197	165	135	C6
	E_TXER	Transition data error detection	192	160	130	A6
I^2S	I2SMCLK0_0	I^2S external clock pin	51	41	-	L2
	I2SDO0_0	I^2S serial transition data output pin	52	42	-	L3
	I2SWS0_0	I^2S frame synchronization signal pin	53	43	-	M2
	I2SDI0_0	I^2S serial received data input pin	34	24	-	G6
	I2SCK0_0	I^2S bit clock pin	35	25	-	H4
High-speed quad SPI	Q_SCK_0	SPI clock output pin	173	143	-	D10
	Q_IO0_0	SPI data input/output pin	172	142	-	C10
	Q_IO1_0		171	141	-	B10
	Q_IO2_0		170	140	-	D11
	Q_IO3_0		169	139	-	C11
	Q_CS0_0	SPI chip select output pin	174	144	-	B9
	Q_CS1_0		175	-	-	-
	Q_CS2_0		176	-	-	-

List of Pin Behavior by Mode State

Pin Status Type	Function Group	Power-On Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC mode or Deep Standby Stop mode State		Return From Deep Standby mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
A	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	Main crystal oscillator input pin/ external main clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input Enabled
B	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	External main clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	Maintain previous state	Hi-Z/internal input fixed at 0	Maintain previous State
	Main crystal oscillator output pin	Hi-Z/ internal input fixed at 0/ or input enable	Hi-Z/ internal input fixed at 0	Hi-Z/ internal input fixed at 0	Maintain previous state while oscillator active/ When oscillation stops*1, it will be Hi-Z/ Internal input fixed at 0					
C	INITX input pin	Pull-up/ input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled
D	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
E	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ input enabled	GPIO selected	Hi-Z/ input enabled	GPIO selected

12.3 DC Characteristics

12.3.1 Current Rating

Table 12-1 Typical and Maximum Current Consumption in Normal Operation (PLL), Code Running from Flash Memory (Flash Accelerator Mode and Trace Buffer Function Enabled)

Parameter	Symbol	Pin Name	Conditions		Frequency*4	Value		Unit	Remarks
						Typ*1	Max*2		
Power supply current	I_{CC}	VCC	Normal operation *7,*8 (PLL)	*5	200 MHz	117	224	mA	*3 When all peripheral clocks are on
					192 MHz	113	219	mA	
					180 MHz	106	211	mA	
				*6	160 MHz	95	197	mA	
					144 MHz	86	186	mA	
					120 MHz	73	169	mA	
					100 MHz	61	155	mA	
					80 MHz	50	140	mA	
					60 MHz	39	126	mA	
					40 MHz	27	112	mA	
					20 MHz	16	97	mA	
					8 MHz	8.7	88.9	mA	
					4 MHz	6.4	86.1	mA	
				*5	200 MHz	71	168	mA	*3 When all peripheral clocks are off
					192 MHz	68	165	mA	
					180 MHz	64	159	mA	
				*6	160 MHz	58	151	mA	
					144 MHz	52	144	mA	
					120 MHz	44	134	mA	
					100 MHz	38	126	mA	
					80 MHz	31	117	mA	
					60 MHz	24	109	mA	
					40 MHz	17	100	mA	
					20 MHz	10	91	mA	
					8 MHz	6.3	86.1	mA	
					4 MHz	5.0	84.5	mA	

*1: T_A = +25°C, V_{CC} = 3.3 V

*2: T_J = +125°C, V_{CC} = 5.5 V

*3: When all ports are fixed

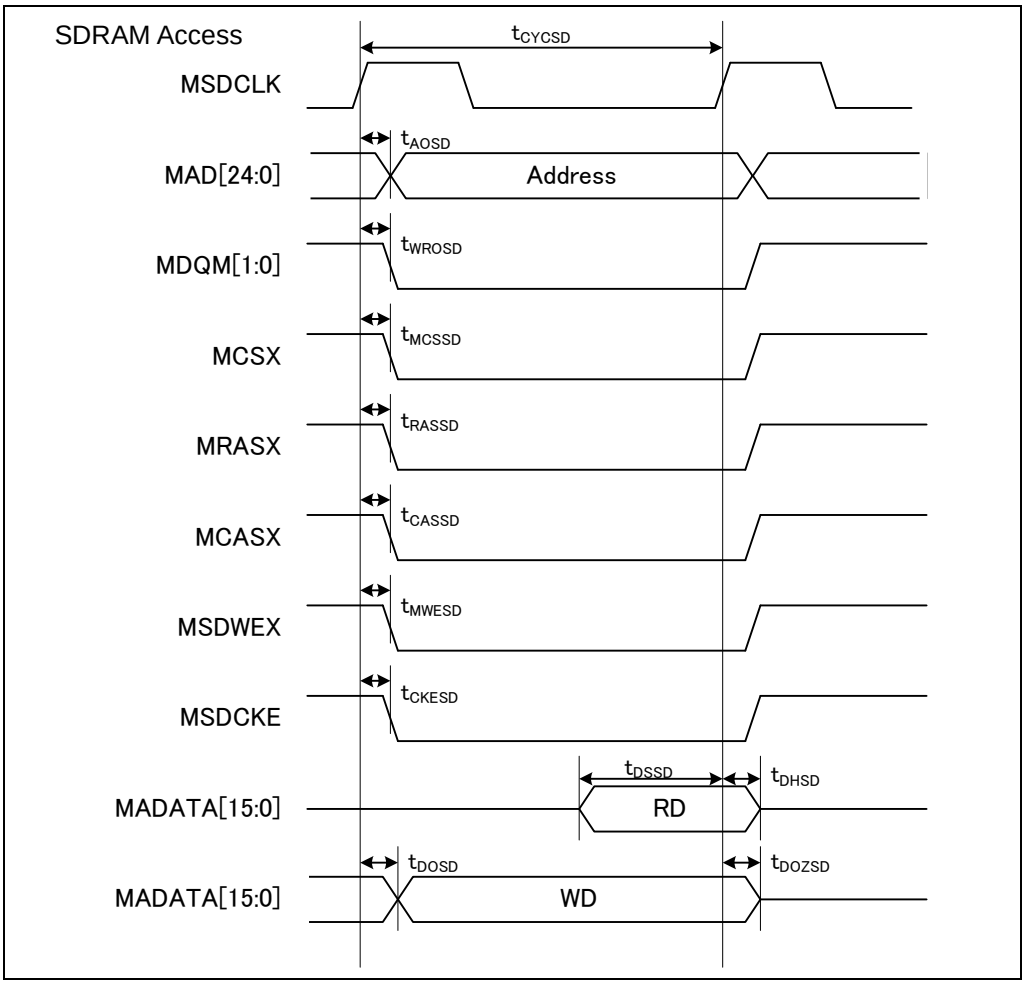
*4: Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK

*5: When stopping flash accelerator mode and trace buffer function (FRWTR.RWT = 11, FBFCR.BE = 1)

*6: When stopping flash accelerator mode and trace buffer function (FRWTR.RWT = 10, FBFCR.BE = 1)

*7: Firmware being executed during data collection for this table is not being accessed from the MainFlash memory."

*8: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)


SDRAM Access
tCYCSD
MSDCLK
tAOSD
MAD[24:0]
Address
tWROSD
MDQM[1:0]
tMCSSD
MCSX
tRASSD
MRASX
tCASSD
MCASX
tMWESD
MSDWEX
tCKESD
MSDCKE
tDSSD
tDHSD
MADATA[15:0]
RD
tDOSD
tDOZSD
MADATA[15:0]
WD

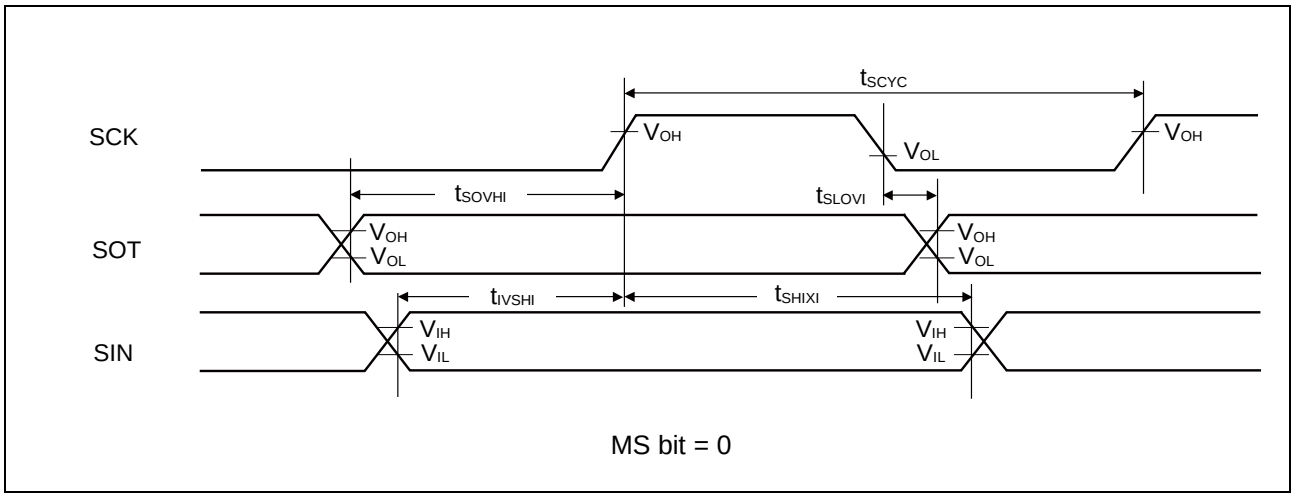
Synchronous Serial (SPI = 1, SCINV = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

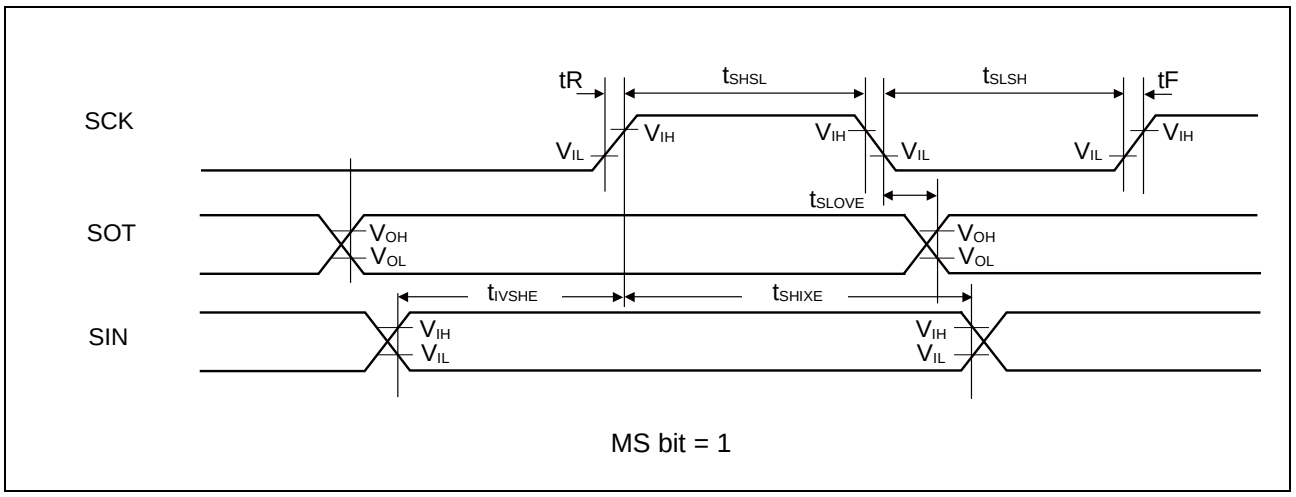
Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↓→SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN→SCK↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	30	-	ns
SCK↑→SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	ns
SOT→SCK↑ delay time	t_{SOVHI}	SCKx, SOTx		$2t_{CYCP}$ - 30	-	$2t_{CYCP}$ - 30	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↓→SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	-	30	ns
SIN→SCK↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK↑→SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK fall time	t_F	SCKx		-	5	-	5	ns
SCK rise time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.*
- *These characteristics only guarantee the same relocate port number; for example, the combination of SCKx_0 and SOTx_1 is not guaranteed.*
- *When the external load capacitance C_L = 30 pF.*



MS bit = 0



MS bit = 1

When Using Synchronous Serial Chip Select (SCINV = 0, CSLVL = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↓ setup time	t_{CSSI}	Internal shift clock operation	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↑→SCS↑ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	ns
SCS↓→SCK↓ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCK↑→SCS↑ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCS↓→SOT delay time	t_{DSE}		-	40	-	40	ns
SCS ↑ →SOT delay time	t_{DEE}		0	-	0	-	ns

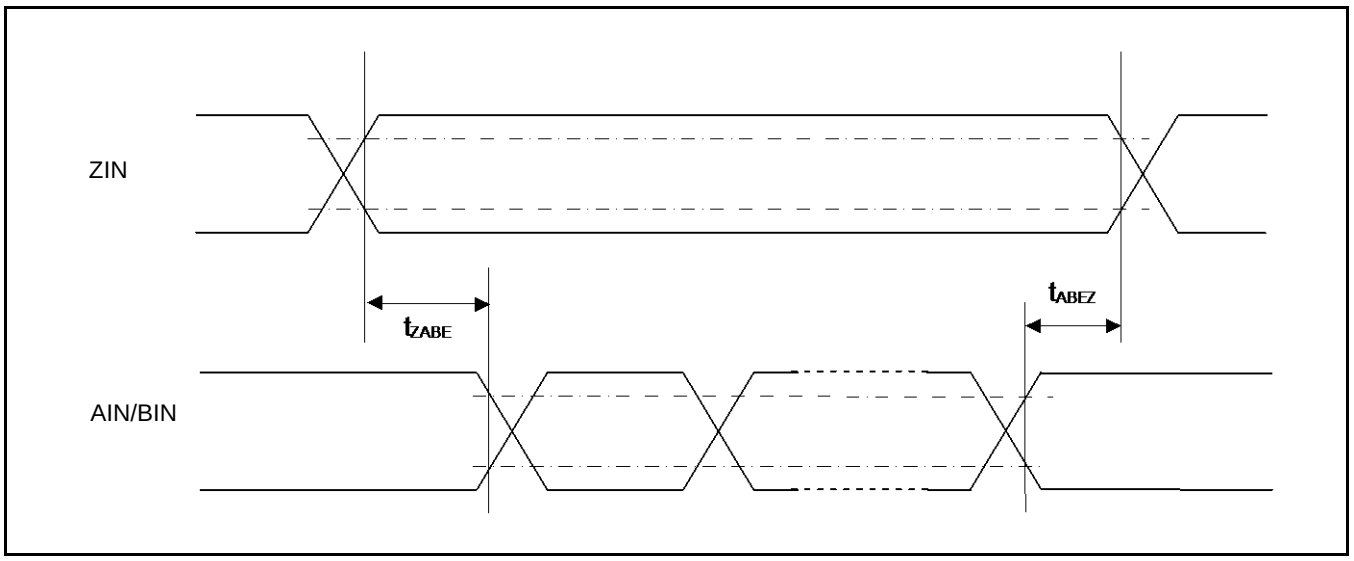
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.*
- *For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*


ZIN
AIN/BIN
tZABE
tABEZ

12.4.21 High-Speed Quad SPI Timing

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock frequency	t_{SCYCM}	Q_SCK_0	C_L = 15 pF, V_{CC} = 3.0 to 3.6V	-	66	MHz	*1
			C_L = 30 pF	-	50	MHz	*2
Enabled CS→ CLK Starting Time (mode0/mode2)	$t_{OSLSK02}$	Q_SCK_0, Q_CS0_0, Q_CS1_0, Q_CS2_0	C_L = 30 pF	$1.5 \times t_{SCYCM}$ - 5	-	ns	
Enabled CS→ CLK Starting Time (mode1/mode3)	$t_{OSLSK13}$			t_{SCYCM} - 5	-	ns	
CLK Last→ Disabled CS Time (mode0/mode2)	$t_{OSKSL02}$			t_{SCYCM}	-	ns	
CLK Last→ Disabled CS Time (mode1/mode3)	$t_{OSKSL13}$			$1.5 \times t_{SCYCM}$	-	ns	
SIO Data output time	t_{OSDAT}	Q_SCK_0, Q_IO0_0, Q_IO1_0, Q_IO2_0, Q_IO3_0	C_L = 15 pF, V_{CC} = 3.0 to 3.6V	0	5	ns	
			C_L = 30 pF	0	5		
SIO Setup	t_{DSSET}		C_L = 30 pF	3	-	ns	*1
				10	-		*2
SIO Hold	t_{SDHOLD}		C_L = 30 pF	$0.5 \times t_{SCYCM}$	-	ns	

*1: When RTM = 1 and mode = 0, 1, 3

*2: When RTM = 1 and mode = 2 or RTM = 0 and mode = 0, 1, 2, 3

Notes:

- *See Chapter 8-3: High-Speed Quad SPI controller in FM4 Family Peripheral Manual Communication Macro Part (002-04862) for the detail of RTM mode.*
- *When using High-Speed Quad SPI, please set PDSR register to set the pin drive capability for V_{CC} = 3V. See Chapter 12: I/O Port in FM4 Family Peripheral Manual Main Part (002-04856) for the details.*

12.5 12-bit A/D Converter

Electrical Characteristics for the A/D Converter

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = AVRL = 0V)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Integral nonlinearity	-	-	- 4.5	-	+ 4.5	LSB	AVRH = 2.7 V to 5.5 V
Differential nonlinearity	-	-	- 2.5	-	+ 2.5	LSB	
Zero transition voltage	V_{ZT}	ANxx	- 15	-	+ 15	mV	
Full-scale transition voltage	V_{FST}	ANxx	AVRH – 15	-	AVRH + 15	mV	
			AV_{CC} - 15	-	AV_{CC} + 15	mV	
Conversion time	-	-	0.5*1	-	-	µs	AV_{CC} ≥ 4.5 V
Sampling time *2	t_S	-	0.15	-	10	µs	AV_{CC} ≥ 4.5 V
			0.3	-			AV_{CC} < 4.5 V
Compare clock cycle*3	t_{CCK}	-	25	-	1000	ns	AV_{CC} ≥ 4.5 V
			50	-	1000		AV_{CC} < 4.5 V
State transition time to operation permission	t_{STT}	-	-	-	1.0	µs	
Power supply current (analog + digital)	-	AVCC	-	0.69	0.92	mA	A/D 1 unit operation
			-	1.3	22	µA	When A/D stop
Reference power supply current (AVRH)	-	AVRH	-	1.1	1.97	mA	A/D 1 unit operation AVRH = 5.5 V
			-	0.3	6.3	µA	When A/D stop
Analog input capacity	C_{AIN}	-	-	-	12.05	pF	
Analog input resistance	R_{AIN}	-	-	-	1.2	kΩ	AV_{CC} ≥ 4.5 V
					1.8		AV_{CC} < 4.5 V
Interchannel disparity	-	-	-	-	4	LSB	
Analog port input leak current	-	ANxx	-	-	5	µA	
Analog input voltage	-	ANxx	AV_{SS}	-	AVRH	V	
			AV_{SS}	-	AV_{CC}	V	
Reference voltage	-	AVRH	4.5	-	AV_{CC}	V	Tcck < 50 ns
			2.7	-	AV_{CC}		Tcck ≥ 50 ns
	-	AVRL	AV_{SS}	-	AV_{SS}	V	

*1: The conversion time is the value of sampling time (t_S) + compare time (t_C).
The condition of the minimum conversion time is when the value of t_S = 150 ns and Tc = 350 ns (AV_{CC} ≥ 4.5V). Ensure that it satisfies the value of sampling time (t_S) and compare clock cycle (t_{CCK}). For setting of sampling time and compare clock cycle, see Chapter 1-1: A/D Converter in FM4 Family Peripheral Manual Analog Macro Part (002-04860). The register setting of the A/D converter is reflected by the APB bus clock timing. For more information about the APB bus number to which the A/D converter is connected, see 8. Block Diagram in this data sheet.
The sampling and compare clock are set at base clock (HCLK).

*2: A necessary sampling time changes by external impedance. Ensure that it sets the sampling time to satisfy (Equation 1).

*3: The compare time (t_C) is the value of (Equation 2).

12.6 12-bit D/A Converter

Electrical Characteristics for the D/A Converter

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	DAx	-	-	12	bit	
Conversion time	t_{C20}		0.56	0.69	0.81	µs	Load 20 pF
	t_{C100}		2.79	3.42	4.06	µs	Load 100 pF
Integral nonlinearity *	INL		- 16	-	+ 16	LSB	
Differential nonlinearity *	DNL		- 0.98	-	+ 1.5	LSB	
Output voltage offset	V_{OFF}		-	-	+ 10	mV	When setting 0x000
			- 20.0	-	+ 1.4	mV	When setting 0xFFF
Analog output impedance	R_O		3.10	3.80	4.50	kΩ	D/A operation
			2.0	-	-	MΩ	When D/A stop
Power supply current *	IDDA	AVCC	260	330	410	µs	D/A 1ch operation AV_{CC} = 3.3 V
			400	510	620	µs	D/A 1ch operation AV_{CC} = 5.0 V
	IDSA		-	-	14	µs	When D/A stop

*: During no load

12.9 MainFlash Memory Write/Erase Characteristics

(V_{CC} = 2.7V to 5.5V)

Parameter		Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	Large Sector	-	0.7	3.7	s	Includes write time prior to internal erase
	Small Sector	-	0.3	1.1	s	
Half word (16-bit) write time	Write cycles ≤ 100 times	-	12	100	µs	Not including system-level overhead time
	Write cycles > 100 times			200		
Chip erase time*		-	13.6	68	s	Includes write time prior to internal erase

*: It indicates the chip erase time of 1MB MainFlash memory

For devices with 1.5 MB or 2 MB of MainFlash memory, two erase cycles are required.

See 3.2.2 Command Operating Explanations and 3.3.3 Flash Erase Operation in this product's Flash Programming Manual for the detail.

Write Cycles and Data Retention Time

Erase/Write Cycles (Cycle)	Data Retention Time (Year)
1,000	20*
10,000	10*
100,000	5*

*: This value comes from the technology qualification (using Arrhenius equation to translate high temperature acceleration test result into average temperature value at + 85°C).

12.10 Dual Flash Memory Write/Erase Characteristics

It is the same write/erase characteristics as the MainFlash memory.

See 3.6 Dual flash mode in this product's Flash Programming Manual for the detail of dual flash mode.