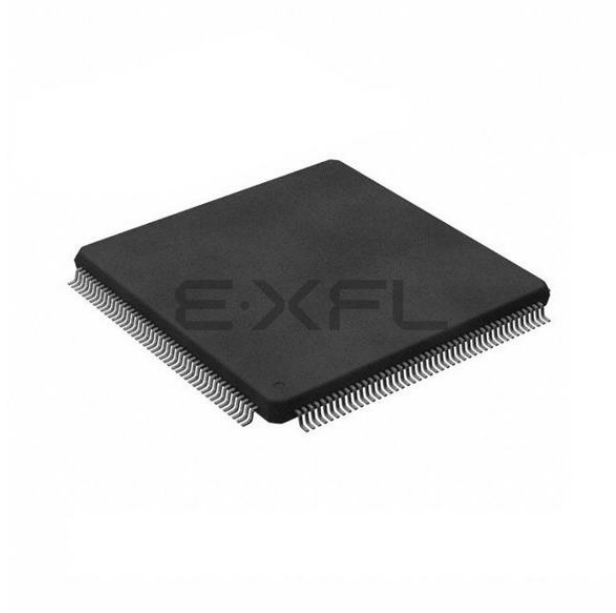

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What is "Embedded - Microcontrollers"?

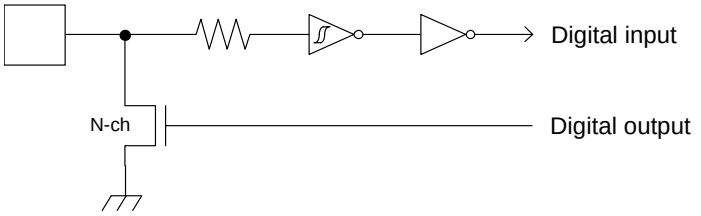
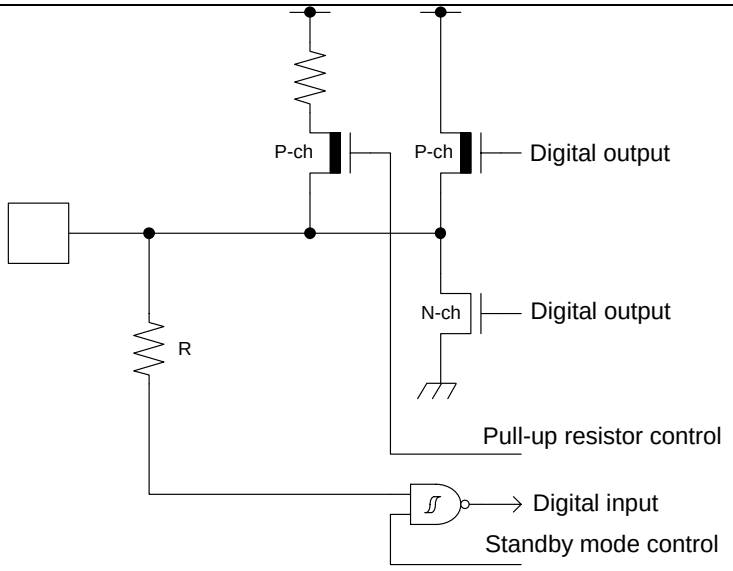
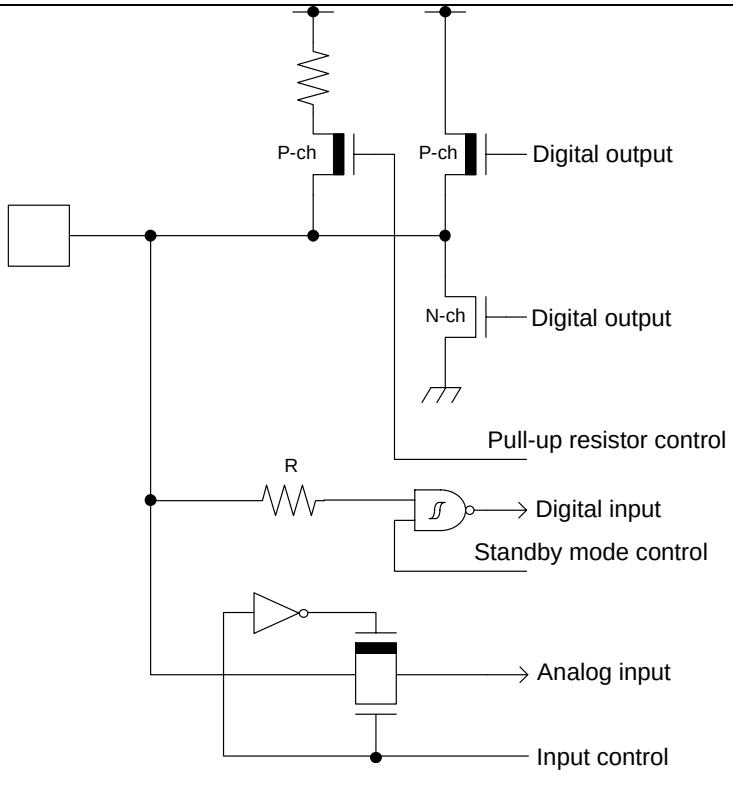
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CSIO, EBI/EMI, Ethernet, I²C, LINbus, SD, SPI, UART/USART, USB
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	152
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2c2aj0agv2000a

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
135	111	91	H11	P1D AN13 SCK12_0 (SCL12_0) TIOB5_2 TRACED3	F	N
136	-	-	-	VSS	-	-
137	-	-	-	VCC	-	-
138	112	-	G13	PB4 AN20 SIN8_1 TIOA11_1 INT10_1 TRACED4	F	O
139	113	-	F14	PB5 AN21 SOT8_1 (SDA8_1) TIOB11_1 INT11_1 TRACED5	F	O
140	114	-	G12	PB6 AN22 SCK8_1 (SCL8_1) TIOA12_1 TRACED6	F	N
141	115	-	G11	PB7 AN23 TIOB12_1 TRACED7	F	N
142	116	92	G10	P1E AN14 TIOA8_1 INT26_1 MAD10_0	F	M
143	117	93	G9	P1F AN15 RTS5_0 TIOB8_1 INT27_1 MAD11_0	F	M
144	118	94	F10	P2A AN24 CTS5_0 MAD12_0	F	L
145	119	95	F11	P29 AN25 SCK5_0 (SCL5_0) MAD13_0	F	L
146	120	96	F12	P28 AN26 SOT5_0 (SDA5_0) MAD14_0	F	L

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
GPIO	P00	General-purpose I/O port 0	164	134	110	B13
	P01		165	135	111	A12
	P02		166	136	112	C12
	P03		167	137	113	B12
	P04		168	138	114	B11
	P08		30	21	18	G3
	P09		31	22	19	G4
	P0A		32	23	20	G5
	P10	General-purpose I/O port 1	114	94	78	L11
	P11		115	95	79	K13
	P12		116	96	80	K12
	P13		117	97	81	K14
	P14		118	98	82	K11
	P15		123	99	83	J13
	P16		124	100	84	J12
	P17		125	101	85	J11
	P18		130	106	86	H9
	P19		131	107	87	H12
	P1A		132	108	88	H14
	P1B		133	109	89	G14
	P1C		134	110	90	H13
	P1D		135	111	91	H11
	P1E		142	116	92	G10
	P1F		143	117	93	G9
	P20	General-purpose I/O port 2	158	128	104	C13
	P21		157	127	103	D13
	P22		156	126	102	D12
	P23		155	125	101	E13
	P24		154	124	100	E12
	P25		153	123	99	E11
	P26		152	122	98	E10
	P27		147	121	97	F13
	P28		146	120	96	F12
	P29		145	119	95	F11
	P2A		144	118	94	F10

Type	Circuit	Remarks
C		• Open drain output • CMOS level hysteresis input
E		• CMOS level output • CMOS level hysteresis input • Pull-up resistor control • Standby mode control • Pull-up resistor: approximately 50 kΩ • I_{OH} = -4 mA, I_{OL} = 4 mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off.
F		• CMOS level output • CMOS level hysteresis input • Input control • Analog input • Pull-up resistor control • Standby mode control • Pull-up resistor: approximately 50 kΩ • I_{OH} = -4 mA, I_{OL} = 4 mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off.

6.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity

   Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

2. Discharge of static electricity

   When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

3. Corrosive gases, dust, or oil

   Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

4. Radiation, including cosmic radiation

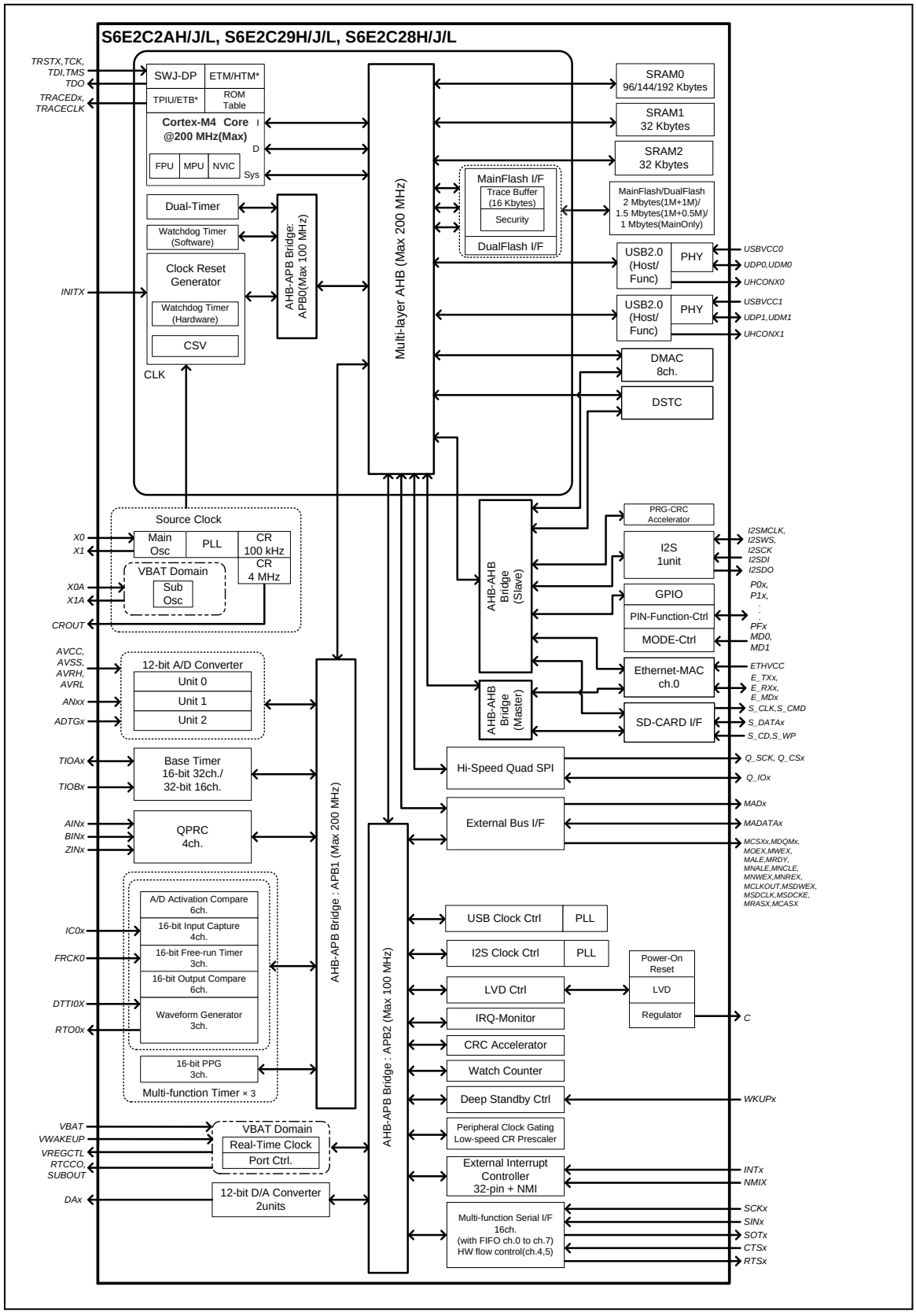
   Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

5. Smoke, flame

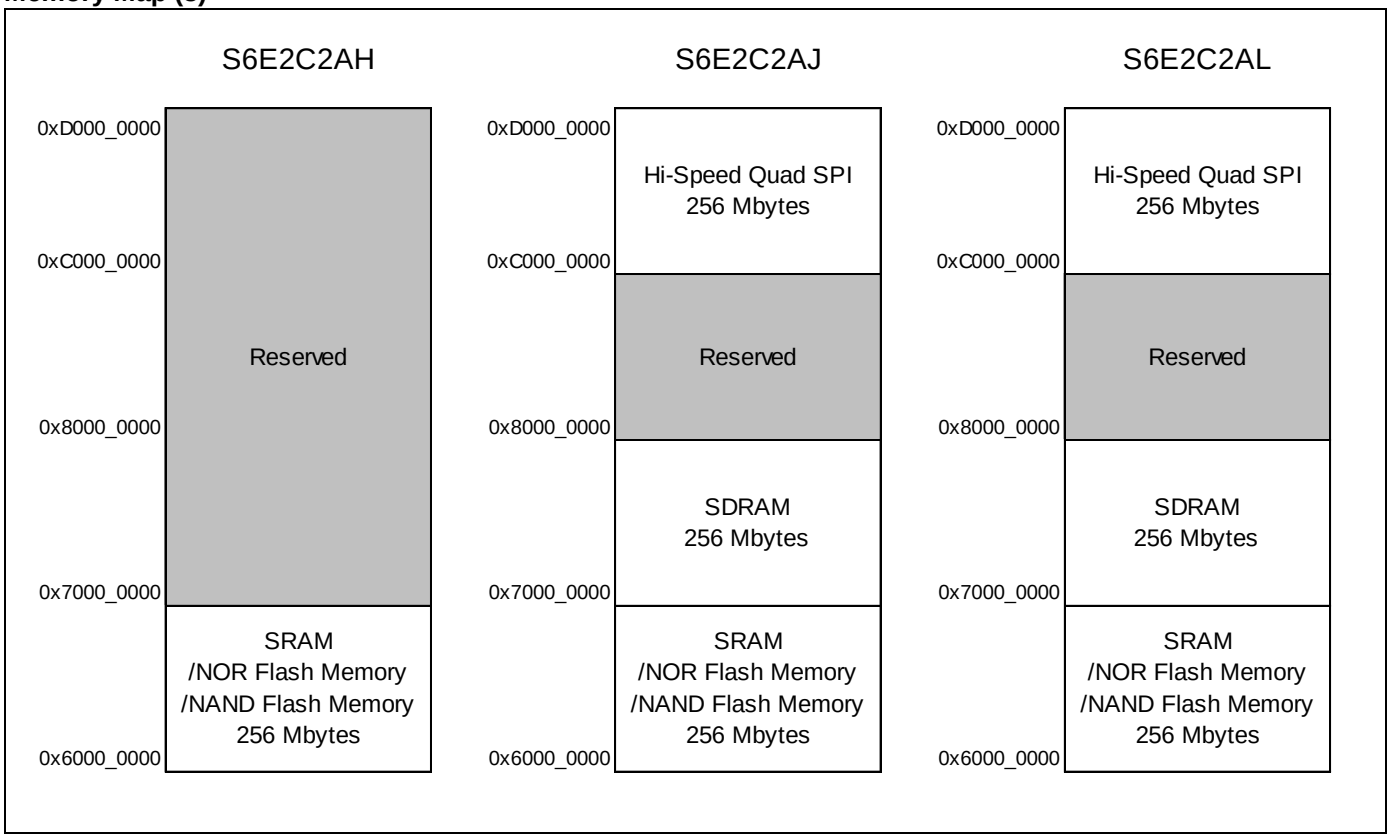
   CAUTION: Plastic molded devices are flammable and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

8. Block Diagram



Memory Map (3)


S6E2C2AH
0xD000_0000
0xC000_0000
0x8000_0000
0x7000_0000
0x6000_0000
Reserved
SRAM
/NOR Flash Memory
/NAND Flash Memory
256 Mbytes
S6E2C2AJ
0xD000_0000
0xC000_0000
0x8000_0000
0x7000_0000
0x6000_0000
Hi-Speed Quad SPI
256 Mbytes
Reserved
SDRAM
256 Mbytes
SRAM
/NOR Flash Memory
/NAND Flash Memory
256 Mbytes
S6E2C2AL
0xD000_0000
0xC000_0000
0x8000_0000
0x7000_0000
0x6000_0000
Hi-Speed Quad SPI
256 Mbytes
Reserved
SDRAM
256 Mbytes
SRAM
/NOR Flash Memory
/NAND Flash Memory
256 Mbytes

11. Pin Status in Each CPU State

The terms used for pin status have the following meanings:

- INITX = 0

  This is the period when the INITX pin is at the L level.

- INITX = 1

  This is the period when the INITX pin is at the H level.

- SPL = 0

  This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to 0.

- SPL = 1

  This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to 1.

- Input enabled

  Indicates that the input function can be used.

- Internal input fixed at 0

  This is the status that the input function cannot be used. Internal input is fixed at L.

- Hi-Z

  Indicates that the pin drive transistor is disabled and the pin is put in the Hi-Z state.

- Setting disabled

  Indicates that the setting is disabled.

- Maintain previous state

  Maintains the state that was immediately prior to entering the current mode.
  If a built-in peripheral function is operating, the output follows the peripheral function.
  If the pin is being used as a port, that output is maintained.

- Analog input is enabled

  Indicates that the analog input is enabled.

- Trace output

  Indicates that the trace function can be used.

- GPIO selected

  In Deep standby mode, pins switch to the general-purpose I/O port.

- Setting prohibition

  Prohibition of a setting by specification limitation

List of VBAT Domain Pin Status

VBAT Pin Status Type	Function Group	Power-on reset*1	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC mode or Deep Standby Stop mode State		Return From Deep Standby mode State	VBAT RTC mode State	Return From VBAT RTC mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable	Power Supply Stable	Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1	-	-
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-	-	-
S	GPIO selected	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Setting prohibition	-
	Sub crystal oscillator input pin/ external sub clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Maintain previous state	Maintain previous state
T	GPIO selected	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Setting prohibition	-
	External sub clock input selected	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	Sub crystal oscillator output pin	Hi-Z/ internal input fixed at 0/ or input enable	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state/ When oscillation stops, Hi-Z*2	Maintain previous state/ When oscillation stops, Hi-Z*2	Maintain previous state/ When oscillation stops, Hi-Z*2	Maintain previous state/ When oscillation stops, Hi-Z*2	Maintain previous state	Maintain previous state	Maintain previous state
U	Resource selected	Hi-Z	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected											

*1: When VBAT and VCC power on.

*2: When the SOSCNTL bit in the WTOSCCNT register is 0, the sub crystal oscillator output pin is maintained in the previous state. When the SOSCNTL bit in the WTOSCCNT register is 1, oscillation is stopped at Stop mode and Deep Standby Stop mode

*6: Ensure that the voltage does not exceed V_{CC} + 0.5 V, for example, when the power is turned on.

*7: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

*8: The average output current is defined as the average current value flowing through any one of the corresponding pins for a 100-ms period.

*9: The total average output current is defined as the average current value flowing through all of corresponding pins for a 100-ms period.

WARNING:

- *Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.*

Table 12-2 Typical and Maximum Current Consumption in Normal Operation (PLL), Code with Data Accessing Running from Flash Memory (Flash Accelerator Mode and Trace Buffer Function Disabled)

Parameter	Symbol	Pin Name	Conditions		Frequency*4	Value		Unit	Remarks
						Typ*1	Max*2		
Power supply current	I_{CC}	VCC	Normal operation *7,*8 (PLL)	*5	200 MHz	128	236	mA	*3 When all peripheral clocks are on
					192 MHz	123	230	mA	
					180 MHz	116	221	mA	
				*6	160 MHz	102	205	mA	
					144 MHz	93	193	mA	
					120 MHz	79	175	mA	
					100 MHz	67	161	mA	
					80 MHz	54	145	mA	
					60 MHz	42	130	mA	
					40 MHz	30	115	mA	
					20 MHz	17	99	mA	
					8 MHz	9.2	90.0	mA	
					4 MHz	6.7	86.9	mA	
				*5	200 MHz	74	170	mA	*3 When all peripheral clocks are off
					192 MHz	71	167	mA	
					180 MHz	67	162	mA	
				*6	160 MHz	59	152	mA	
					144 MHz	53	145	mA	
					120 MHz	45	135	mA	
					100 MHz	39	127	mA	
					80 MHz	32	118	mA	
					60 MHz	25	110	mA	
					40 MHz	18	101	mA	
					20 MHz	11	92	mA	
					8 MHz	6.5	86.8	mA	
					4 MHz	5.1	85.0	mA	

*1: T_A = +25°C, V_{CC} = 3.3 V

*2: T_J = +125°C, V_{CC} = 5.5 V

*3: When all ports are fixed

*4: Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK

*5: When stopping flash accelerator mode and trace buffer function (FRWTR.RWT = 11, FBFCR.BE = 0)

*6: When stopping flash accelerator mode and trace buffer function (FRWTR.RWT = 10, FBFCR.BE = 0)

*7: With data access to a MainFlash memory.

*8: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

NAND Flash Mode

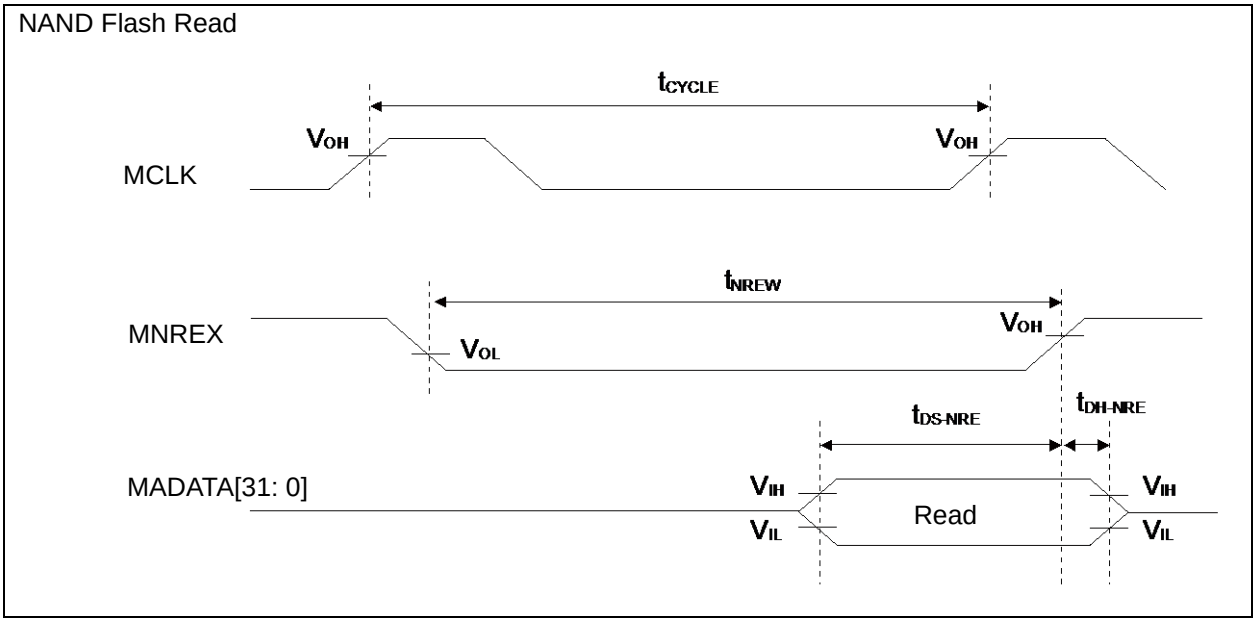
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
MNREX Min pulse width	t_{NREW}	MNREX	-	MCLK×n-3	-	ns	
Data set up →MNREX ↑ time	t_{DS-NRE}	MNREX, MADATA[31: 0]	-	20	-	ns	
MNREX ↑ → Data hold time	t_{DH-NRE}	MNREX, MADATA[31: 0]	-	0	-	ns	
MNALE ↑ → MNWEX delay time	$t_{ALEH-NWEL}$	MNALE, MNWEX	-	MCLK×m-9	MCLK×m+9	ns	
MNALE ↓ → MNWEX delay time	$t_{ALEL-NWEL}$	MNALE, MNWEX	-	MCLK×m-9	MCLK×m+9	ns	
MNCLE ↑ → MNWEX delay time	$t_{CLEH-NWEL}$	MNCLE, MNWEX	-	MCLK×m-9	MCLK×m+9	ns	
MNWEX ↑ → MNCLE delay time	$t_{NWEH-CLEL}$	MNCLE, MNWEX	-	0	MCLK×m+9	ns	
MNWEX Min pulse width	t_{NWEW}	MNWEX	-	MCLK×n-3	-	ns	
MNWEX ↓ → Data output time	$t_{NWEL-DV}$	MNWEX, MADATA[31: 0]	-	-9	9	ns	
MNWEX ↑ → Data hold time	$t_{NWEH-DX}$	MNWEX, MADATA[31: 0]	-	0	MCLK×m+9	ns	

Note:

- *When the external load capacitance C_L = 30 pF (m = 0 to 15, n = 1 to 16)*

NAND Flash Read



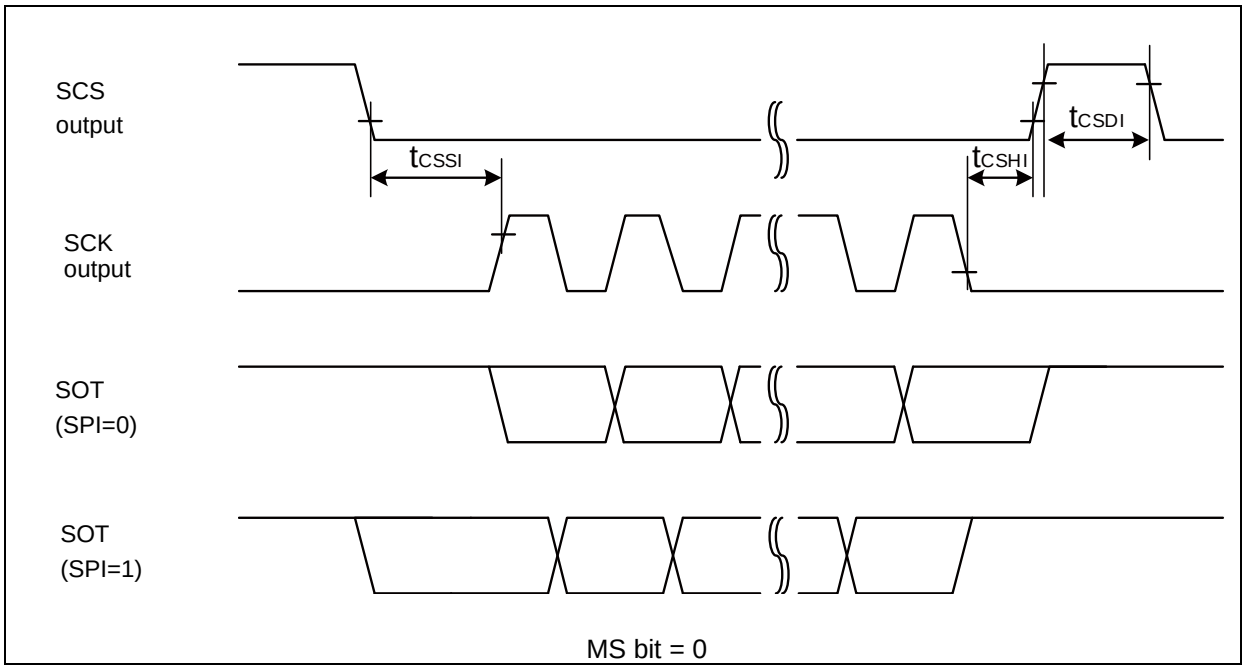
SDRAM Mode

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

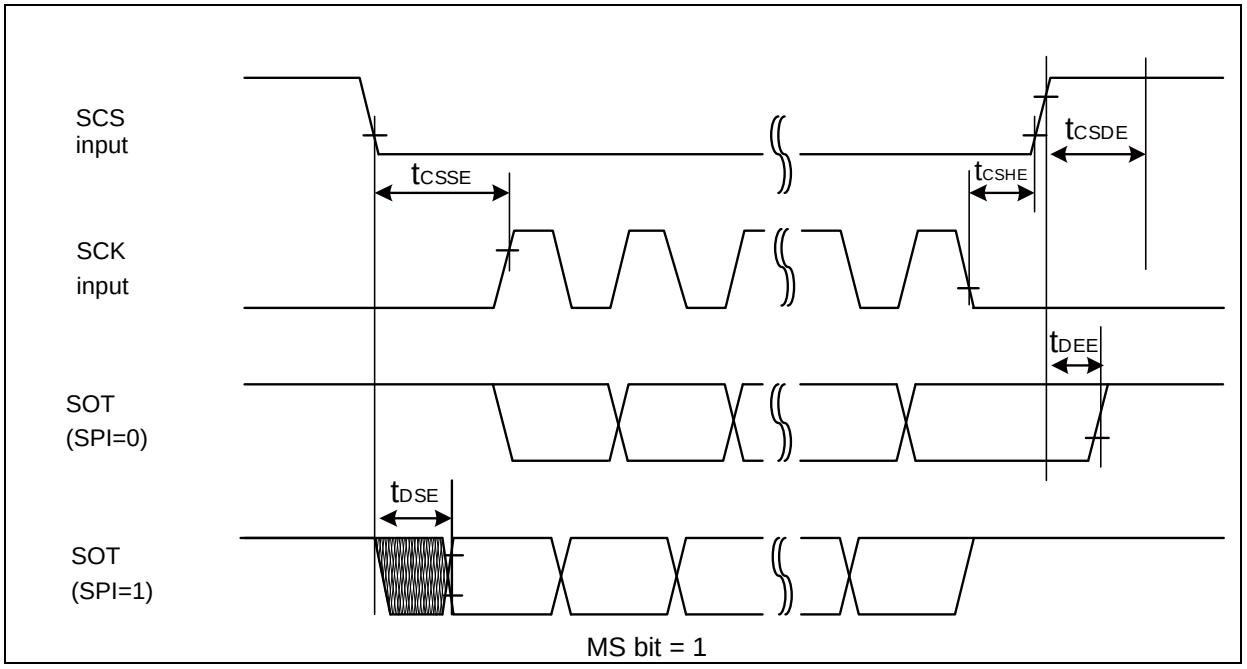
Parameter	Symbol	Pin Name	Value	Unit		Unit	Remarks
				Min	Max		
Output frequency	t_{CYCSD}	MSDCLK	-	-	50	MHz	
Address delay time	t_{AOSD}	MSDCLK, MAD[15: 0]	-	2	12	ns	
MSDCLK ↑ → Data output delay time	t_{DOSD}	MSDCLK, MADATA[31: 0]	-	2	12	ns	
MSDCLK ↑ → Data output Hi-Z time	t_{DOZSD}	MSDCLK, MADATA[31: 0]	-	2	19.5	ns	
MDQM[3: 0] delay time	t_{WROSD}	MSDCLK, MDQM[1: 0]	-	1	12	ns	
MCSX delay time	t_{MCSSD}	MSDCLK, MCSX8	-	2	12	ns	
MRASX delay time	t_{RASSD}	MSDCLK, MRASX	-	2	12	ns	
MCASX delay time	t_{CASSD}	MSDCLK, MCASX	-	2	12	ns	
MSDWEX delay time	t_{MWESD}	MSDCLK, MSDWEX	-	2	12	ns	
MSDCKE delay time	t_{CKESD}	MSDCLK, MSDCKE	-	2	12	ns	
Data set up time	t_{DSSD}	MSDCLK, MADATA[31: 0]	-	19	-	ns	
Data hold time	t_{DHSD}	MSDCLK, MADATA[31: 0]	-	0	-	ns	

Note:

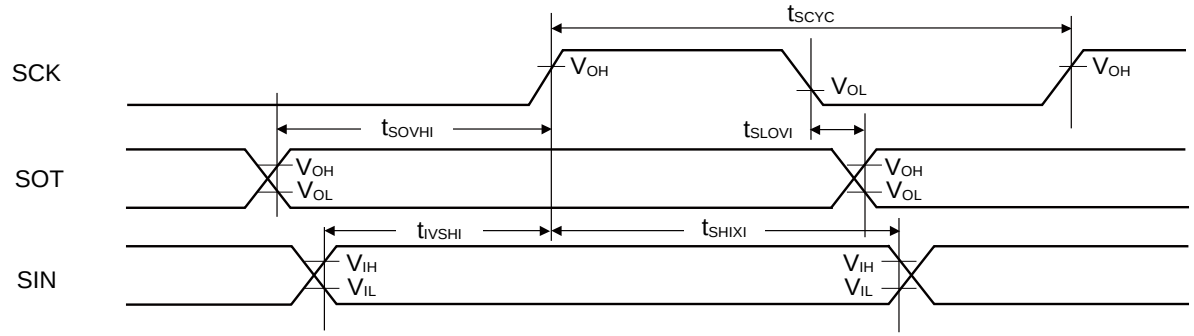
- *When the external load capacitance C_L = 30 pF*



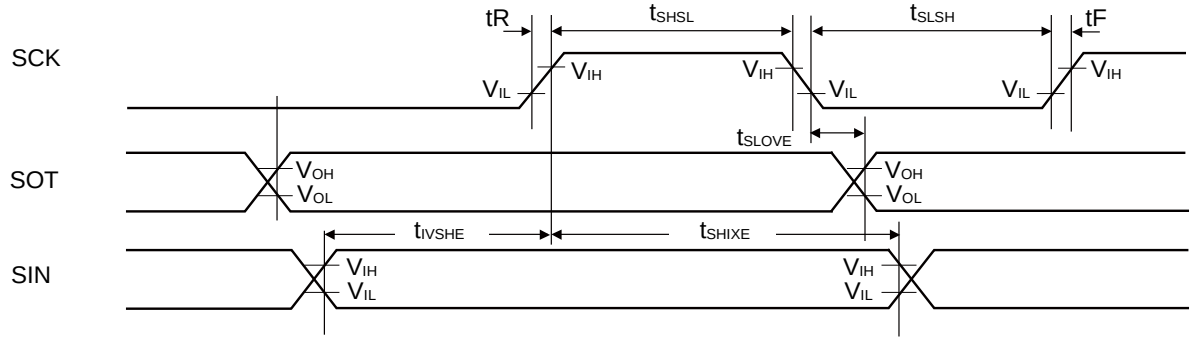
MS bit = 0



MS bit = 1



MS bit = 0



MS bit = 1

When Using High-Speed Synchronous Serial Chip Select (SCINV = 0, CSLVL = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↑→SCK↓ setup time	t_{CSSI}	Internal shift clock operation	(*1)-20	(*1)+0	(*1)-20	(*1)+0	ns
SCK↑→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+20	(*2)+0	(*2)+20	ns
SCS deselect time	t_{CSDI}		(*3)-20 +5t_{CYCP}	(*3)+20 +5t_{CYCP}	(*3)-20 +5t_{CYCP}	(*3)+20 +5t_{CYCP}	ns
SCS↑→SCK↓ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCK↑→SCS↓ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCS↑→SOT delay time	t_{DSE}		-	25	-	25	ns
SCS↓→SOT delay time	t_{DEE}		0	-	0	-	ns

(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

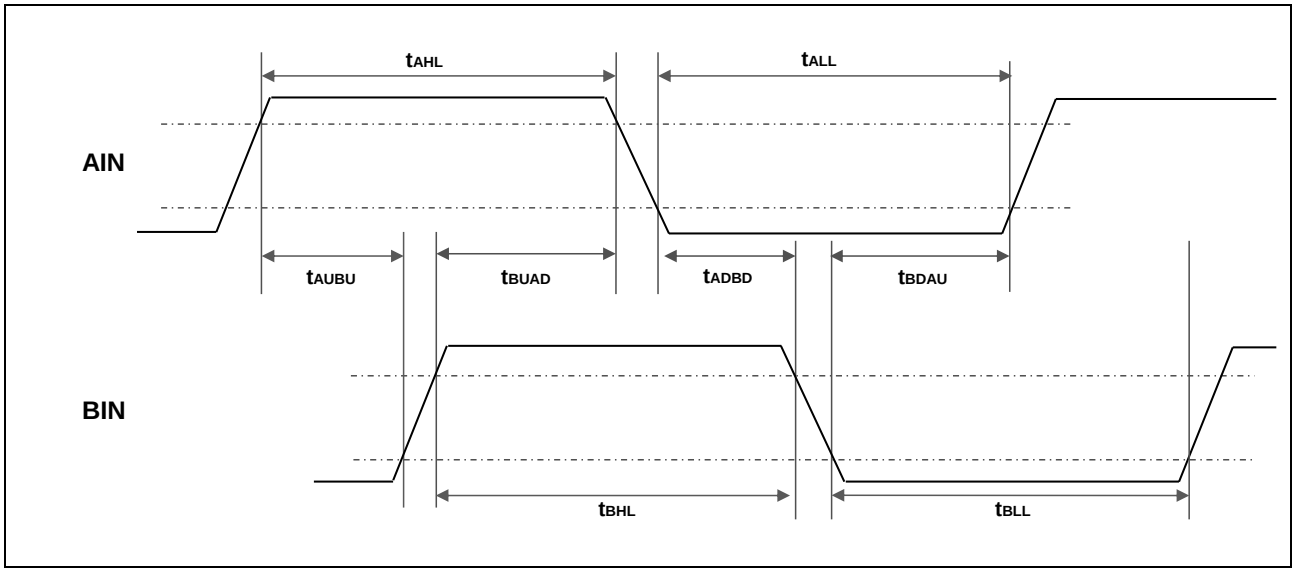
- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.*
- *For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*

12.4.14 Quadrature Position/Revolution Counter Timing

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = -40°C to +105°C)

Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
AIN pin H width	t_{AHL}	-	$2t_{CYCP}$*	-	ns
AIN pin L width	t_{ALL}	-			
BIN pin H width	t_{BHL}	-			
BIN pin L width	t_{BLL}	-			
BIN rise time from AIN pin H level	t_{AUBU}	PC_Mode2 or PC_Mode3			
AIN fall time from BIN pin H level	t_{BUAD}	PC_Mode2 or PC_Mode3			
BIN fall time from AIN pin L level	t_{ADBD}	PC_Mode2 or PC_Mode3			
AIN rise time from BIN pin L level	t_{BDAU}	PC_Mode2 or PC_Mode3			
AIN rise time from BIN pin H level	t_{BUAU}	PC_Mode2 or PC_Mode3			
BIN fall time from AIN pin H level	t_{AUBD}	PC_Mode2 or PC_Mode3			
AIN fall time from BIN pin L level	t_{BDAD}	PC_Mode2 or PC_Mode3			
BIN rise time from AIN pin L level	t_{ADBU}	PC_Mode2 or PC_Mode3			
ZIN pin H width	t_{ZHL}	QCR: CGSC = 0			
ZIN pin L width	t_{ZLL}	QCR: CGSC = 0			
AIN/BIN rise and fall time from determined ZIN level	t_{ZABE}	QCR: CGSC = 1			
Determined ZIN level from AIN/BIN rise and fall time	t_{ABEZ}	QCR: CGSC = 1			

*: t_{CYCP} indicates the APB bus clock cycle time except when in Stop mode, in Timer mode. For more information about the APB bus number to which the quadrature position/revolution counter is connected, see "8. Block Diagram" in this data sheet.

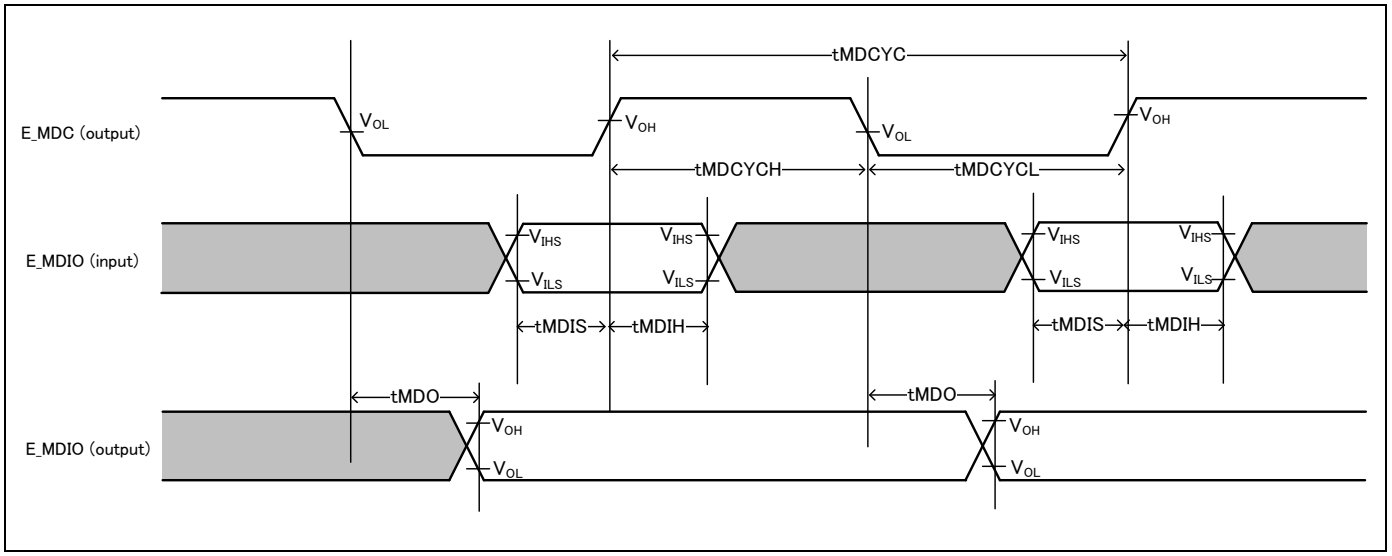


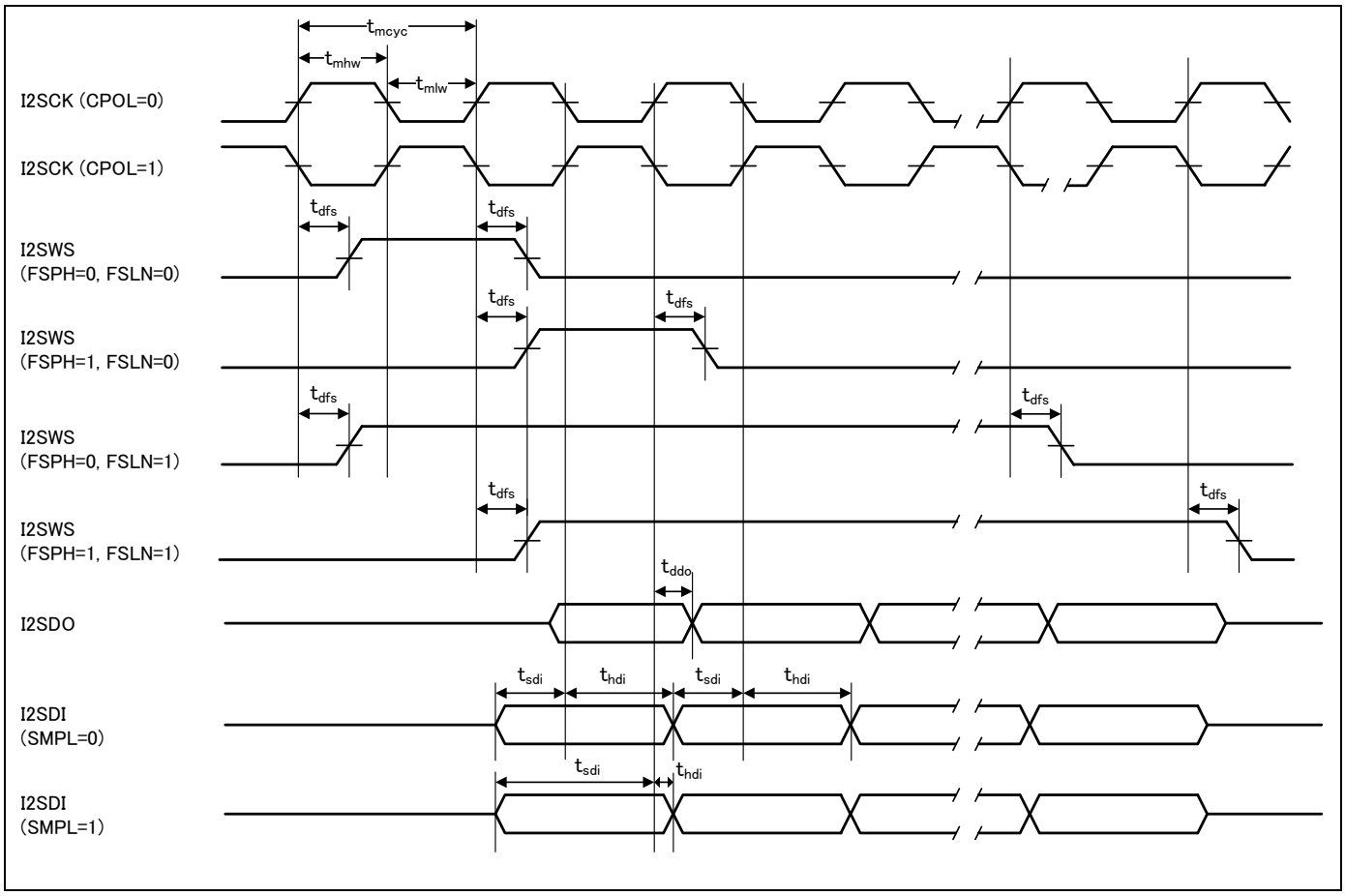
Management Interface

($ETHV_{CC}$ = 3.0V to 3.6V, 4.5V to 5.5V, V_{SS} = 0V, C_L = 25 pF)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Management clock cycle time*	t_{MDCYC}	E_MDC	-	400	-	ns
Management clock High pulse width duty cycle	t_{MDCYCH}	E_MDC	t_{MDCYCH}/t_{MDCYC}	35	65	%
Management clock Low pulse width duty cycle	t_{MDCYCL}	E_MDC	t_{MDCYCL}/t_{MDCYC}	35	65	%
MDC ↓ → MDIO Delay time	t_{MDO}	E_MDIO	-	-	60	ns
MDIO → MDC ↑ Setup time	t_{MDIS}	E_MDIO	-	20	-	ns
MDC ↑ → MDIO Hold time	t_{MDIH}	E_MDIO	-	0	-	ns

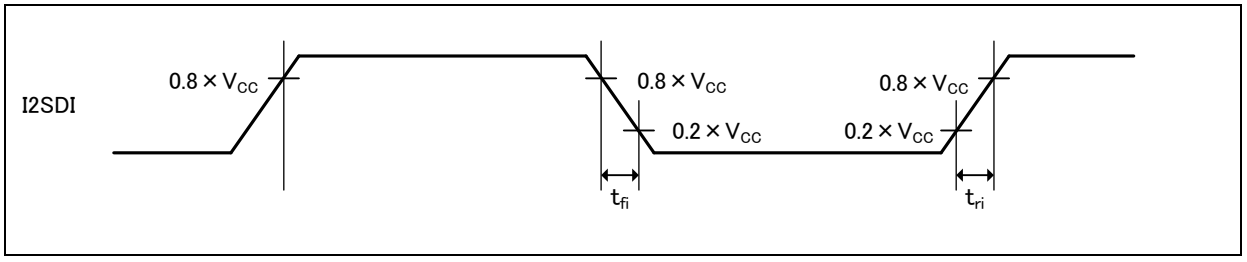
*: The clock time should be set to a value greater than the minimum value by setting the Ethernet-MAC setting register.

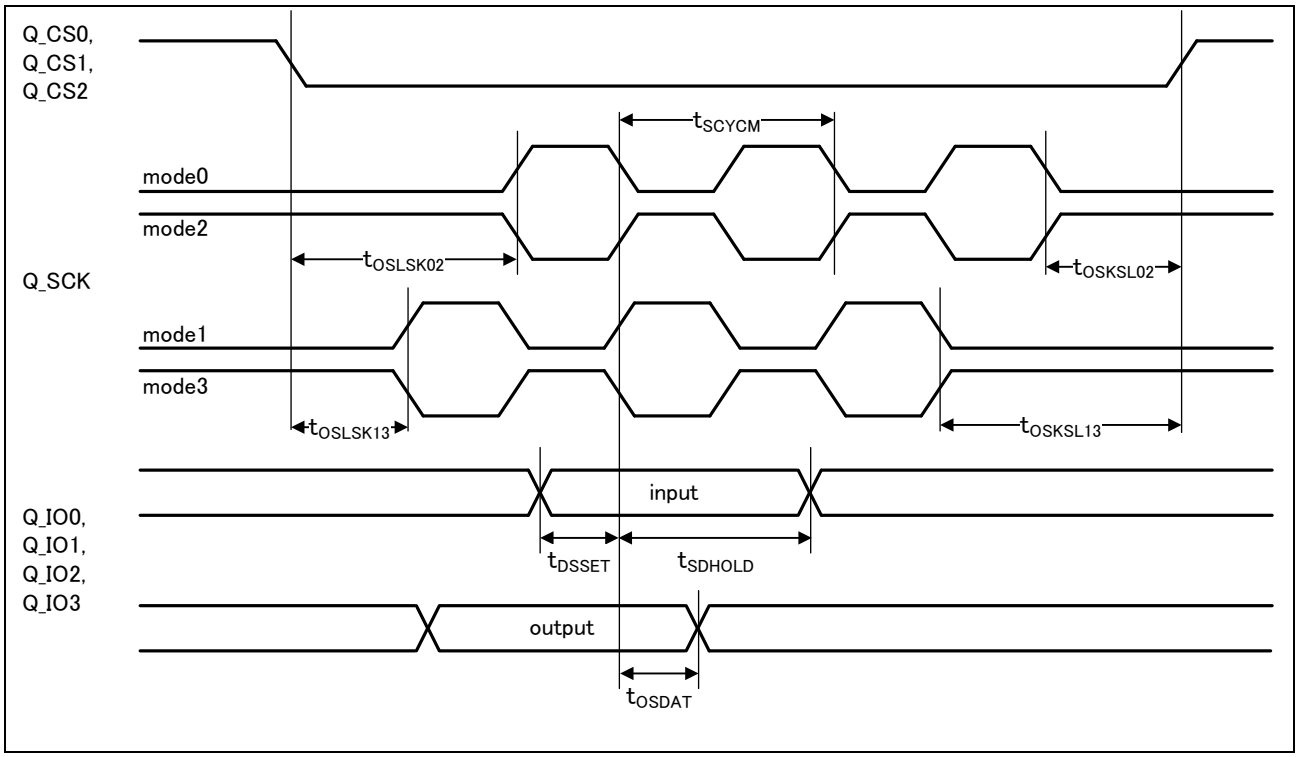




Note:

- *See Chapter 7-2: I²S (Inter-IC Sound bus) Interface in FM4 Family Peripheral Manual Communication Macro Part (002-04862) for the details of CPOL, FSPH, FSLIN, and SMPL.*




Q_CS0,
Q_CS1,
Q_CS2
tSCYCM
mode0
mode2
tOSLSK02
tOSKSL02
Q_SCK
mode1
mode3
tOSLSK13
tOSKSL13
input
Q_IO0,
Q_IO1,
Q_IO2,
Q_IO3
tDSSET
tSDHOLD
output
tOSDAT

15. Major Changes

Spansion Publication Number: S6E2C2_DS709-00013

Page	Section	Change Results
Revision 0.1		
-	-	Initial release
Revision 0.2		
1, 3	Title	Added the following products. S6E2C28HHA/S6E2C29HHA/S6E2C2AHHA/ S6E2C28JHA/S6E2C29JHA/S6E2C2AJHA/ S6E2C28LHA/S6E2C29LHA/S6E2C2ALHA
13	2.Feature	Added “Crypto Assist Function”
15, 16	3.Product Lineup	Added “Crypto Assist Function”
17	4.Packages	Added the following products. S6E2C28HHA/S6E2C29HHA/S6E2C2AHHA/ S6E2C28JHA/S6E2C29JHA/S6E2C2AJHA/ S6E2C28LHA/S6E2C29LHA/S6E2C2ALHA
210	15.ORDERING INFORMATION	Added the following part numbers. S6E2C28HHAGV20000/ S6E2C29HHAGV20000/ S6E2C2AHHAGV20000 S6E2C28JHAGV20000/ S6E2C29JHAGV20000/ S6E2C2AJHAGV20000 S6E2C28JHAGB10000/ S6E2C29JHAGB10000/ S6E2C2AJHAGB10000 S6E2C28LHAGL20000/ S6E2C29LHAGL20000/ S6E2C2ALHAGL20000
Revision 1.0		
11 14 88 89	2. Features 3. Product Lineup 10. Block Diagram 12. Memory Map	Deleted HDM-CEC/Remote Control Receiver.
17-19	5. Pin Assignments	Deleted the pins of HDM-CEC/Remote Control Receiver.(CEC0,CEC1) Revised the pin name of I2S. (MI2S*_0→MI2S*0_0) Deleted the pin of IGTRG0_0.
21-72	6. Pin Descriptions	Deleted the pins of HDM-CEC/Remote Control Receiver.(CEC0,CEC1) Revised the pin name of I2S. (MI2S*_0→MI2S*0_0) Revised the pin number of PF7 in LQFP216.(91→90) Revised the pin number of X1. (73, 58, 50, P5→107, 87, 71, P13) Revised the pin number of X0A. (107, 87, 71, P13→73, 58, 50, P5)
73-80	7. I/O Circuit Type	Revised IOH/IOL of Type S.(IOH=-12mA→-10mA, IOL=12mA→10mA) Added the case of using I2C in Type E, F, G, L, N, S.
95-103	13. Pin Status In Each CPU State	Deleted X and Y in Pin Status Type.
104-105	14.1. Absolute Maximum Ratings	Added 10 mA type.
106-110	14.2. Recommended Operating Conditions	Added AVRL in Analog reference voltage. Revised the mistake in Ethernet-MAC Pins. Revised the leakage current in Maximum leakage current at operating
111-120	14.3.1. Current Rating	Revised the maximum current of each category.
121-123	14.3.2. Pin Characteristics	Added the characteristic of external bus in H level input voltage (hysteresis input). Added the characteristic of 10 mA type.
126	14.4.5. Operating Conditions of USB/Ethernet PLL・I2S PLL (in the case of using main clock for input clock of PLL)	Revised the maximum of I2S PLL macro oscillation clock frequency. (307.2 MHz→384 MHz)