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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	48MHz
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	LED, POR, PWM, WDT
Number of I/O	34
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	1.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at89c5130a-rdtim

The table below shows all SFRs with their address and their reset value.

Table 20. SFR Descriptions

	Bit Addressable	**Non-Bit Addressable**							
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
F8h	UEPINT 0000 0000	CH 0000 0000	CCAP0H XXXX XXXX	CCAP1H XXXX XXXX	CCAP2H XXXX XXXX	CCAP3H XXXX XXXX	CCAP4H XXXX XXXX		FFh
F0h	B 0000 0000	LEDCON 0000 0000							F7h
E8h		CL 0000 0000	CCAP0L XXXX XXXX	CCAP1L XXXX XXXX	CCAP2L XXXX XXXX	CCAP3L XXXX XXXX	CCAP4L XXXX XXXX		EFh
E0h	ACC 0000 0000		UBYCTLX 0000 0000	UBYCTHX 0000 0000					E7h
D8h	CCON 00X0 0000	CMOD 00XX X000	CCAPM0 X000 0000	CCAPM1 X000 0000	CCAPM2 X000 0000	CCAPM3 X000 0000	CCAPM4 X000 0000		DFh
D0h	PSW 0000 0000	FCON (1) XXXX 0000	EECON XXXX XX00		UEPCONX 1000 0000	UEPRST 0000 0000			D7h
C8h	T2CON 0000 0000	T2MOD XXXX XX00	RCAP2L 0000 0000	RCAP2H 0000 0000	TL2 0000 0000	TH2 0000 0000	UEPSTAX 0000 0000	UEPDATX 0000 0000	CFh
C0h	P4 XXXX 1111		UEPIEN 0000 0000	SPCON 0001 0100	SPSTA 0000 0000	SPDAT XXXX XXXX	USBADDR 1000 0000	UEPNUM 0000 0000	C7h
B8h	IPL0 X000 000	SADEN 0000 0000	UFNUML 0000 0000	UFNUMH 0000 0000	USBCON 0000 0000	USBINT 0000 0000	USBIEN 0000 0000		BFh
B0h	P3 1111 1111	IEN1 X0XX X000	IPL1 X0XX X000	IPH1 X0XX X000				IPH0 X000 0000	B7h
A8h	IEN0 0000 0000	SADDR 0000 0000						CKCON1 0000 0000	AFh
A0h	P2 1111 1111		AUXR1 XXXX X0X0	PLLCON XXXX XX00	PLLDIV 0000 0000		WDTRST XXXX XXXX	WDTPRG XXXX X000	A7h
98h	SCON 0000 0000	SBUF XXXX XXXX	BRL 0000 0000	BDRCON XXX0 0000	KBLS 0000 0000	KBE 0000 0000	KBF 0000 0000		9Fh
90h	P1 1111 1111			SSCON 0000 0000	SSCS 1111 1000	SSDAT 1111 1111	SSADR 1111 1110		97h
88h	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000	AUXR XX0X 0000	CKCON0 0000 0000	8Fh
80h	P0 1111 1111	SP 0000 0111	DPL 0000 0000	DPH 0000 0000				PCON 00X1 0000	87h
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	

Note: 1. FCON access is reserved for the Flash API and ISP software.

Reserved

Table 57. CL Register

CL - PCA Counter Register Low (0E9h)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-

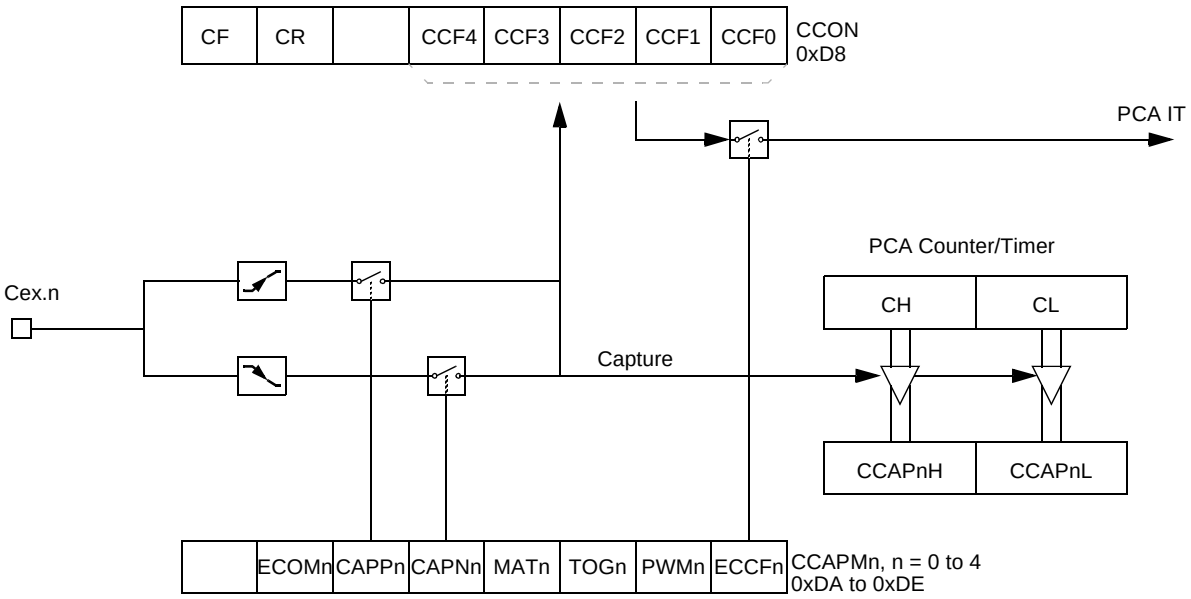
Bit Number	Bit Mnemonic	Description
7 - 0	-	**PCA Counter** CL Value

Reset Value = 0000 0000b
Not bit addressable

PCA Capture Mode

To use one of the PCA modules in the capture mode either one or both of the CCAPM bits CAPN and CAPP for that module must be set. The external CEX input for the module (on port 1) is sampled for a transition. When a valid transition occurs the PCA hardware loads the value of the PCA counter registers (CH and CL) into the module's capture registers (CCAPnL and CCAPnH). If the CCFn bit for the module in the CCON SFR and the ECCFn bit in the CCAPMn SFR are set then an interrupt will be generated (see Figure 27).

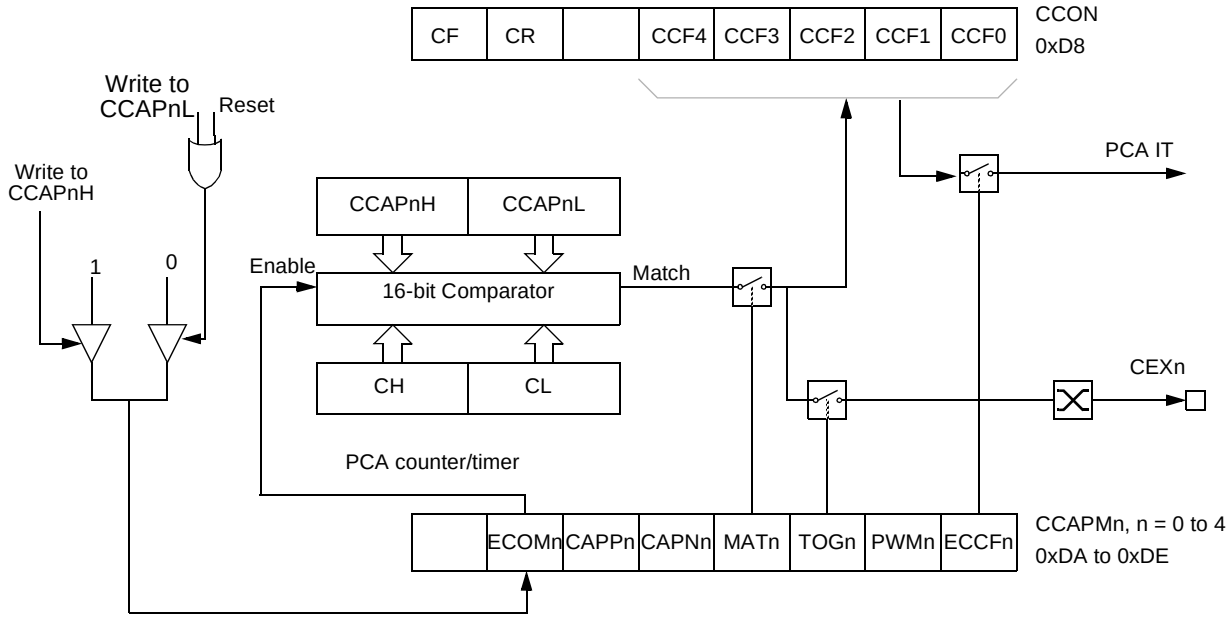
Figure 27. PCA Capture Mode



16-bit Software Timer/Compare Mode

The PCA modules can be used as software timers by setting both the ECOM and MAT bits in the modules CCAPMn register. The PCA timer will be compared to the module's capture registers and when a match occurs an interrupt will occur if the CCFn (CCON SFR) and the ECCFn (CCAPMn SFR) bits for the module are both set (see Figure 28).

Figure 29. PCA High-speed Output Mode



Before enabling ECOM bit, CCAPnL and CCAPnH should be set with a non zero value, otherwise an unwanted match could happen.

Once ECOM set, writing CCAPnL will clear ECOM so that an unwanted match doesn't occur while modifying the compare value. Writing to CCAPnH will set ECOM. For this reason, user software should write CCAPnL first, and then CCAPnH. Of course, the ECOM bit can still be controlled by accessing to CCAPMn register.

Pulse Width Modulator Mode

All of the PCA modules can be used as PWM outputs. Figure 30 shows the PWM function. The frequency of the output depends on the source for the PCA timer. All of the modules will have the same frequency of output because they all share the PCA timer. The duty cycle of each module is independently variable using the module's capture register CCAPLn. When the value of the PCA CL SFR is less than the value in the module's CCAPLn SFR the output will be low, when it is equal to or greater than the output will be high. When CL overflows from FF to 00, CCAPLn is reloaded with the value in CCAPHn. This allows updating the PWM without glitches. The PWM and ECOM bits in the module's CCAPMn register must be set to enable the PWM mode.

Example of computed value when X2 = 1, SMOD1 = 1, SPD = 1

Baud Rates	F_{osc} = 16.384 MHz		F_{osc} = 24 MHz	
	BRL	Error (%)	BRL	Error (%)
115200	247	1.23	243	0.16
57600	238	1.23	230	0.16
38400	229	1.23	217	0.16
28800	220	1.23	204	0.16
19200	203	0.63	178	0.16
9600	149	0.31	100	0.16
4800	43	1.23	-	-

Example of computed value when X2 = 0, SMOD1 = 0, SPD = 0

Baud Rates	F_{osc} = 16.384 MHz		F_{osc} = 24 MHz	
	BRL	Error (%)	BRL	Error (%)
4800	247	1.23	243	0.16
2400	238	1.23	230	0.16
1200	220	1.23	202	3.55
600	185	0.16	152	0.16

The baud rate generator can be used for mode 1 or 3 (refer to Figure 34.), but also for mode 0 for UART, thanks to the bit SRC located in BDRCON register (Table 61.)

UART Registers

SADEN - Slave Address Mask Register for UART (B9h)

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	–

Reset Value = 0000 0000b

SADDR - Slave Address Register for UART (A9h)

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	–

Reset Value = 0000 0000b

SBUF - Serial Buffer Register for UART (99h)

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	–

Reset Value = XXXX XXXXb

Table 63. IEN0 Register

IEN0 - Interrupt Enable Register (A8h)

7	6	5	4	3	2	1	0
EA	EC	ET2	ES	ET1	EX1	ET0	EX0

Bit Number	Bit Mnemonic	Description
7	EA	**Enable All interrupt bit** Cleared to disable all interrupts. Set to enable all interrupts.
6	EC	**PCA interrupt enable bit** Cleared to disable. Set to enable.
5	ET2	**Timer 2 overflow interrupt Enable bit** Cleared to disable Timer 2 overflow interrupt. Set to enable Timer 2 overflow interrupt.
4	ES	**Serial port Enable bit** Cleared to disable serial port interrupt. Set to enable serial port interrupt.
3	ET1	**Timer 1 overflow interrupt Enable bit** Cleared to disable Timer 1 overflow interrupt. Set to enable Timer 1 overflow interrupt.
2	EX1	**External interrupt 1 Enable bit** Cleared to disable external interrupt 1. Set to enable external interrupt 1.
1	ET0	**Timer 0 overflow interrupt Enable bit** Cleared to disable timer 0 overflow interrupt. Set to enable timer 0 overflow interrupt.
0	EX0	**External interrupt 0 Enable bit** Cleared to disable external interrupt 0. Set to enable external interrupt 0.

Reset Value = 0000 0000b
Bit addressable

Table 67. IPL1 Register

IPL1 - Interrupt Priority Register (B2h)

7	6	5	4	3	2	1	0
-	PUSBL	-	-	-	PSPIL	PTWIL	PKBDL

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	PUSBL	**USB Interrupt Priority bit** Refer to PUSBH for priority level.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	PSPIL	**SPI Interrupt Priority bit** Refer to PSPIH for priority level.
1	PTWIL	**TWI Interrupt Priority bit** Refer to PTWIH for priority level.
0	PKBL	**Keyboard Interrupt Priority bit** Refer to PKBH for priority level.

Reset Value = X0XX X000b
Not bit addressable

Table 71. KBE Register

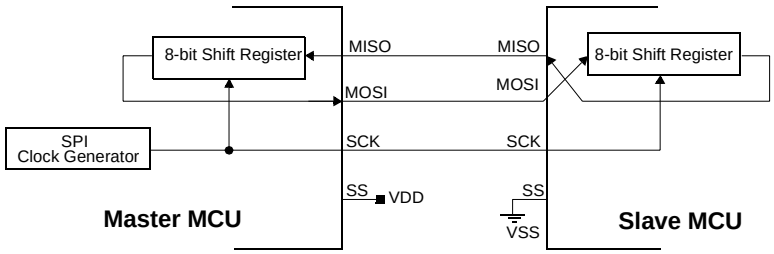
KBE **-** Keyboard Input Enable Register (9Dh)

7	6	5	4	3	2	1	0
KBE7	KBE6	KBE5	KBE4	KBE3	KBE2	KBE1	KBE0

Bit Number	Bit Mnemonic	Description
7	KBE7	**Keyboard line 7 Enable bit** Cleared to enable standard I/O pin. Set to enable KBF.7 bit in KBF register to generate an interrupt request.
6	KBE6	**Keyboard line 6 Enable bit** Cleared to enable standard I/O pin. Set to enable KBF.6 bit in KBF register to generate an interrupt request.
5	KBE5	**Keyboard line 5 Enable bit** Cleared to enable standard I/O pin. Set to enable KBF.5 bit in KBF register to generate an interrupt request.
4	KBE4	**Keyboard line 4 Enable bit** Cleared to enable standard I/O pin. Set to enable KBF.4 bit in KBF register to generate an interrupt request.
3	KBE3	**Keyboard line 3 Enable bit** Cleared to enable standard I/O pin. Set to enable KBF.3 bit in KBF register to generate an interrupt request.
2	KBE2	**Keyboard line 2 Enable bit** Cleared to enable standard I/O pin. Set to enable KBF.2 bit in KBF register to generate an interrupt request.
1	KBE1	**Keyboard line 1 Enable bit** Cleared to enable standard I/O pin. Set to enable KBF.1 bit in KBF register to generate an interrupt request.
0	KBE0	**Keyboard line 0 Enable bit** Cleared to enable standard I/O pin. Set to enable KBF.0 bit in KBF register to generate an interrupt request.

Reset Value = 0000 0000b

Figure 41. Full-duplex Master/Slave Interconnection



Master Mode

The SPI operates in Master mode when the Master bit, MSTR (1), in the SPCON register is set. Only one Master SPI device can initiate transmissions. Software begins the transmission from a Master SPI module by writing to the Serial Peripheral Data Register (SPDAT). If the shift register is empty, the byte is immediately transferred to the shift register. The byte begins shifting out on MOSI pin under the control of the serial clock, SCK. Simultaneously, another byte shifts in from the Slave on the Master's MISO pin. The transmission ends when the Serial Peripheral transfer data flag, SPIF, in SPSTA becomes set. At the same time that SPIF becomes set, the received byte from the Slave is transferred to the receive data register in SPDAT. Software clears SPIF by reading the Serial Peripheral Status register (SPSTA) with the SPIF bit set, and then reading the SPDAT.

Slave Mode

The SPI operates in Slave mode when the Master bit, MSTR (2), in the SPCON register is cleared. Before a data transmission occurs, the Slave Select pin, $\overline{SS}$, of the Slave device must be set to'0'. $\overline{SS}$ must remain low until the transmission is complete.

In a Slave SPI module, data enters the shift register under the control of the SCK from the Master SPI module. After a byte enters the shift register, it is immediately transferred to the receive data register in SPDAT, and the SPIF bit is set. To prevent an overflow condition, Slave software must then read the SPDAT before another byte enters the shift register (3). A Slave SPI must complete the write to the SPDAT (shift register) at least one bus cycle before the Master SPI starts a transmission. If the write to the data register is late, the SPI transmits the data already in the shift register from the previous transmission.

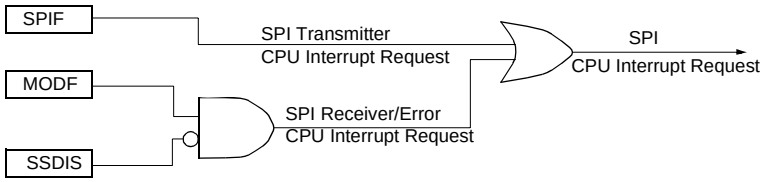
Transmission Formats

Software can select any of four combinations of serial clock (SCK) phase and polarity using two bits in the SPCON: the Clock POLarity (CPOL (4)) and the Clock PHAse (CPHA4). CPOL defines the default SCK line level in idle state. It has no significant effect on the transmission format. CPHA defines the edges on which the input data are sampled and the edges on which the output data are shifted (Figure 42 and Figure 43). The clock phase and polarity should be identical for the Master SPI device and the communicating Slave device.

Notes:

1. The SPI module should be configured as a Master before it is enabled (SPEN set). Also the Master SPI should be configured before the Slave SPI.
2. The SPI module should be configured as a Slave before it is enabled (SPEN set).
3. The maximum frequency of the SCK for an SPI configured as a Slave is $F_{CLK\ PERIPH}/2$.
4. Before writing to the CPOL and CPHA bits, the SPI should be disabled (SPEN ='0').

Figure 45. SPI Interrupt Requests Generation



Registers

There are three registers in the module that provide control, status and data storage functions. These registers are describes in the following paragraphs.

Serial Peripheral Control Register (SPCON)

- The Serial Peripheral Control Register does the following:
  - Selects one of the Master clock rates
  - Configure the SPI module as Master or Slave
  - Selects serial clock polarity and phase
  - Enables the SPI module
  - Frees the SS pin for a general-purpose

Table 76 describes this register and explains the use of each bit.

Table 76. SPCON Register

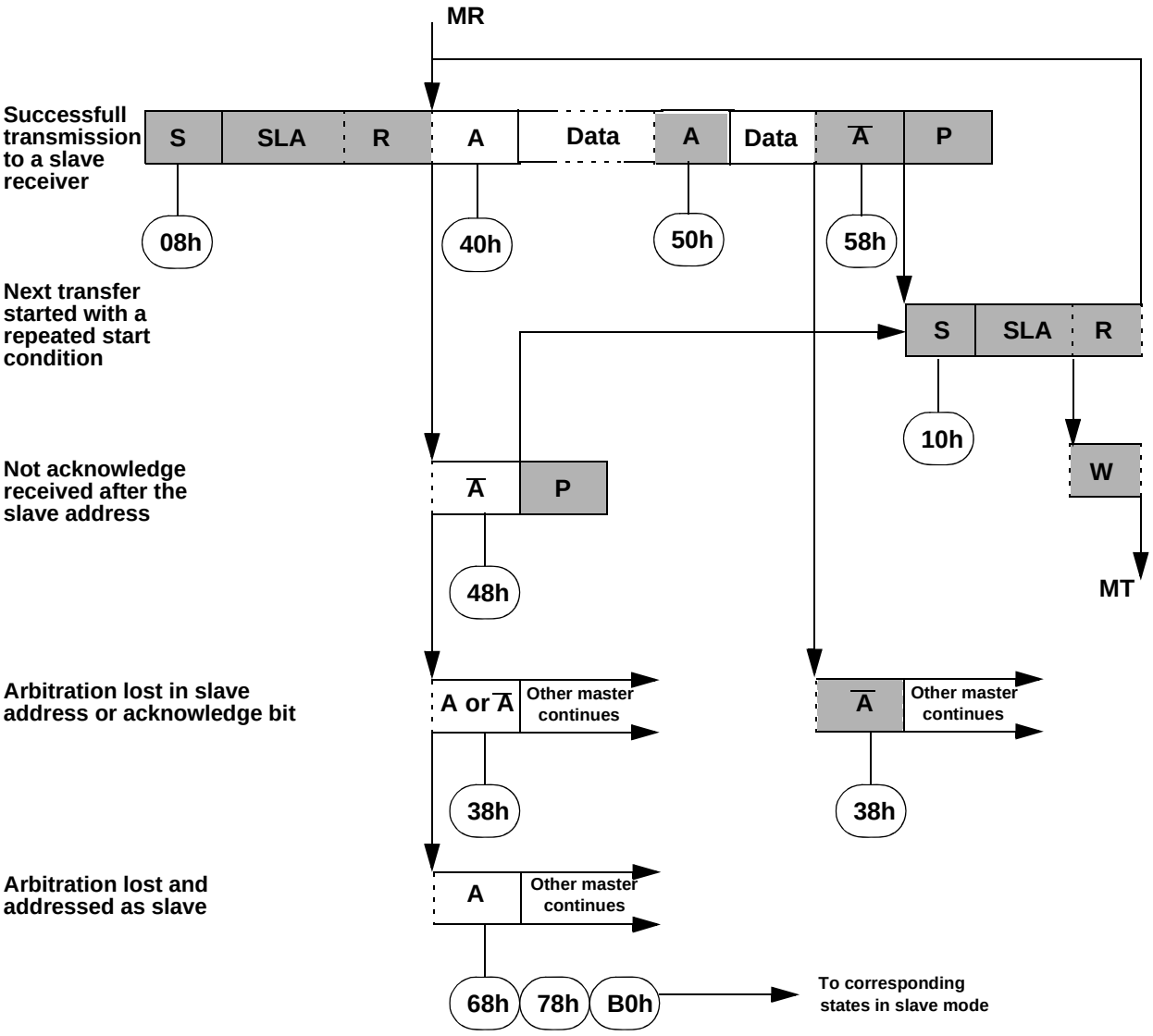
7	6	5	4	3	2	1	0
SPR2	**SPEN**	**SSDIS**	**MSTR**	**CPOL**	**CPHA**	**SPR1**	**SPR0**

Bit Number	Bit Mnemonic	Description
7	SPR2	**Serial Peripheral Rate 2** Bit with SPR1 and SPR0 define the clock rate.
6	SPEN	**Serial Peripheral Enable** Cleared to disable the SPI interface. Set to enable the SPI interface.
5	SSDIS	**$\overline{SS}$ Disable** Cleared to enable $\overline{SS}$ in both Master and Slave modes. Set to disable $\overline{SS}$ in both Master and Slave modes. In Slave mode, this bit has no effect if CPHA = “0”.
4	MSTR	**Serial Peripheral Master** Cleared to configure the SPI as a Slave. Set to configure the SPI as a Master.
3	CPOL	**Clock Polarity** Cleared to have the SCK set to “0” in idle state. Set to have the SCK set to “1” in idle state.
2	CPHA	**Clock Phase** Cleared to have the data sampled when the SCK leaves the idle state (see CPOL). Set to have the data sampled when the SCK returns to idle state (see CPOL).

Table 83. Status in Master Transmitter Mode

Status Code SSSTA	Status of the Two-wire Bus and Two-wire Hardware	Application software response					Next Action Taken by Two-wire Hardware
		To/From SSDAT	To SSCON				
			SSSTA	SSSTO	SSI	SSAA	
08h	A START condition has been transmitted	Write SLA+W	X	0	0	X	SLA+W will be transmitted.
10h	A repeated START condition has been transmitted	Write SLA+W	X	0	0	X	SLA+W will be transmitted.
		Write SLA+R	X	0	0	X	SLA+R will be transmitted. Logic will switch to master receiver mode
18h	SLA+W has been transmitted; ACK has been received	Write data byte	0	0	0	X	Data byte will be transmitted.
		No SSDAT action	1	0	0	X	Repeated START will be transmitted.
		No SSDAT action	0	1	0	X	STOP condition will be transmitted and SSSTO flag will be reset.
		No SSDAT action	1	1	0	X	STOP condition followed by a START condition will be transmitted and SSSTO flag will be reset.
20h	SLA+W has been transmitted; NOT ACK has been received	Write data byte	0	0	0	X	Data byte will be transmitted.
		No SSDAT action	1	0	0	X	Repeated START will be transmitted.
		No SSDAT action	0	1	0	X	STOP condition will be transmitted and SSSTO flag will be reset.
		No SSDAT action	1	1	0	X	STOP condition followed by a START condition will be transmitted and SSSTO flag will be reset.
28h	Data byte has been transmitted; ACK has been received	Write data byte	0	0	0	X	Data byte will be transmitted.
		No SSDAT action	1	0	0	X	Repeated START will be transmitted.
		No SSDAT action	0	1	0	X	STOP condition will be transmitted and SSSTO flag will be reset.
		No SSDAT action	1	1	0	X	STOP condition followed by a START condition will be transmitted and SSSTO flag will be reset.
30h	Data byte has been transmitted; NOT ACK has been received	Write data byte	0	0	0	X	Data byte will be transmitted.
		No SSDAT action	1	0	0	X	Repeated START will be transmitted.
		No SSDAT action	0	1	0	X	STOP condition will be transmitted and SSSTO flag will be reset.
		No SSDAT action	1	1	0	X	STOP condition followed by a START condition will be transmitted and SSSTO flag will be reset.
38h	Arbitration lost in SLA+W or data bytes	No SSDAT action	0	0	0	X	Two-wire bus will be released and not addressed slave mode will be entered.
		No SSDAT action	1	0	0	X	A START condition will be transmitted when the bus becomes free.

Figure 50. Format and State in the Master Receiver Mode



From master to slave

From slave to master

Data A — Any number of data bytes and their associated acknowledge bits

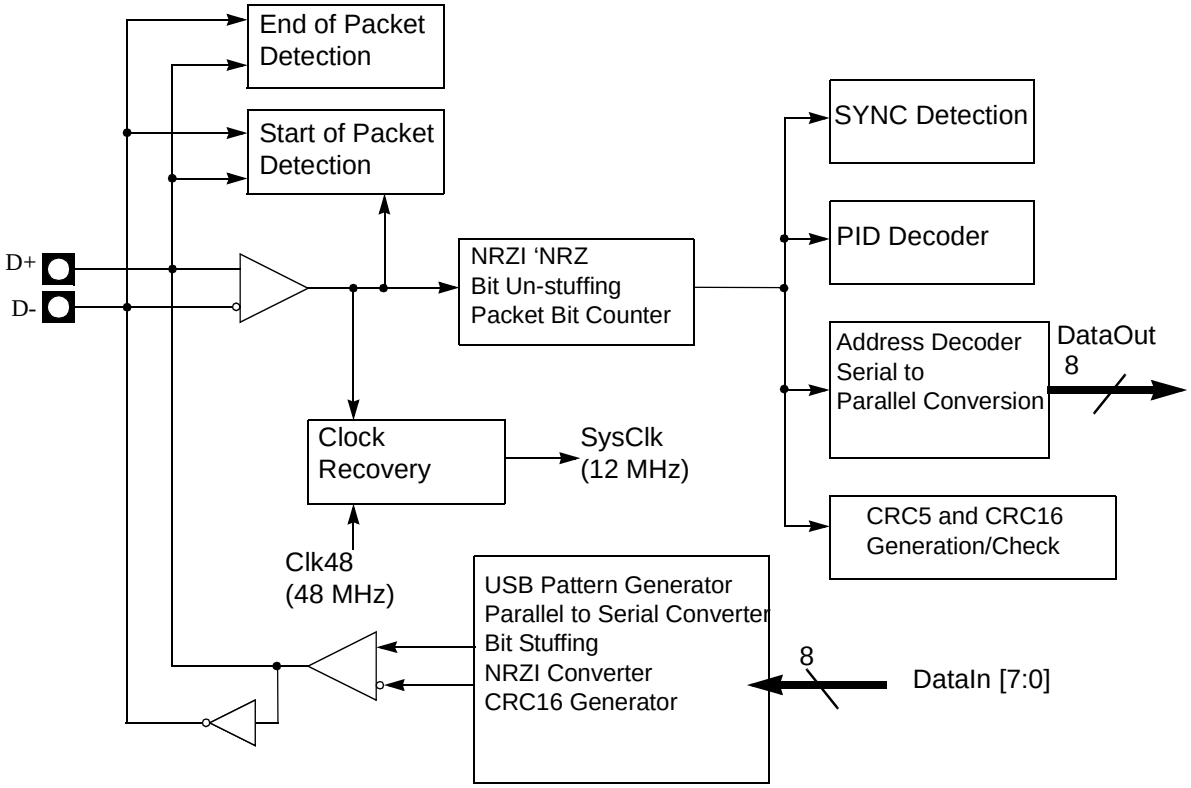
n — This number (contained in SSCS) corresponds to a defined state of the 2-wire bus

Serial Interface Engine (SIE)

The SIE performs the following functions:

- NRZI data encoding and decoding.
- Bit stuffing and un-stuffing.
- CRC generation and checking.
- Handshakes.
- TOKEN type identifying.
- Address checking.
- Clock generation (via DPLL).

Figure 54. SIE Block Diagram



Function Interface Unit (FIU) The Function Interface Unit provides the interface between the AT89C5131 and the SIE. It manages transactions at the packet level with minimal intervention from the device firmware, which reads and writes the endpoint FIFOs.

Figure 55. UFI Block Diagram

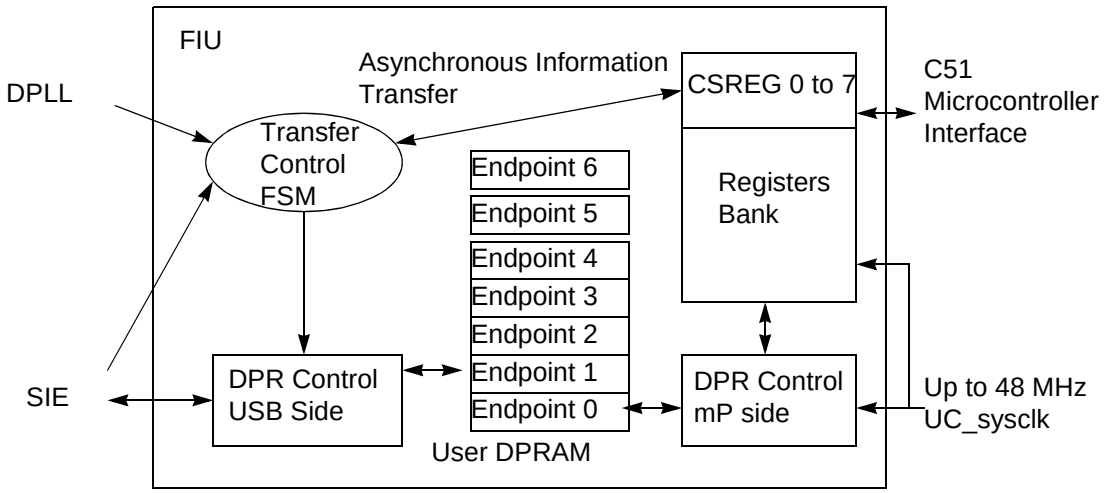
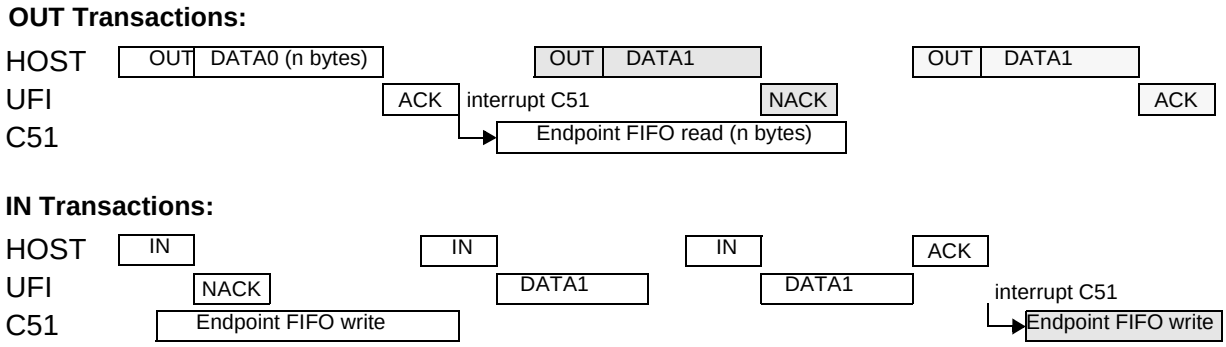


Figure 56. Minimum Intervention from the USB Device Firmware



Control Transactions

Setup Stage

The DIR bit in the UEPSTAX register will be at 0.

Receiving Setup packets is the same as receiving Bulk Out packets, except that the RXSETUP bit in the UEPSTAX register is set by the USB controller instead of the RXOUTB0 bit to indicate that an Out packet with a Setup PID has been received on the Control endpoint. When the RXSETUP bit has been set, all the other bits of the UEPSTAX register are cleared and an interrupt is triggered if enabled.

The firmware has to read the Setup request stored in the Control endpoint FIFO before clearing the RXSETUP bit to free the endpoint FIFO for the next transaction.

Data Stage: Control Endpoint Direction

The data stage management is similar to Bulk management.

A Control endpoint is managed by the USB controller as a full-duplex endpoint: IN and OUT. All other endpoint types are managed as half-duplex endpoint: IN or OUT. The firmware has to specify the control endpoint direction for the data stage using the DIR bit in the UEPSTAX register.
The firmware has to use the DIR bit before data IN in order to meet the data-toggle requirements:

- If the data stage consists of INs,
  the firmware has to set the DIR bit in the UEPSTAX register before writing into the FIFO and sending the data by setting to 1 the TXRDY bit in the UEPSTAX register. The IN transaction is complete when the TXCMPL has been set by the hardware. The firmware will clear the TXCMPL bit before any other transaction.
- If the data stage consists of OUTs,
  the firmware has to leave the DIR bit at 0. The RXOUTB0 bit is set by hardware when a new valid packet has been received on the endpoint. The firmware must read the data stored into the FIFO and then clear the RXOUTB0 bit to reset the FIFO and to allow the next transaction.

To send a STALL handshake, see “STALL Handshake” on page 130.

Status Stage

The DIR bit in the UEPSTAX register will be reset at 0 for IN and OUT status stage.

The status stage management is similar to Bulk management.

- For a Control Write transaction or a No-Data Control transaction, the status stage consists of a IN Zero Length Packet (see “Bulk/Interrupt IN Transactions in Standard Mode” on page 125). To send a STALL handshake, see “STALL Handshake” on page 130.
- For a Control Read transaction, the status stage consists of a OUT Zero Length Packet (see “Bulk/Interrupt OUT Transactions in Standard Mode” on page 123).

Table 93. Priority Levels

IPHUSB	IPLUSB	USB Priority Level
0	0	0 Lowest
0	1	1
1	0	2
1	1	3 Highest

USB Interrupt Control System

As shown in Figure 68, many events can produce a USB interrupt:

- TXCMPL: Transmitted In Data (see Table 100 on page 142). This bit is set by hardware when the Host accept a In packet.
- RXOUTB0: Received Out Data Bank 0 (see Table 100 on page 142). This bit is set by hardware when an Out packet is accepted by the endpoint and stored in bank 0.
- RXOUTB1: Received Out Data Bank 1 (only for Ping-pong endpoints) (see Table 100 on page 142). This bit is set by hardware when an Out packet is accepted by the endpoint and stored in bank 1.
- RXSETUP: Received Setup (see Table 100 on page 142). This bit is set by hardware when an SETUP packet is accepted by the endpoint.
- STLCRC: STALLED (only for Control, Bulk and Interrupt endpoints) (see Table 100 on page 142). This bit is set by hardware when a STALL handshake has been sent as requested by STALLRQ, and is reset by hardware when a SETUP packet is received.
- SOFINT: Start of Frame Interrupt (See “USBIEN Register USBIEN (S:BEh) USB Global Interrupt Enable Register” on page 139.). This bit is set by hardware when a USB Start of Frame packet has been received.
- WUPCPU: Wake-Up CPU Interrupt (See “USBIEN Register USBIEN (S:BEh) USB Global Interrupt Enable Register” on page 139.). This bit is set by hardware when a USB resume is detected on the USB bus, after a SUSPEND state.
- SPINT: Suspend Interrupt (See “USBIEN Register USBIEN (S:BEh) USB Global Interrupt Enable Register” on page 139.). This bit is set by hardware when a USB suspend is detected on the USB bus.

Figure 68. USB Interrupt Control Block Diagram

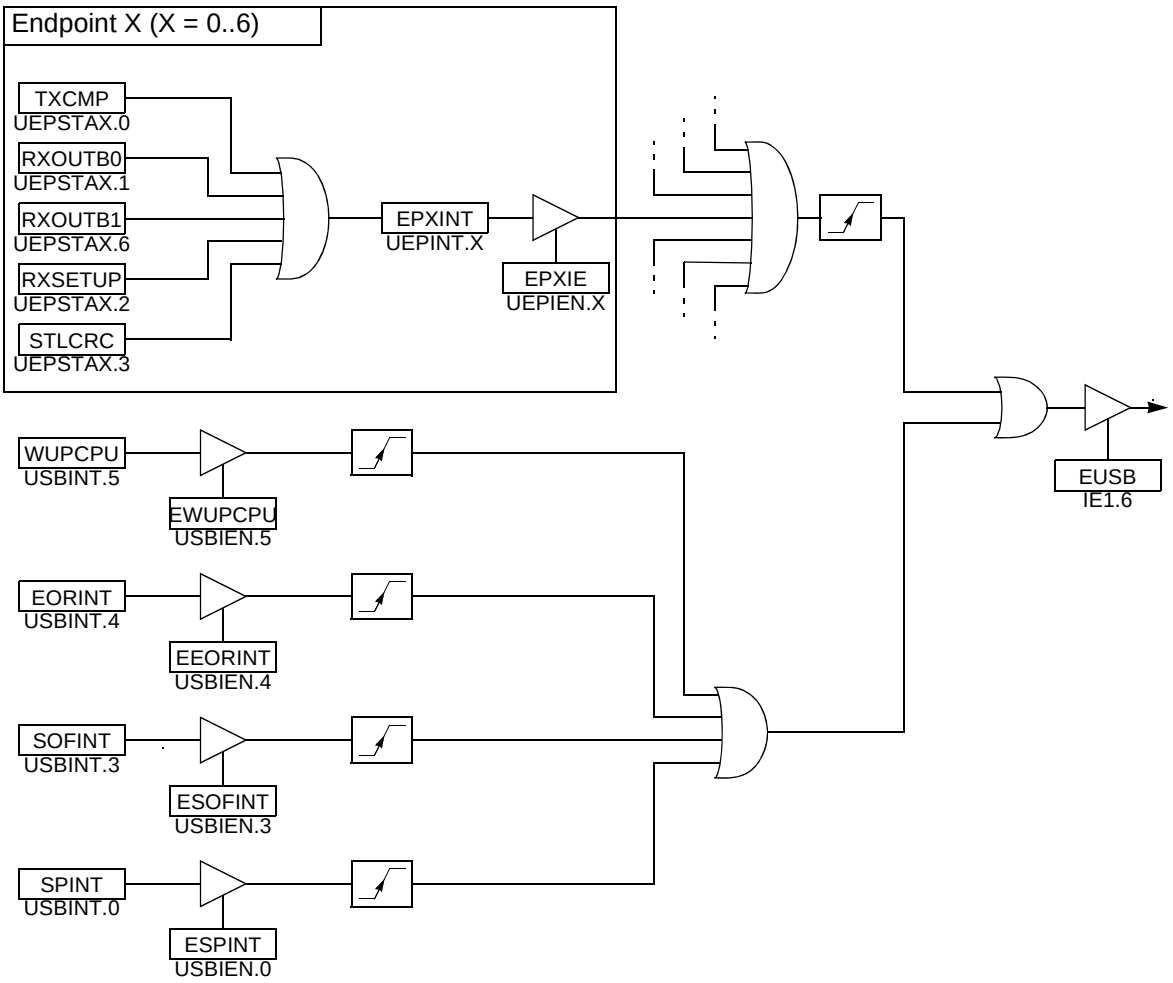


Table 106. UEPIEN Register
UEPIEN (S:C2h)
USB Endpoint Interrupt Enable Register

7	6	5	4	3	2	1	0
-	EP6INTE	EP5INTE	EP4INTE	EP3INTE	EP2INTE	EP1INTE	EP0INTE

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is always 0. Do not set this bit.
6	EP6INTE	**Endpoint 6 Interrupt Enable** Set this bit to enable the interrupts for this endpoint. Clear this bit to disable the interrupts for this endpoint.
5	EP5INTE	**Endpoint 5 Interrupt Enable** Set this bit to enable the interrupts for this endpoint. Clear this bit to disable the interrupts for this endpoint.
4	EP4INTE	**Endpoint 4 Interrupt Enable** Set this bit to enable the interrupts for this endpoint. Clear this bit to disable the interrupts for this endpoint.
3	EP3INTE	**Endpoint 3 Interrupt Enable** Set this bit to enable the interrupts for this endpoint. Clear this bit to disable the interrupts for this endpoint.
2	EP2INTE	**Endpoint 2 Interrupt Enable** Set this bit to enable the interrupts for this endpoint. Clear this bit to disable the interrupts for this endpoint.
1	EP1INTE	**Endpoint 1 Interrupt Enable** Set this bit to enable the interrupts for this endpoint. Clear this bit to disable the interrupts for this endpoint.
0	EP0INTE	**Endpoint 0 Interrupt Enable** Set this bit to enable the interrupts for this endpoint. Clear this bit to disable the interrupts for this endpoint.

Reset Value = 00h

For timing purposes as port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm 20$ mA.

Ordering Information

Table 131. Possible Order Entries

Part Number	Memory Size (Kbytes)	Supply Voltage	Temperature Range	Package	Packing
AT89C5130A-RDTIM	16	2.7 to 5.5V	Industrial	VQFP64	Tray
AT89C5130A-PUTIM	16	2.7 to 5.5V	Industrial	QFN32	Tray
AT89C5130A-S3SIM	16	2.7 to 5.5V	Industrial	PLCC52	Stick
AT89C5131A-RDTIM	32	2.7 to 5.5V	Industrial	VQFP64	Tray
AT89C5131A-PUTIM	32	2.7 to 5.5V	Industrial	QFN32	Tray
AT89C5131A-S3SIM	32	2.7 to 5.5V	Industrial	PLCC52	Stick
AT89C5130A-RDTUM	16	2.7 to 5.5V	Industrial & Green	VQFP64	Tray & Dry Pack
AT89C5130A-PUTUM	16	2.7 to 5.5V	Industrial & Green	QFN32	Tray & Dry Pack
AT89C5130A-S3SUM	16	2.7 to 5.5V	Industrial & Green	PLCC52	Tray & Dry Pack
AT89C5131A-RDTUM	32	2.7 to 5.5V	Industrial & Green	VQFP64	Tray & Dry Pack
AT89C5131A-PUTUM	32	2.7 to 5.5V	Industrial & Green	QFN32	Tray & Dry Pack
AT89C5131A-S3SUM	32	2.7 to 5.5V	Industrial & Green	PLCC52	Tray & Dry Pack

Notes: 1. Optional Packing and Package options (please consult Atmel sales representative)
-Tape and Reel
-Dry Pack
-Die form