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Details

Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	40MHz
Connectivity	CANbus, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	36
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LFBGA, CSPBGA
Supplier Device Package	64-CSPBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at89c51cc03u-7ctim

Table 1. SFR Mapping

	0/8 ⁽²⁾	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
F8h	IPL1 xxxx x000	CH 0000 0000	CCAP0H 0000 0000	CCAP1H 0000 0000	CCAP2H 0000 0000	CCAP3H 0000 0000	CCAP4H 0000 0000		FFh
F0h	B 0000 0000		ADCLK xxx0 0000	ADCON x000 0000	ADDL 0000 0000	ADDH 0000 0000	ADCF 0000 0000	IPH1 xxxx x000	F7h
E8h	IEN1 xxxx x000	CL 0000 0000	CCAP0L 0000 0000	CCAP1L 0000 0000	CCAP2L 0000 0000	CCAP3L 0000 0000	CCAP4L 0000 0000		EFh
E0h	ACC 0000 0000								E7h
D8h	CCON 0000 0000	CMOD 00xx x000	CCAPM0 x000 0000	CCAPM1 x000 0000	CCAPM2 x000 0000	CCAPM3 x000 0000	CCAPM4 x000 0000		DFh
D0h	PSW 0000 0000	FCON 0000 0000	EECON xxxx xx00	FSTA xxxx xx00	SPCON 0001 0100	SPSCR 0000 0000	SPDAT xxxx xxxx		D7h
C8h	T2CON 0000 0000	T2MOD xxxx xx00	RCAP2L 0000 0000	RCAP2H 0000 0000	TL2 0000 0000	TH2 0000 0000	CANEN1 x000 0000	CANEN2 0000 0000	CFh
C0h	P4 xxx1 1111	CANGIE xx00 000x	CANIE1 x000 0000	CANIE2 0000 0000	CANIDM1 xxxx xxxx	CANIDM2 xxxx xxxx	CANIDM3 xxxx xxxx	CANIDM4 xxxx xxxx	C7h
B8h	IPL0 x000 0000	SADEN 0000 0000	CANSIT1 0000 0000	CANSIT2 0000 0000	CANIDT1 xxxx xxxx	CANIDT2 xxxx xxxx	CANIDT3 xxxx xxxx	CANIDT4 xxxx xxxx	BFh
B0h	P3 1111 1111	CANPAGE 0000 0000	CANSTCH xxxx xxxx	CANCONCH xxxx xxxx	CANBT1 xxxx xxxx	CANBT2 xxxx xxxx	CANBT3 xxxx xxxx	IPH0 x000 0000	B7h
A8h	IEN0 0000 0000	SADDR 0000 0000	CANGSTA x0x0 0000	CANGCON 0000 0x00	CANTIML 0000 0000	CANTIMH 0000 0000	CANSTMPL 0000 0000	CANSTMPH 0000 0000	AFh
A0h	P2 1111 1111	CANTCON 0000 0000	AUXR1 xxxx 00x0	CANMSG xxxx xxxx	CANTTCL 0000 0000	CANTTCH 0000 0000	WDTRST 1111 1111	WDTPRG xxxx x000	A7h
98h	SCON 0000 0000	SBUF 0000 0000		CANGIT 0x00 0000	CANTEC 0000 0000	CANREC 0000 0000		CKCON1 xxxx xx00	9Fh
90h	P1 1111 1111								97h
88h	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000	AUXR x001 0100	CKCON0 0000 0000	8Fh
80h	P0 1111 1111	SP 0000 0111	DPL 0000 0000	DPH 0000 0000				PCON 00x1 0000	87h
	0/8 ⁽²⁾	1/9	2/A	3/B	4/C	5/D	6/E	7/F	

Reserved 

Note: 1. Do not read or write Reserved Registers

2. These registers are bit-addressable.

Sixteen addresses in the SFR space are both byte-addressable and bit-addressable. The bit-addressable SFR's are those whose address ends in 0 and 8. The bit addresses, in this area, are 0x80 through to 0xFF.

Power Monitor

The POR/PFD function monitors the internal power-supply of the CPU core memories and the peripherals, and if needed, suspends their activity when the internal power supply falls below a safety threshold. This is achieved by applying an internal reset to them.

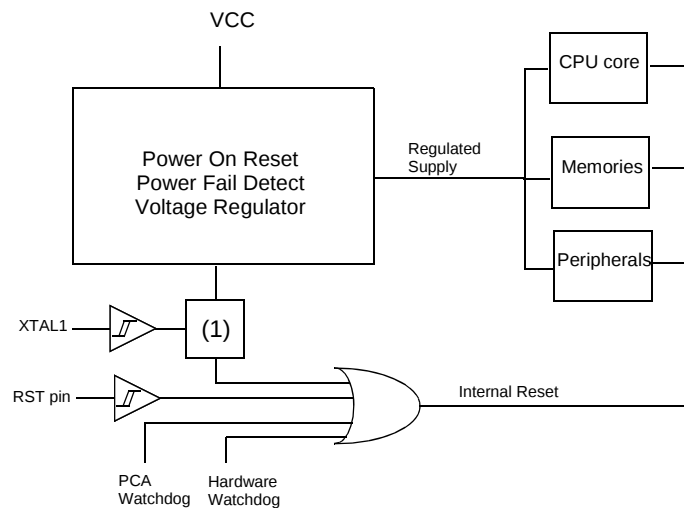
By generating the Reset the Power Monitor insures a correct start up when AT89C51CC03 is powered up.

Description

In order to startup and maintain the microcontroller in correct operating mode, V_{CC} has to be stabilized in the V_{CC} operating range and the oscillator has to be stabilized with a nominal amplitude compatible with logic level VIH/VIL.

These parameters are controlled during the three phases: power-up, normal operation and power going down. See Figure 14.

Figure 14. Power Monitor Block Diagram



Note: 1. Once XTAL1 high and low levels reach above and below VIH/VIL a 1024 clock period delay will extend the reset coming from the Power Fail Detect. If the power falls below the Power Fail Detect threshold level, the reset will be applied immediately.

The Voltage regulator generates a regulated internal supply for the CPU core the memories and the peripherals. Spikes on the external Vcc are smoothed by the voltage regulator.

The Power fail detect monitor the supply generated by the voltage regulator and generate a reset if this supply falls below a safety threshold as illustrated in the Figure 15.

Sharing Instructions

Table 19. Instructions shared

Action	RAM	XRAM ERAM	EEPROM DATA	Boot FLASH	FM0	Hardware Byte	XROW
Read	MOV	MOVX	MOVX	MOVC	MOVC	MOVC	MOVC
Write	MOV	MOVX	MOVX	-	by cl	by cl	by cl

Note: by cl : using Column Latch

Table 20. Read MOVX A, @DPTR

EEE bit in EECON Register	FPS in FCON Register	ENBOOT	EA	XRAM ERAM	EEPROM DATA	Flash Column Latch
0	0	X	X	OK		
0	1	X	X	OK		
1	0	X	X		OK	
1	1	X	X	OK		

Table 21. Write MOVX @DPTR,A

EEE bit in EECON Register	FPS bit in FCON Register	ENBOOT	EA	XRAM ERAM	EEPROM Data	Flash Column Latch
0	0	X	X	OK		
0	1	X	1			OK
			0	OK		
1	0	X	X		OK	
1	1	X	1			OK
			0	OK		

Watchdog Programming

The three lower bits (S0, S1, S2) located into WDTPRG register permit to program the WDT duration.

Table 42. Machine Cycle Count

S2	S1	S0	Machine Cycle Count
0	0	0	2^{14}
0	0	1	2^{15}
0	1	0	2^{16}
0	1	1	2^{17}
1	0	0	2^{18}
1	0	1	2^{19}
1	1	0	2^{20}
1	1	1	2^{21}

To compute WD Time-Out, the following formula is applied:

$$FTime - Out = \frac{F_{osc}}{6 \times 2^{WDX2 \wedge X2} (2^{14} \times 2^{Svalue})}$$

Note: Svalue represents the decimal value of (S2 S1 S0)

The following table outlines the time-out value for $F_{osc_XTAL} = 12$ MHz in X1 mode

Table 43. Time-Out Computation

S2	S1	S0	Fosc = 12 MHz	Fosc = 16 MHz	Fosc = 20 MHz
0	0	0	16.38 ms	12.28 ms	9.82 ms
0	0	1	32.77 ms	24.57 ms	19.66 ms
0	1	0	65.54 ms	49.14 ms	39.32 ms
0	1	1	131.07 ms	98.28 ms	78.64 ms
1	0	0	262.14 ms	196.56 ms	157.28 ms
1	0	1	524.29 ms	393.12 ms	314.56 ms
1	1	0	1.05 s	786.24 ms	629.12 ms
1	1	1	2.10 s	1.57 s	1.25 s

Working on Message Objects

The Page message object register (CANPAGE) is used to select one of the 15 message objects. Then, message object Control (CANCONCH) and message object Status (CANSTCH) are available for this selected message object number in the corresponding SFRs. A single register (CANMSG) is used for the message. The mailbox pointer is managed by the Page message object register with an auto-incrementation at the end of each access. The range of this counter is 8.

Note that the mailbox is a pure RAM, dedicated to one message object, without overlap. In most cases, it is not necessary to transfer the received message into the standard memory. The message to be transmitted can be built directly in the mailbox. Most calculations or tests can be executed in the mailbox area which provide quicker access.

CAN Controller Management

In order to enable the CAN Controller correctly the following registers have to be initialized:

- General Control (CANGCON),
- Bit Timing (CANBT 1, 2 and 3),
- And for each page of 15 message objects
 - message object Control (CANCONCH),
 - message object Status (CANSTCH).

During operation, the CAN Enable message object registers 1 and 2 (CANEN 1 and 2) gives a fast overview of the message objects availability.

The CAN messages can be handled by interrupt or polling modes.

A message object can be configured as follows:

- Transmit message object,
- Receive message object,
- Receive buffer message object.
- Disable

This configuration is made in the CONCH1:2 field of the CANCONCH register (see Table 46).

When a message object is configured, the corresponding ENCH bit of CANEN 1 and 2 register is set.

Table 46. Configuration for CONCH1:2

CONCH 1	CONCH 2	Type of Message Object
0	0	Disable
0	1	Transmitter
1	0	Receiver
1	1	Receiver buffer

When a Transmitter or Receiver action of a message object is completed, the corresponding ENCH bit of the CANEN 1 and 2 register is cleared. In order to re-enable the message object, it is necessary to re-write the configuration in CANCONCH register.

Non-consecutive message objects can be used for all three types of message objects (Transmitter, Receiver and Receiver buffer),

Bit Timing and Baud Rate

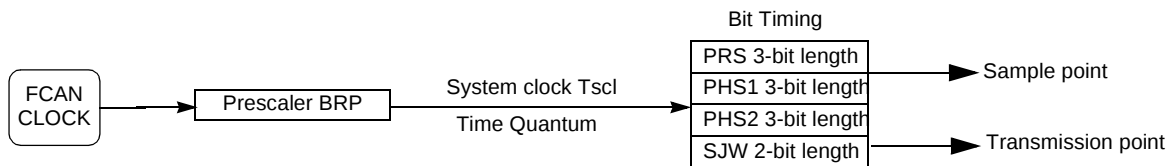
FSM's (Finite State Machine) of the CAN channel need to be synchronous to the time quantum. So, the input clock for bit timing is the clock used into CAN channel FSM's.

Field and segment abbreviations:

- BRP: Baud Rate Prescaler.
- TQ: Time Quantum (output of Baud Rate Prescaler).
- SYNS: SYNchronization Segment is 1 TQ long.
- PRS: PRopagation time Segment is programmable to be 1, 2, ..., 8 TQ long.
- PHS1: PHase Segment 1 is programmable to be 1, 2, ..., 8 TQ long.
- PHS2: PHase Segment 2 is programmable to be superior or equal to the INFORMATION PROCESSING TIME and inferior or equal to TPSH1.
- INFORMATION PROCESSING TIME is 2 TQ.
- SJW: (Re) Synchronization Jump Width is programmable to be minimum of PHS1 and 4.

The total number of TQ in a bit time has to be programmed at least from 8 to 25.

Figure 51. Sample And Transmission Point



The baud rate selection is made by Tbit calculation:

$$T_{bit} = T_{syns} + T_{prs} + T_{phs1} + T_{phs2}$$

1. $T_{syns} = T_{scl} = (BRP[5..0] + 1) / F_{can} = 1TQ$.
2. $T_{prs} = (1 \text{ to } 8) * T_{scl} = (PRS[2..0] + 1) * T_{scl}$
3. $T_{phs1} = (1 \text{ to } 8) * T_{scl} = (PHS1[2..0] + 1) * T_{scl}$
4. $T_{phs2} = (1 \text{ to } 8) * T_{scl} = (PHS2[2..0] + 1) * T_{scl}$
 $T_{phs2} = \text{Max of } (T_{phs1} \text{ and } 2TQ)$
5. $T_{sjw} = (1 \text{ to } 4) * T_{scl} = (SJW[1..0] + 1) * T_{scl}$

The total number of Tscl (Time Quanta) in a bit time must be comprised between **8 to 25**.

4. Interrupt routine

```
// Save the current CANPAGE

// Find the first message object which generate an interrupt in CANSIT1 and CANSIT2

// Select the corresponding message object

// Analyse the CANSTCH register to identify which kind of interrupt is generated

// Manage the interrupt

// Clear the status register CANSTCH = 00h;

// if it is not a channel interrupt but a general interrupt
// Manage the general interrupt and clear CANGIT register

// restore the old CANPAGE
```

CAN SFR's

Table 47. CAN SFR's With Reset Values

	0/8 ⁽¹⁾	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
F8h	IPL1 xxxx x000	CH 0000 0000	CCAP0H 0000 0000	CCAP1H 0000 0000	CCAP2H 0000 0000	CCAP3H 0000 0000	CCAP4H 0000 0000		FFh
F0h	B 0000 0000		ADCLK xx00 x000	ADCON 0000 0000	ADDL xxxx xx00	ADDH 0000 0000	ADCF 0000 0000	IPH1 xxxx x000	F7h
E8h	IEN1 xxxx x000	CL 0000 0000	CCAP0L 0000 0000	CCAP1L 0000 0000	CCAP2L 0000 0000	CCAP3L 0000 0000	CCAP4L 0000 0000		EFh
E0h	ACC 0000 0000								E7h
D8h	CCON 00xx xx00	CMOD 00xx x000	CCAPM0 x000 0000	CCAPM1 x000 0000	CCAPM2 x000 0000	CCAPM3 x000 0000	CCAPM4 x000 0000		DFh
D0h	PSW 0000 0000	FCON 0000 0000	EECON xxxx xx00	FSTA xxxx xx00	SPCON 0001 0100	SPSCR 0000 0000	SPDAT xxxx xxxx		D7h
C8h	T2CON 0000 0000	T2MOD xxxx xx00	RCAP2L 0000 0000	RCAP2H 0000 0000	TL2 0000 0000	TH2 0000 0000	CANEN1 xx00 0000	CANEN2 0000 0000	CFh
C0h	P4 xxxx xx11	CANGIE 0000 0000	CANIE1 xx00 0000	CANIE2 0000 0000	CANIDM1 xxxx xxxx	CANIDM2 xxxx xxxx	CANIDM3 xxxx xxxx	CANIDM4 xxxx xxxx	C7h
B8h	IPL0 x000 0000	SADEN 0000 0000	CANSIT1 0x00 0000	CANSIT2 0000 0000	CANIDT1 xxxx xxxx	CANIDT2 xxxx xxxx	CANIDT3 xxxx xxxx	CANIDT4 xxxx xxxx	BFh
B0h	P3 1111 1111	CANPAGE 0000 0000	CANSTCH xxxx xxxx	CANCONCH xxxx xxxx	CANBT1 xxxx xxxx	CANBT2 xxxx xxxx	CANBT3 xxxx xxxx	IPH0 x000 0000	B7h
A8h	IEN0 0000 0000	SADDR 0000 0000	CANGSTA 0000 0000	CANGCON 0000 x000	CANTIML 0000 0000	CANTIMH 0000 0000	CANSTMPL 0000 0000	CANSTMPH 0000 0000	AFh
A0h	P2 1111 1111	CANTCON 0000 0000	AUXR1 xxxx 00x0	CANMSG xxxx xxxx	CANTTCL 0000 0000	CANTTCH 0000 0000	WDRST 1111 1111	WDTPRG xxxx x000	A7h
98h	SCON 0000 0000	SBUF 0000 0000		CANGIT 0x00 0000	CANTEC 0000 0000	CANREC 0000 0000		CKCON1 xxxx xxx0	9Fh
90h	P1 1111 1111								97h
88h	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000	AUXR X001 0100	CKCON 0000 0000	8Fh
80h	P0 1111 1111	SP 0000 0111	DPL 0000 0000	DPH 0000 0000				PCON 0000 0000	87h
	0/8 ⁽¹⁾	1/9	2/A	3/B	4/C	5/D	6/E	7/F	

Table 54. CANEN1 Register

CANEN1 (S:CEh Read Only)
CAN Enable Message Object Registers 1

7	6	5	4	3	2	1	0
-	ENCH14	ENCH13	ENCH12	ENCH11	ENCH10	ENCH9	ENCH8
Bit Number	Bit Mnemonic	Description					
7	-	Reserved The values read from this bit is indeterminate. Do not set this bit.					
6-0	ENCH14:8	Enable Message Object These bits provide the availability of the MOB. It is set to one when the MOB is enabled. Once TXOK or RXOK is set to one (TXOK for automatic reply), the corresponding ENMOB is reset. ENMOB is also set to zero configuring the MOB in disabled mode, applying abortion or standby mode. 0 - message object disabled: MOB available for a new transmission or reception. 1 - message object enabled: MOB in use. This bit is resetable by re-writing the CANCONCH of the corresponding message object.					

Reset Value = x000 0000b

Table 55. CANEN2 Register

CANEN2 (S:CFh Read Only)
CAN Enable Message Object Registers 2

7	6	5	4	3	2	1	0
ENCH7	ENCH6	ENCH5	ENCH4	ENCH3	ENCH2	ENCH1	ENCH0
Bit Number	Bit Mnemonic	Description					
7-0	ENCH7:0	Enable Message Object These bits provide the availability of the MOB. It is set to one when the MOB is enabled. Once TXOK or RXOK is set to one (TXOK for automatic reply), the corresponding ENMOB is reset. ENMOB is also set to zero configuring the MOB in disabled mode, applying abortion or standby mode. 0 - message object disabled: MOB available for a new transmission or reception. 1 - message object enabled: MOB in use. This bit is resetable by re-writing the CANCONCH of the corresponding message object.					

Reset Value = 0000 0000b

Table 63. CANPAGE Register

CANPAGE (S:B1h)
CAN Message Object Page Register

7	6	5	4	3	2	1	0
CHNB 3	CHNB 2	CHNB 1	CHNB 0	AINC	INDX2	INDX1	INDX0
Bit Number	Bit Mnemonic	Description					
7-4	CHNB3:0	Selection of Message Object Number The available numbers are: 0 to 14 (see Figure 48).					
3	AINC	Auto Increment of the Index (active low) 0 - auto-increment of the index (default value). 1 - non-auto-increment of the index.					
2-0	INDX2:0	Index Byte location of the data field for the defined message object (see Figure 48).					

Reset Value = 0000 0000b

Table 64. CANCONCH Register

CANCONCH (S:B3h)
CAN Message Object Control and DLC Register

7	6	5	4	3	2	1	0
CONCH 1	CONCH 0	RPLV	IDE	DLC 3	DLC 2	DLC 1	DLC 0
Bit Number	Bit Mnemonic	Description					
7-6	CONCH1:0	Configuration of Message Object CONCH1 CONCH0 0 0: disable 0 1: Launch transmission 1 0: Enable Reception 1 1: Enable Reception Buffer Note: The user must re-write the configuration to enable the corresponding bit in the CANEN1:2 registers.					
5	RPLV	Reply Valid Used in the automatic reply mode after receiving a remote frame 0 - reply not ready. 1 - reply ready and valid.					
4	IDE	Identifier Extension 0 - CAN standard rev 2.0 A (ident = 11 bits). 1 - CAN standard rev 2.0 B (ident = 29 bits).					
3-0	DLC3:0	Data Length Code Number of Bytes in the data field of the message. The range of DLC is from 0 up to 8. This value is updated when a frame is received (data or remote frame). If the expected DLC differs from the incoming DLC, a warning appears in the CANSTCH register.					

No default value after reset

Figure 60. Data Transmission Format (CPHA = 0)

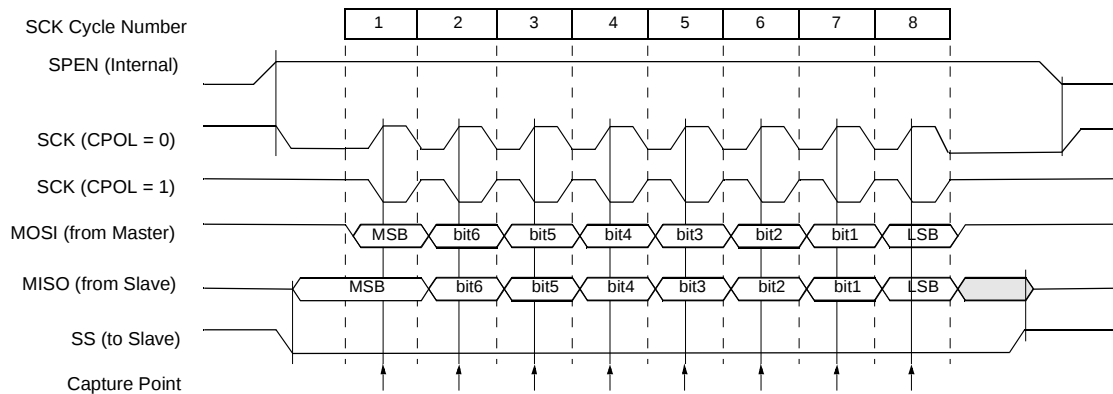


Figure 61. Data Transmission Format (CPHA = 1)

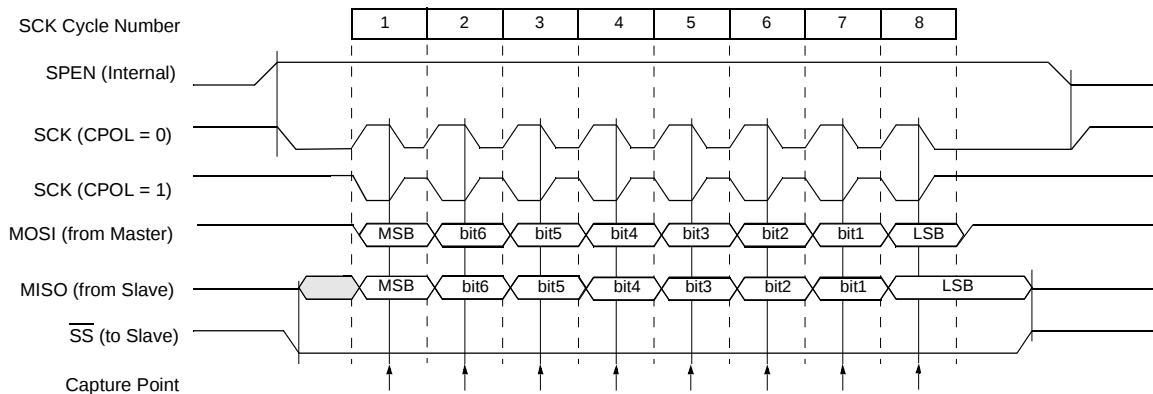
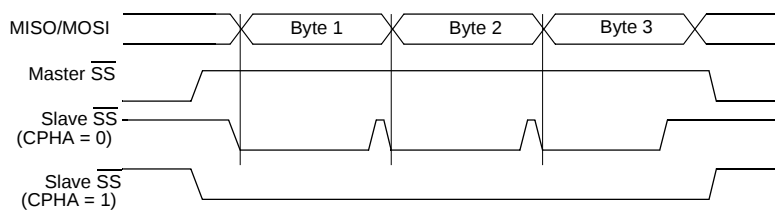


Figure 62. CPHA/SS Timing



As shown in Figure 60, the first SCK edge is the MSB capture strobe. Therefore, the Slave must begin driving its data before the first SCK edge, and a falling edge on the SS pin is used to start the transmission. The SS pin must be toggled high and then low between each Byte transmitted (Figure 62).

Figure 61 shows an SPI transmission in which CPHA is '1'. In this case, the Master begins driving its MOSI pin on the first SCK edge. Therefore, the Slave uses the first SCK edge as a start transmission signal. The SS pin can remain low between transmissions (Figure 62). This format may be preferred in systems having only one Master and only one Slave driving the MISO data line.

Queuing transmission

For an SPI configured in master or slave mode, a queued data byte must be transmitted/received immediately after the previous transmission has completed.

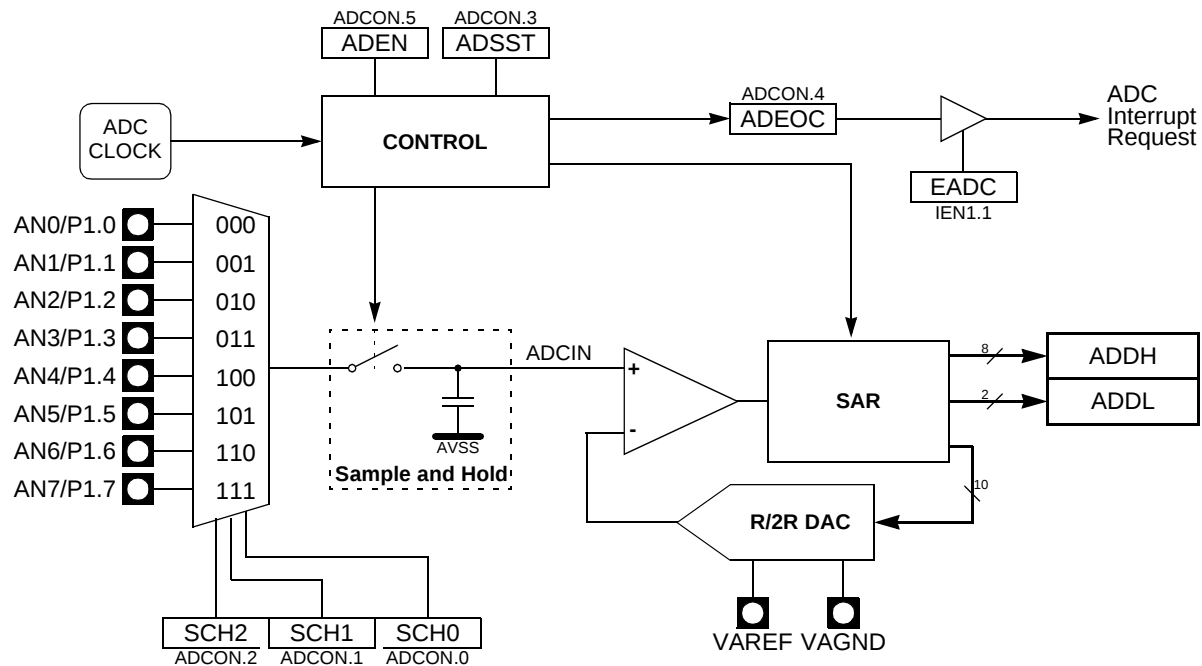
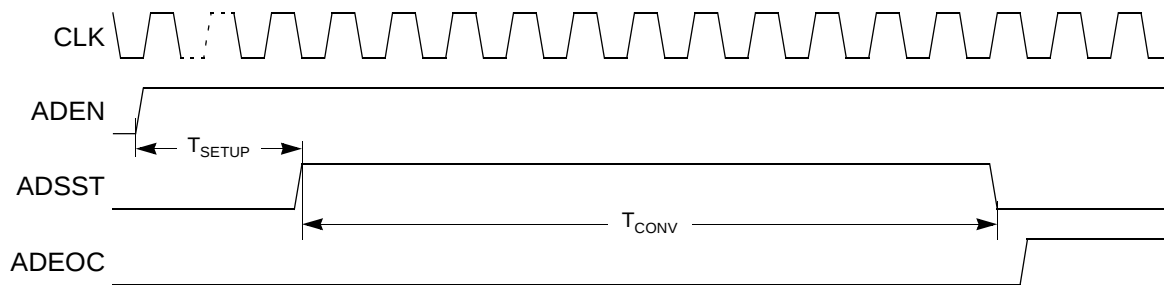


Figure 74 shows the timing diagram of a complete conversion. For simplicity, the figure depicts the waveforms in idealized form and do not provide precise timing information. For ADC characteristics and timing parameters refer to the Section “AC Characteristics” of the AT89C51CC03 datasheet.



Note: Tsetup min = 4 us
Tconv=11 clock ADC = 1sample and hold + 10 bit conversion
The user must ensure that 4 us minimum time between setting ADEN and the start of the first conversion.

```
EADC = 1
// clear the field SCH[2:0]
ADCON and = F8h
// Select the channel
ADCON | = channel
// Start conversion in precision mode
ADCON | = 48h
```

Note: to enable the ADC interrupt:
EA = 1

Table 105. ADCLK Register

ADCLK (S:F2h)
ADC Clock Prescaler

7	6	5	4	3	2	1	0
-	-	-	PRS 4	PRS 3	PRS 2	PRS 1	PRS 0

Bit Number	Bit Mnemonic	Description
7-5	-	Reserved The value read from these bits are indeterminate. Do not set these bits.
4-0	PRS4:0	Clock Prescaler See Note ⁽¹⁾

Reset Value = XXX0 0000b

Note: 1. In X1 mode:
For PRS > 0 $F_{ADC} = \frac{F_{XTAL}}{4 \times PRS}$
For PRS = 0 $F_{ADC} = \frac{F_{XTAL}}{128}$
In X2 mode:
For PRS > 0 $F_{ADC} = \frac{F_{XTAL}}{2 \times PRS}$
For PRS = 0 $F_{ADC} = \frac{F_{XTAL}}{64}$

Table 106. ADDH Register

ADDH (S:F5h Read Only)
ADC Data High Byte Register

7	6	5	4	3	2	1	0
ADAT 9	ADAT 8	ADAT 7	ADAT 6	ADAT 5	ADAT 4	ADAT 3	ADAT 2

Bit Number	Bit Mnemonic	Description
7-0	ADAT9:2	ADC result bits 9-2

Reset Value = 00h

Table 107. ADDL Register

ADDL (S:F4h Read Only)
ADC Data Low Byte Register

7	6	5	4	3	2	1	0
-	-	-	-	-	-	ADAT 1	ADAT 0

Table 111. IEN1 Register

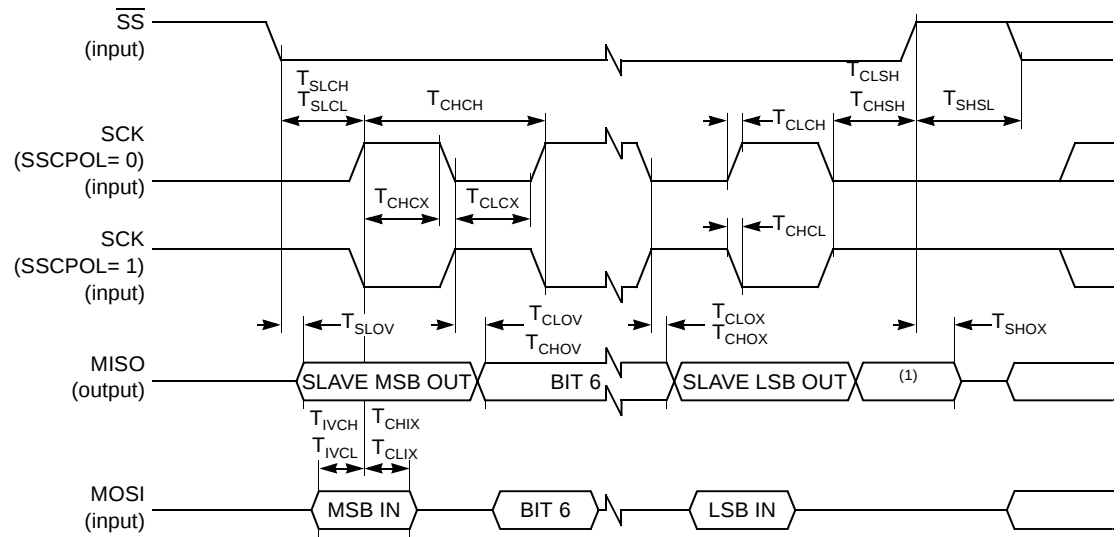
IEN1 (S:E8h)
Interrupt Enable Register

7	6	5	4	3	2	1	0
-	-	-	-	ESPI	ETIM	EADC	ECAN

Bit Number	Bit Mnemonic	Description
7	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
6	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
5	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
4	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
3	ESPI	SPI Interrupt Enable bit Clear to disable the SPI interrupt. Set to enable the SPI interrupt.
2	ETIM	Timer Overrun Interrupt Enable bit Clear to disable the timer overrun interrupt. Set to enable the timer overrun interrupt.
1	EADC	ADC Interrupt Enable bit Clear to disable the ADC interrupt. Set to enable the ADC interrupt.
0	ECAN	CAN Interrupt Enable bit Clear to disable the CAN interrupt. Set to enable the CAN interrupt.

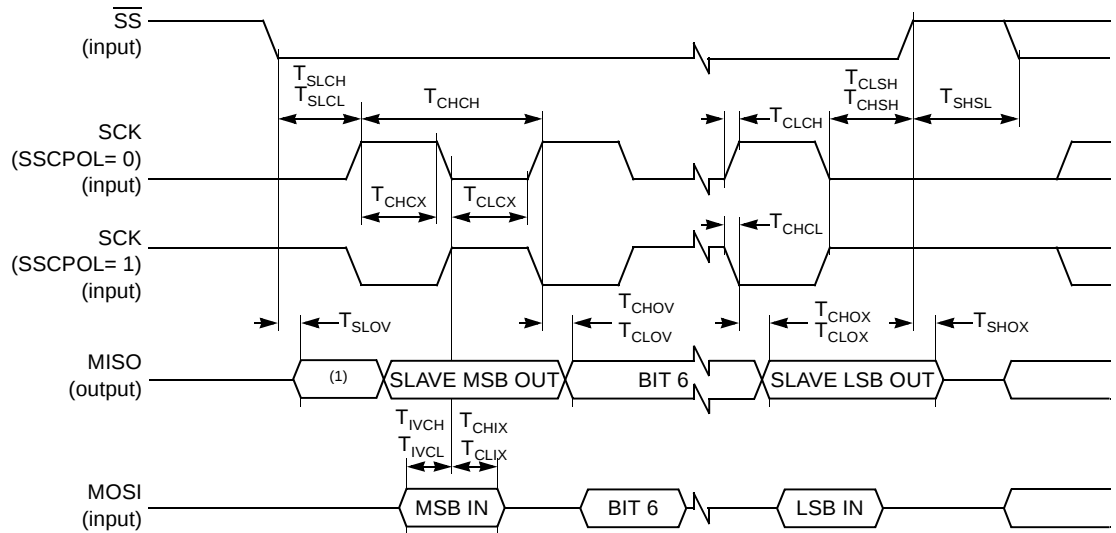
Reset Value = xxxx 0000b
bit addressable

Figure 84. SPI Slave Waveforms (SSCPHA= 0)



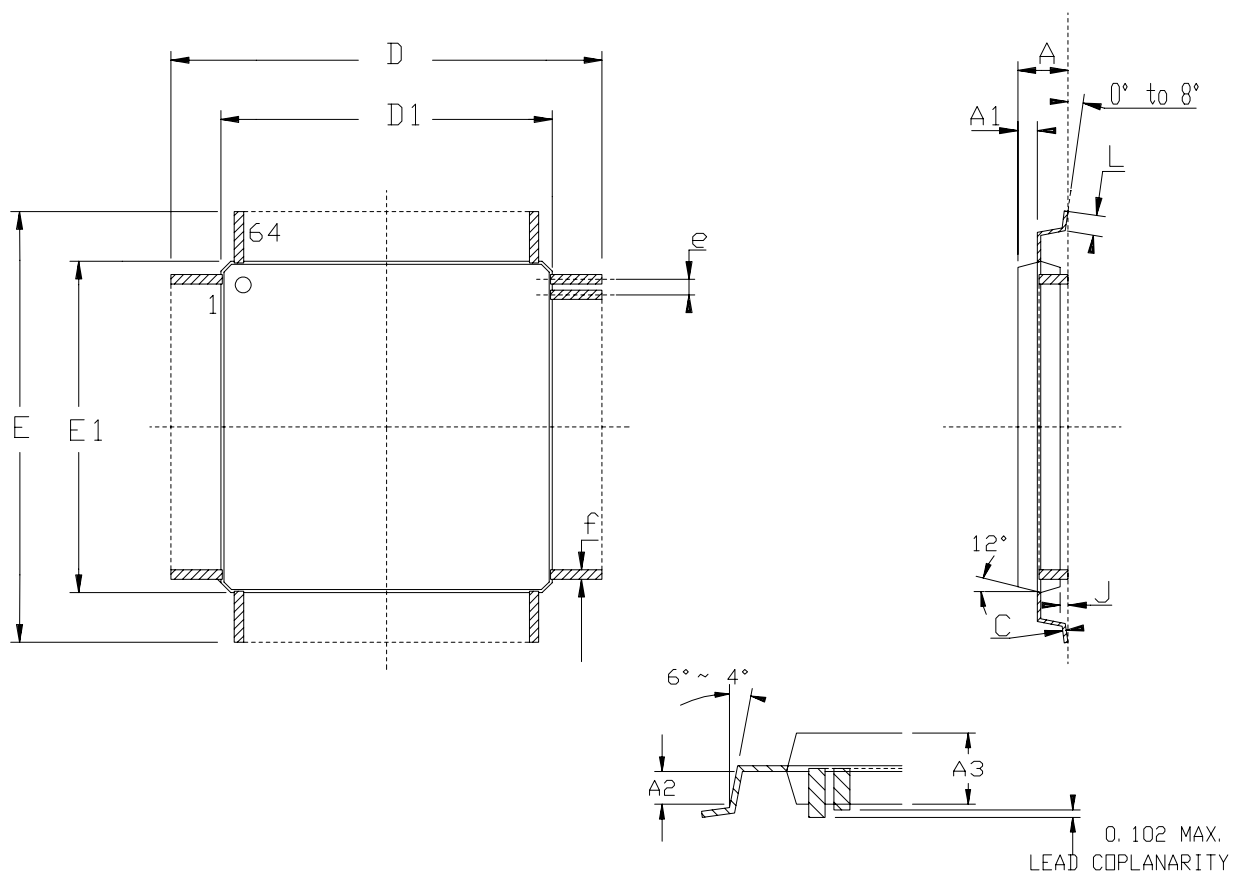
Note: 1. Not Defined but generally the MSB of the character which has just been received.

Figure 85. SPI Slave Waveforms (SSCPHA= 1)



Note: 1. Not Defined but generally the LSB of the character which has just been received.

VQFP64



	MM		INCH	
	Min	Max	Min	Max
A	-	1.60	-	.063
A1	0.64 REF		.025 REF	
A2	0.64 REF		.025 REF	
A3	1.35	1.45	.053	.057
D	11.75	12.25	.463	.483
D1	9.90	10.10	.390	.398
E	11.75	12.25	.463	.483
E1	9.90	10.10	.390	.398
J	0.05	-	.002	-
L	0.45	0.75	.018	.030
e	0.50 BSC		.0197 BSC	
f	0.25 BSC		.010 BSC	

STANDARD NOTES FOR PQFP/ VQFP / TQFP / DQFP

1/ CONTROLLING DIMENSIONS : INCHES

2/ ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y 14.5M - 1982.

**3/ "D1 AND E1" DIMENSIONS DO NOT INCLUDE MOLD PROTUSIONS.
MOLD PROTUSIONS SHALL NOT EXCEED 0.25 mm (0.010 INCH).
THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM
PACKAGE BODY SIZE BY AS MUCH AS 0.15 mm.**

**4/ DATUM PLANE "H" LOCATED AT MOLD PARTING LINE AND
COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT
BOTTOM OF PARTING LINE.**

5/ DATUM "A" AND "D" TO BE DETERMINED AT DATUM PLANE H.

**6/ DIMENSION " f " DOES NOT INCLUDE DAMBAR PROTUSION ALLOWABLE
DAMBAR PROTUSION SHALL BE 0.08mm/.003" TOTAL IN EXCESS OF THE
" f " DIMENSION AT MAXIMUM MATERIAL CONDITION .
DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.**

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