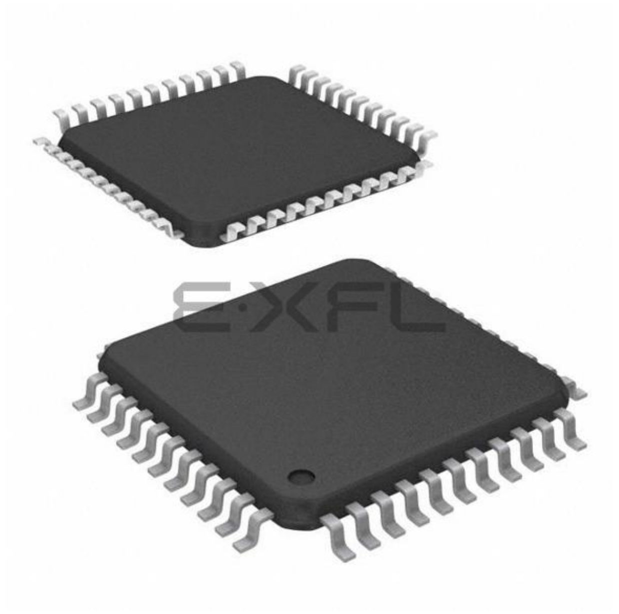

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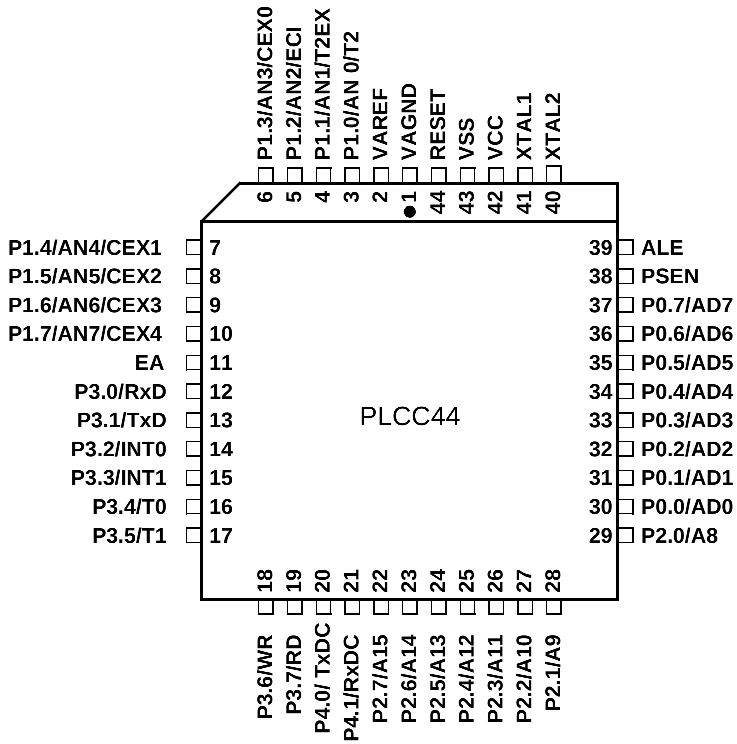
### Applications of "Embedded - Microcontrollers"

| **Details** | |
|---|---|
| Product Status | Obsolete |
| Core Processor | 80C51 |
| Core Size | 8-Bit |
| Speed | 40MHz |
| Connectivity | CANbus, SPI, UART/USART |
| Peripherals | POR, PWM, WDT |
| Number of I/O | 36 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 2K x 8 |
| RAM Size | 2.25K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 5.5V |
| Data Converters | A/D 8x10b |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-LQFP |
| Supplier Device Package | 44-VQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/at89c51cc03u-rdtim |

## Pin Configuration



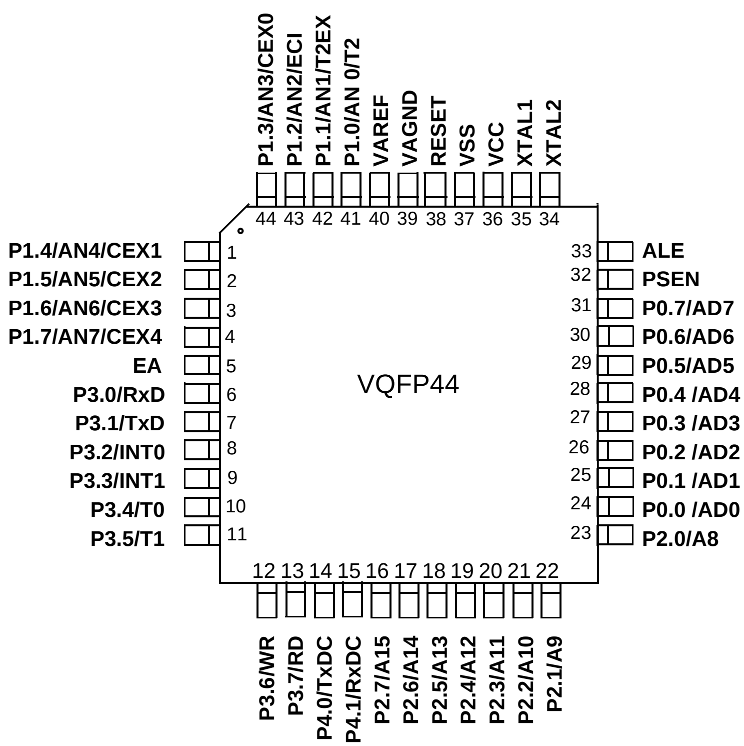



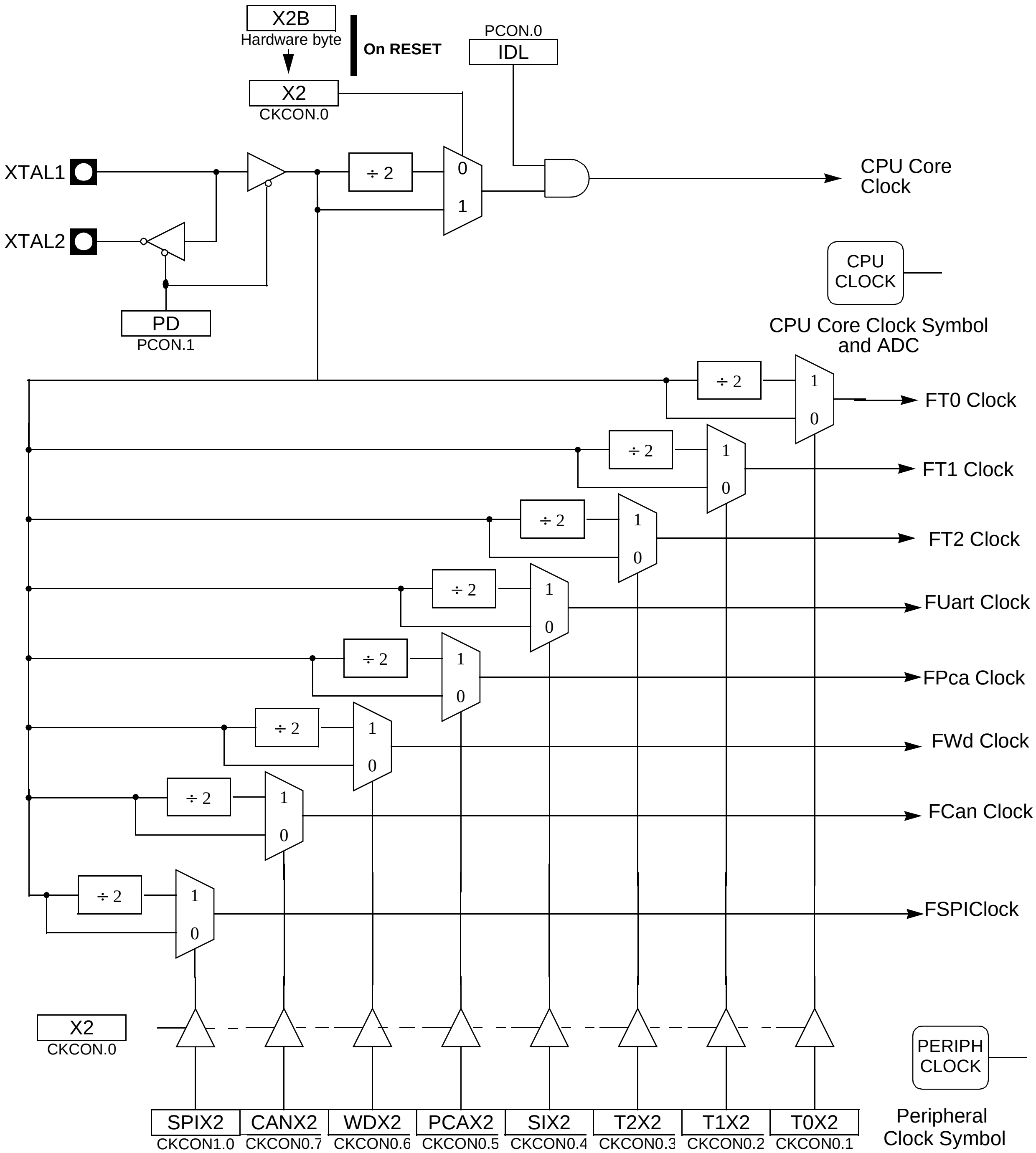
**Table 1.** SFR Mapping

| | 0/8[2] | 1/9 | 2/A | 3/B | 4/C | 5/D | 6/E | 7/F | |
|---|---|---|---|---|---|---|---|---|---|
| F8h | IPL1 xxxx x000 | CH 0000 0000 | CCAP0H 0000 0000 | CCAP1H 0000 0000 | CCAP2H 0000 0000 | CCAP3H 0000 0000 | CCAP4H 0000 0000 | | FFh |
| F0h | B 0000 0000 | | ADCLK xxx0 0000 | ADCON x000 0000 | ADDL 0000 0000 | ADDH 0000 0000 | ADCF 0000 0000 | IPH1 xxxx x000 | F7h |
| E8h | IEN1 xxxx x000 | CL 0000 0000 | CCAP0L 0000 0000 | CCAP1L 0000 0000 | CCAP2L 0000 0000 | CCAP3L 0000 0000 | CCAP4L 0000 0000 | | EFh |
| E0h | ACC 0000 0000 | | | | | | | | E7h |
| D8h | CCON 0000 0000 | CMOD 00xx x000 | CCAPM0 x000 0000 | CCAPM1 x000 0000 | CCAPM2 x000 0000 | CCAPM3 x000 0000 | CCAPM4 x000 0000 | | DFh |
| D0h | PSW 0000 0000 | FCON 0000 0000 | EECON xxxx xx00 | FSTA xxxx xx00 | SPCON 0001 0100 | SPSCR 0000 0000 | SPDAT xxxx xxxx | | D7h |
| C8h | T2CON 0000 0000 | T2MOD xxxx xx00 | RCAP2L 0000 0000 | RCAP2H 0000 0000 | TL2 0000 0000 | TH2 0000 0000 | CANEN1 x000 0000 | CANEN2 0000 0000 | CFh |
| C0h | P4 xxx1 1111 | CANGIE xx00 000x | CANIE1 x000 0000 | CANIE2 0000 0000 | CANIDM1 xxxx xxxx | CANIDM2 xxxx xxxx | CANIDM3 xxxx xxxx | CANIDM4 xxxx xxxx | C7h |
| B8h | IPL0 x000 0000 | SADEN 0000 0000 | CANSIT1 0000 0000 | CANSIT2 0000 0000 | CANIDT1 xxxx xxxx | CANIDT2 xxxx xxxx | CANIDT3 xxxx xxxx | CANIDT4 xxxx xxxx | BFh |
| B0h | P3 1111 1111 | CANPAGE 0000 0000 | CANSTCH xxxx xxxx | CANCONCH xxxx xxxx | CANBT1 xxxx xxxx | CANBT2 xxxx xxxx | CANBT3 xxxx xxxx | IPH0 x000 0000 | B7h |
| A8h | IEN0 0000 0000 | SADDR 0000 0000 | CANGSTA x0x0 0000 | CANGCON 0000 0x00 | CANTIML 0000 0000 | CANTIMH 0000 0000 | CANSTMPL 0000 0000 | CANSTMPH 0000 0000 | AFh |
| A0h | P2 1111 1111 | CANTCON 0000 0000 | AUXR1 xxxx 00x0 | CANMSG xxxx xxxx | CANTTCL 0000 0000 | CANTTCH 0000 0000 | WDTRST 1111 1111 | WDTPRG xxxx x000 | A7h |
| 98h | SCON 0000 0000 | SBUF 0000 0000 | | CANGIT 0x00 0000 | CANTEC 0000 0000 | CANREC 0000 0000 | | CKCON1 xxxx xxx0 | 9Fh |
| 90h | P1 1111 1111 | | | | | | | | 97h |
| 88h | TCON 0000 0000 | TMOD 0000 0000 | TL0 0000 0000 | TL1 0000 0000 | TH0 0000 0000 | TH1 0000 0000 | AUXR x001 0100 | CKCON0 0000 0000 | 8Fh |
| 80h | P0 1111 1111 | SP 0000 0111 | DPL 0000 0000 | DPH 0000 0000 | | | | PCON 00x1 0000 | 87h |
| | 0/8[2] | 1/9 | 2/A | 3/B | 4/C | 5/D | 6/E | 7/F | |

Reserved

Note:
1. Do not read or write Reserved Registers
2. These registers are bit–addressable.
   Sixteen addresses in the SFR space are both byte–addressable and bit–addressable. The bit–addressable SFR's are those whose address ends in 0 and 8. The bit addresses, in this area, are 0x80 through to 0xFF.

**Figure 5.** Clock CPU Generation Diagram



# External Space

## Memory Interface

The external memory interface comprises the external bus (port 0 and port 2) as well as the bus control signals (RD#, WR#, and ALE).

Figure 10 shows the structure of the external address bus. P0 carries address A7:0 while P2 carries address A15:8. Data D7:0 is multiplexed with A7:0 on P0. Table 5 describes the external memory interface signals.

**Figure 10.** External Data Memory Interface Structure

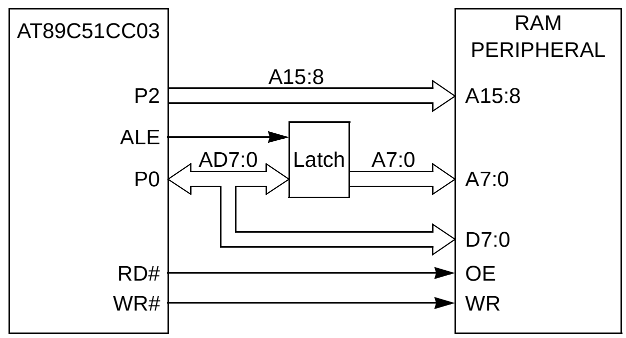



**Table 5.** External Data Memory Interface Signals

| Signal Name | Type | Description | Alternative Function |
|---|---|---|---|
| A15:8 | O | **Address Lines**<br>Upper address lines for the external bus. | P2.7:0 |
| AD7:0 | I/O | **Address/Data Lines**<br>Multiplexed lower address lines and data for the external memory. | P0.7:0 |
| ALE | O | **Address Latch Enable**<br>ALE signals indicates that valid address information are available on lines AD7:0. | - |
| RD# | O | **Read**<br>Read signal output to external data memory. | P3.7 |
| WR# | O | **Write**<br>Write signal output to external memory. | P3.6 |

## External Bus Cycles

This section describes the bus cycles the AT89C51CC03 executes to read (see Figure 11), and write data (see Figure 12) in the external data memory.
External memory cycle takes 6 CPU clock periods. This is equivalent to 12 oscillator clock period in standard mode or 6 oscillator clock periods in X2 mode. For further information on X2 mode.

Slow peripherals can be accessed by stretching the read and write cycles. This is done using the M0 bit in AUXR register. Setting this bit changes the width of the RD# and WR# signals from 3 to 15 CPU clock periods.

For simplicity, the accompanying figures depict the bus cycle waveforms in idealized form and do not provide precise timing information. For bus cycle timing parameters refer to the Section “AC Characteristics” of the AT89C51CC03 datasheet.

*Power Down Request*

Before entering in Power Down (Set bit PD in PCON register) the user should check that no write sequence is in progress (check BUSY=0), then check that the column latches are reset (FLOAD=0 in FSTA register. Launch a reset column latches to clear FLOAD if necessary.

**Reading the Flash Spaces**

*User*

The following procedure is used to read the User space:

- Read one byte in Accumulator by executing MOVC A,@A+DPTR with A+DPTR=read@.

Note: FCON is supposed to be reset when not needed.

*Extra Row*

The following procedure is used to read the Extra Row space and is summarized in Figure 28:

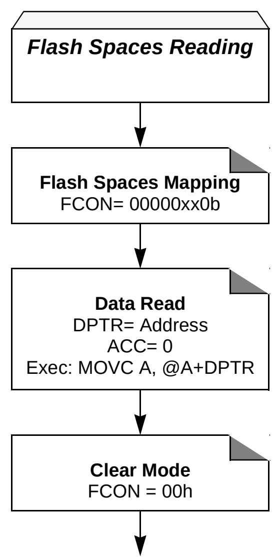
- Map the Extra Row space by writing 02h in FCON register.
- Read one byte in Accumulator by executing MOVC A,@A+DPTR with A = 0 and DPTR = FF80h to FFFFh.
- Clear FCON to unmap the Extra Row.

*Hardware Security Byte*

The following procedure is used to read the Hardware Security space and is summarized in Figure 28:

- Map the Hardware Security space by writing 04h in FCON register.
- Read the byte in Accumulator by executing MOVC A,@A+DPTR with A = 0 and DPTR = 0000h.

**Figure 28.** Clear FCON to unmap the Hardware Security Byte.Reading Procedure




**Flash Protection from Parallel Programming**

The three lock bits in Hardware Security Byte (see "In-System Programming" section) are programmed according to Table 17 provide different level of protection for the on-chip code and data located in FM0 and FM1.

The only way to write this bits are the parallel mode. They are set by default to level 4

**Table 31.** TMOD Register

TMOD (S:89h)
Timer/Counter Mode Control Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| GATE1 | C/T1# | M11 | M01 | GATE0 | C/T0# | M10 | M00 |

| Bit Number | Bit Mnemonic | Description |
|---|---|---|
| 7 | GATE1 | **Timer 1 Gating Control Bit**<br>Clear to enable Timer 1 whenever TR1 bit is set.<br>Set to enable Timer 1 only while INT1# pin is high and TR1 bit is set. |
| 6 | C/T1# | **Timer 1 Counter/Timer Select Bit**<br>Clear for Timer operation: Timer 1 counts the divided-down system clock.<br>Set for Counter operation: Timer 1 counts negative transitions on external pin T1. |
| 5 | M11 | **Timer 1 Mode Select Bits**<br>M11 M01 Operating mode<br>0 0 Mode 0: 8-bit Timer/Counter (TH1) with 5-bit prescaler (TL1).<br>0 1 Mode 1: 16-bit Timer/Counter.<br>1 0 Mode 2: 8-bit auto-reload Timer/Counter (TL1) (1)<br>1 1 Mode 3: Timer 1 halted. Retains count |
| 4 | M01 | |
| 3 | GATE0 | **Timer 0 Gating Control Bit**<br>Clear to enable Timer 0 whenever TR0 bit is set.<br>Set to enable Timer/Counter 0 only while INT0# pin is high and TR0 bit is set. |
| 2 | C/T0# | **Timer 0 Counter/Timer Select Bit**<br>Clear for Timer operation: Timer 0 counts the divided-down system clock.<br>Set for Counter operation: Timer 0 counts negative transitions on external pin T0. |
| 1 | M10 | **Timer 0 Mode Select Bit**<br>M10 M00 Operating mode<br>0 0 Mode 0: 8-bit Timer/Counter (TH0) with 5-bit prescaler (TL0).<br>0 1 Mode 1: 16-bit Timer/Counter.<br>1 0 Mode 2: 8-bit auto-reload Timer/Counter (TL0) (2)<br>1 1 Mode 3: TL0 is an 8-bit Timer/Counter<br>TH0 is an 8-bit Timer using Timer 1's TR0 and TF0 bits. |
| 0 | M00 | |

1. Reloaded from TH1 at overflow.
2. Reloaded from TH0 at overflow.

Reset Value = 0000 0000b

## Registers

**Table 36.** T2CON Register

T2CON (S:C8h)
Timer 2 Control Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| TF2 | EXF2 | RCLK | TCLK | EXEN2 | TR2 | C/T2# | CP/RL2# |

| Bit Number | Bit Mnemonic | Description |
|---|---|---|
| 7 | TF2 | **Timer 2 Overflow Flag**<br>TF2 is not set if RCLK=1 or TCLK = 1.<br>Must be cleared by software.<br>Set by hardware on timer 2 overflow. |
| 6 | EXF2 | **Timer 2 External Flag**<br>Set when a capture or a reload is caused by a negative transition on T2EX pin if EXEN2=1.<br>Set to cause the CPU to vector to timer 2 interrupt routine when timer 2 interrupt is enabled.<br>Must be cleared by software. |
| 5 | RCLK | **Receive Clock bit**<br>Clear to use timer 1 overflow as receive clock for serial port in mode 1 or 3.<br>Set to use timer 2 overflow as receive clock for serial port in mode 1 or 3. |
| 4 | TCLK | **Transmit Clock bit**<br>Clear to use timer 1 overflow as transmit clock for serial port in mode 1 or 3.<br>Set to use timer 2 overflow as transmit clock for serial port in mode 1 or 3. |
| 3 | EXEN2 | **Timer 2 External Enable bit**<br>Clear to ignore events on T2EX pin for timer 2 operation.<br>Set to cause a capture or reload when a negative transition on T2EX pin is detected, if timer 2 is not used to clock the serial port. |
| 2 | TR2 | **Timer 2 Run Control bit**<br>Clear to turn off timer 2.<br>Set to turn on timer 2. |
| 1 | C/T2# | **Timer/Counter 2 Select bit**<br>Clear for timer operation (input from internal clock system: $F_{OSC}$).<br>Set for counter operation (input from T2 input pin). |
| 0 | CP/RL2# | **Timer 2 Capture/Reload bit**<br>If RCLK=1 or TCLK=1, CP/RL2# is ignored and timer is forced to auto-reload on timer 2 overflow.<br>Clear to auto-reload on timer 2 overflows or negative transitions on T2EX pin if EXEN2=1.<br>Set to capture on negative transitions on T2EX pin if EXEN2=1. |

Reset Value = 0000 0000b
Bit addressable

**Table 39.** TL2 Register

TL2 (S:CCh)
Timer 2 Low Byte Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| - | - | - | - | - | - | - | - |

| Bit Number | Bit Mnemonic | Description |
|---|---|---|
| 7-0 | | Low Byte of Timer 2. |

Reset Value = 0000 0000b
Not bit addressable

**Table 40.** RCAP2H Register

RCAP2H (S:CBh)
Timer 2 Reload/Capture High Byte Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| - | - | - | - | - | - | - | - |

| Bit Number | Bit Mnemonic | Description |
|---|---|---|
| 7-0 | | High Byte of Timer 2 Reload/Capture. |

Reset Value = 0000 0000b
Not bit addressable

**Table 41.** RCAP2L Register

RCAP2L (S:CAH)
TIMER 2 REload/Capture Low Byte Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| - | - | - | - | - | - | - | - |

| Bit Number | Bit Mnemonic | Description |
|---|---|---|
| 7-0 | | Low Byte of Timer 2 Reload/Capture. |

Reset Value = 0000 0000b
Not bit addressable

## Watchdog Timer During Power-down Mode and Idle

In Power-down mode the oscillator stops, which means the WDT also stops. While in Power-down mode, the user does not need to service the WDT. There are 2 methods of exiting Power-down mode: by a hardware reset or via a level activated external interrupt which is enabled prior to entering Power-down mode. When Power-down is exited with hardware reset, the Watchdog is disabled. Exiting Power-down with an interrupt is significantly different. The interrupt shall be held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service for the interrupt used to exit Power-down.

To ensure that the WDT does not overflow within a few states of exiting powerdown, it is best to reset the WDT just before entering powerdown.

In the Idle mode, the oscillator continues to run. To prevent the WDT from resetting AT89C51CC03 while in Idle mode, the user should always set up a timer that will periodically exit Idle, service the WDT, and re-enter Idle mode.

## Register

**Table 44.** WDTPRG Register

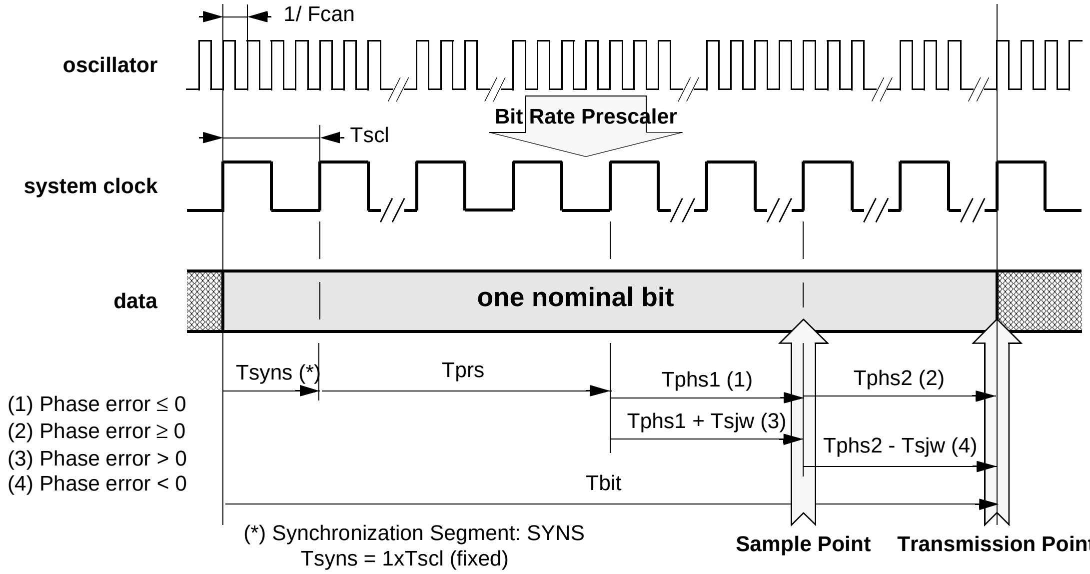
WDTPRG (S:A7h)
Watchdog Timer Duration Programming Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| – | – | – | – | – | S2 | S1 | S0 |

| Bit Number | Bit Mnemonic | Description |
|---|---|---|
| 7 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 6 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 5 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 4 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 3 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 2 | S2 | **Watchdog Timer Duration selection bit 2**<br>Work in conjunction with bit 1 and bit 0. |
| 1 | S1 | **Watchdog Timer Duration selection bit 1**<br>Work in conjunction with bit 2 and bit 0. |
| 0 | S0 | **Watchdog Timer Duration selection bit 0**<br>Work in conjunction with bit 1 and bit 2. |

Reset Value = XXXX X000b

**Figure 52.** General Structure of a Bit Period




Tbit calculation: $Tbit = Tsyns + Tprs + Tphs1 + Tphs2$

**example of bit timing determination for CAN baudrate of 500kbit/s:**
Fosc = 12 MHz in X1 mode => FCAN = 6 MHz

Verify that the CAN baud rate you want is an integer division of FCAN clock.

FCAN/CAN baudrate = 6 MHz/500 kHz = 12

The time quanta TQ must be comprised between 8 and 25: TQ = 12 and **BRP = 0**

Define the various timing parameters: Tbit = Tsyns + Tprs + Tphs1 + Tphs2 = 12TQ

Tsyns = 1TQ and Tsjw =1TQ => **SJW = 0**

If we chose a sample point at 66.6% => Tphs2 = 4TQ => **PHS2 = 3**

Tbit = 12 = 4 + 1 + Tphs1 + Tprs, let us choose Tprs = 3 Tphs1 = 4

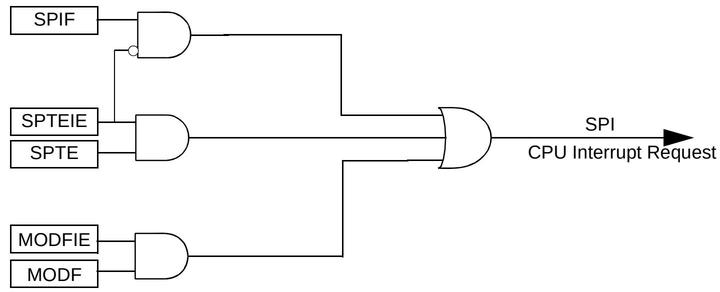
**PHS1 = 3** and **PRS = 2**

BRP = 0 so CANBT1 = 00h

SJW = 0 and PRS = 2 so CANBT2 = 04h

PHS2 = 3 and PHS1 = 3 so CANBT3 = 36h

**Figure 66. SPI Interrupt Requests Generation**




## Registers

Three registers in the SPI module provide control, status and data storage functions. These registers are describe in the following paragraphs.

### *Serial Peripheral Control Register (SPCON)*

- The Serial Peripheral Control Register does the following:
- Selects one of the Master clock rates
- Configure the SPI Module as Master or Slave
- Selects serial clock polarity and phase
- Enables the SPI Module
- Frees the SS pin for a general-purpose

Table 92 describes this register and explains the use of each bit

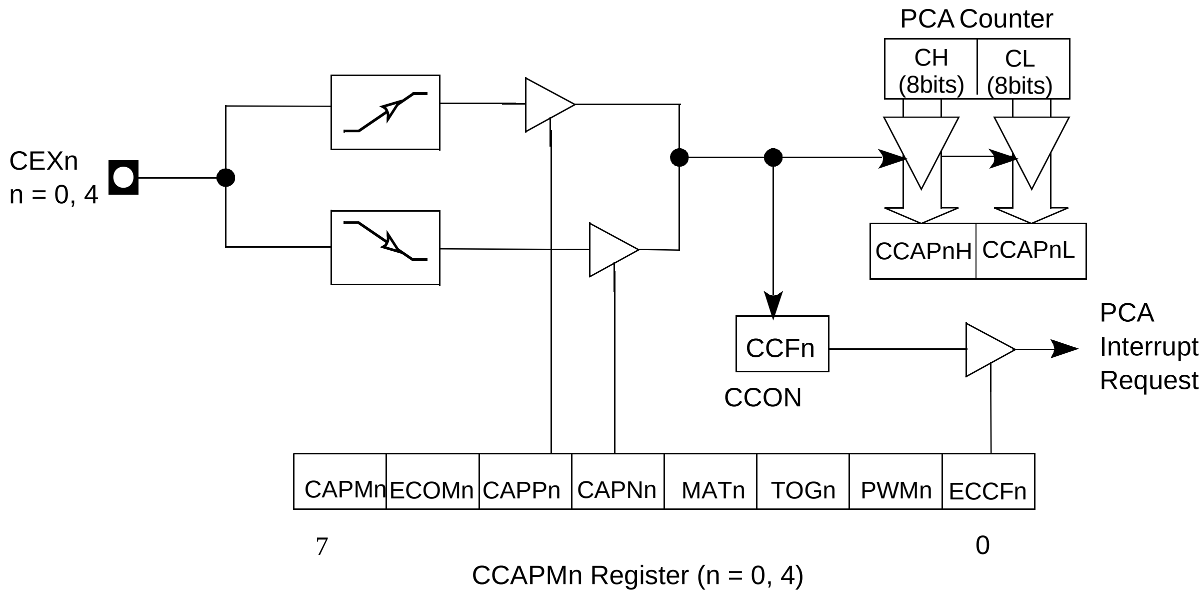
**Table 92.** SPCON Register

SPCON - Serial Peripheral Control Register (0D4H)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **SPR2** | **SPEN** | **SSDIS** | **MSTR** | **CPOL** | **CPHA** | **SPR1** | **SPR0** |

| Bit Number | Bit Mnemonic | Description |
|---|---|---|
| 7 | SPR2 | **Serial Peripheral Rate 2**<br>Bit with SPR1 and SPR0 define the clock rate (See bits SPR1 and SPR0 for detail). |
| 6 | SPEN | **Serial Peripheral Enable**<br>Cleared to disable the SPI interface (internal reset of the SPI).<br>Set to enable the SPI interface. |
| 5 | SSDIS | **$\overline{SS}$ Disable**<br>Cleared to enable $\overline{SS}$ in both Master and Slave modes.<br>Set to disable $\overline{SS}$ in both Master and Slave modes. In Slave mode, this bit has no effect if CPHA ='0'. When SSDIS is set, no MODF interrupt request is generated. |
| 4 | MSTR | **Serial Peripheral Master**<br>Cleared to configure the SPI as a Slave.<br>Set to configure the SPI as a Master. |

**Figure 69.** PCA Capture Mode




## 16-bit Software Timer Mode

The PCA modules can be used as software timers by setting both the ECOM and MAT bits in the modules CCAPMn register. The PCA timer will be compared to the module's capture registers and when a match occurs an interrupt will occur if the CCFn (CCON SFR) and the ECCFn (CCAPMn SFR) bits for the module are both set.

**Figure 70.** PCA 16-bit Software Timer and High Speed Output Mode

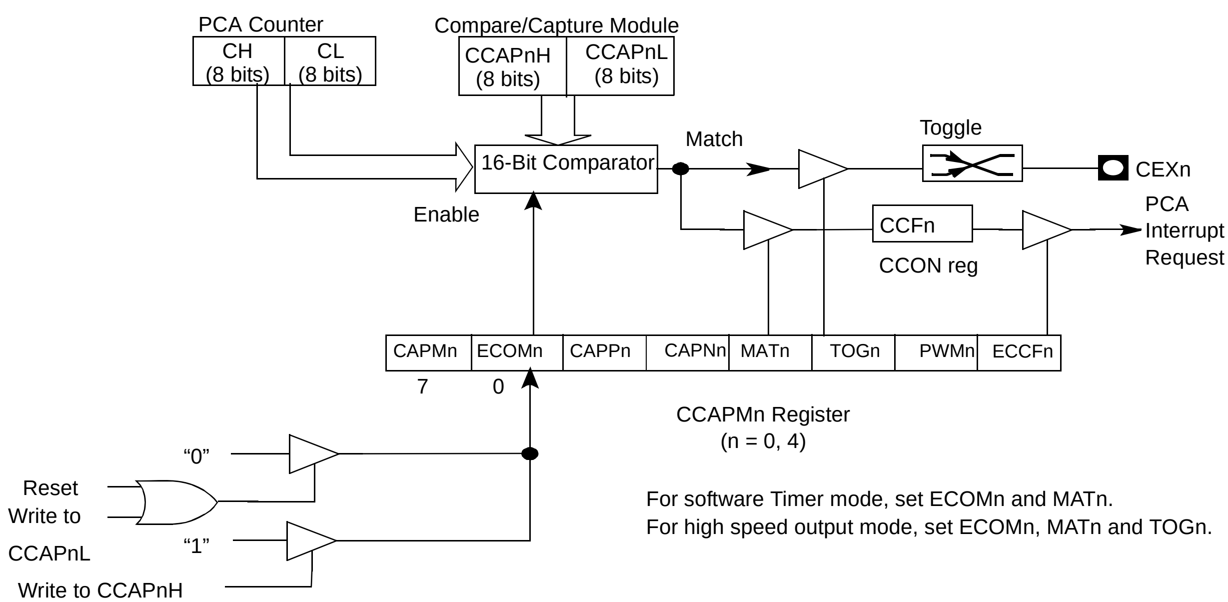


**Figure 73.** ADC Description

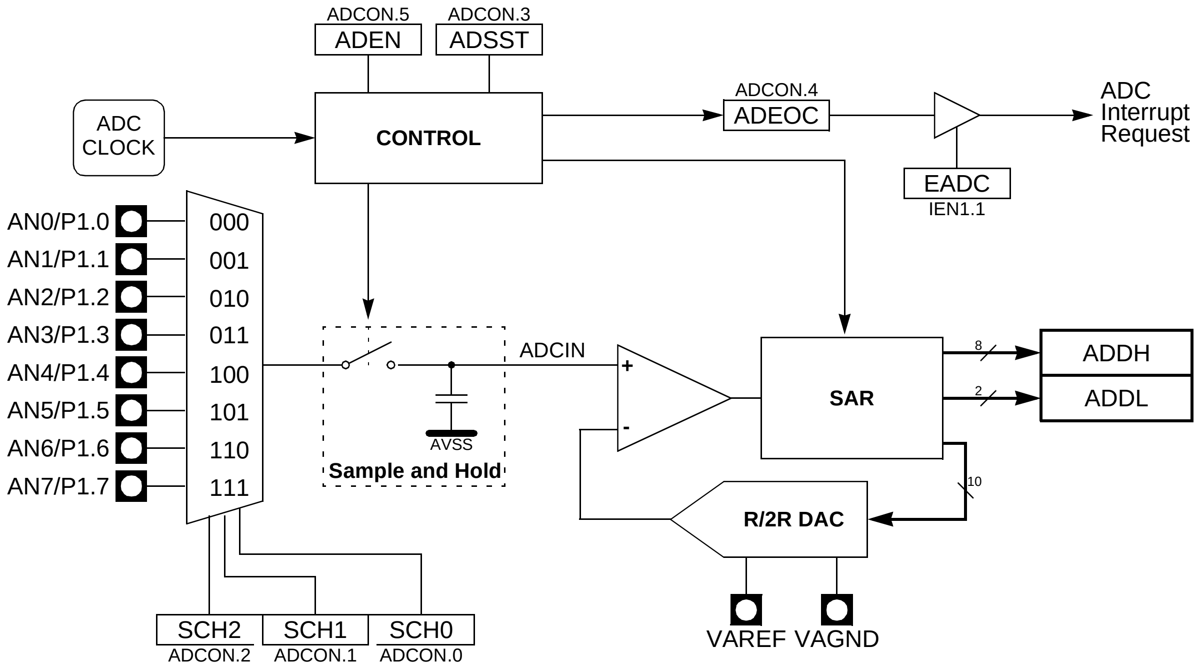
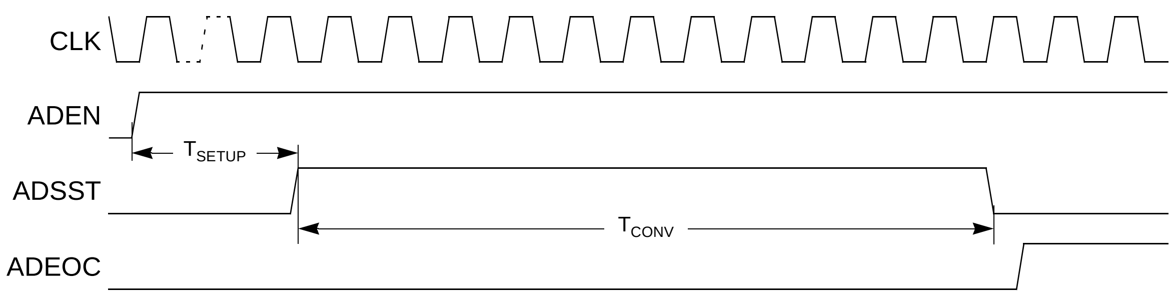


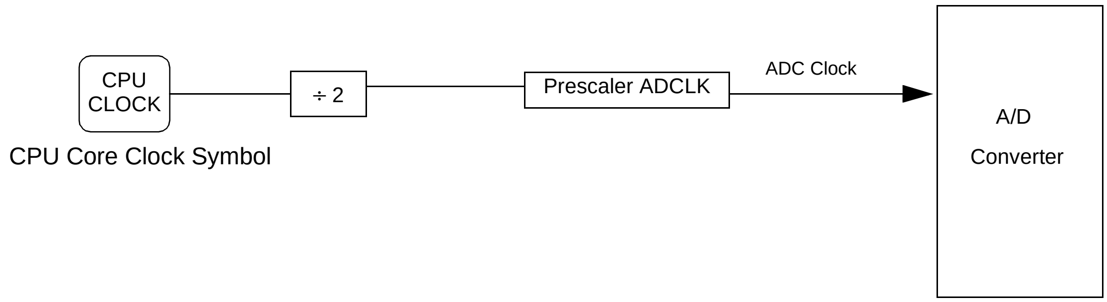

Figure 74 shows the timing diagram of a complete conversion. For simplicity, the figure depicts the waveforms in idealized form and do not provide precise timing information. For ADC characteristics and timing parameters refer to the Section “AC Characteristics” of the AT89C51CC03 datasheet.

**Figure 74.** Timing Diagram




Note: Tsetup min = 4 us
Tconv=11 clock ADC = 1sample and hold + 10 bit conversion
The user must ensure that 4 us minimum time between setting ADEN and the start of the first conversion.

**Figure 75.** A/D Converter Clock



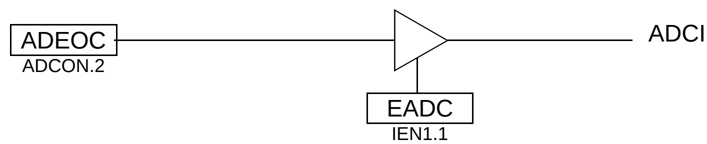

## ADC Standby Mode

When the ADC is not used, it is possible to set it in standby mode by clearing bit ADEN in ADCON register. In this mode its power dissipation is about 1 µW.

## IT ADC Management

An interrupt end-of-conversion will occurs when the bit ADEOC is activated and the bit EADC is set. For re-arming the interrupt the bit ADEOC must be cleared by software.

**Figure 76.** ADC Interrupt Structure




## Routines examples

1. Configure P1.2 and P1.3 in ADC channels

```
// configure channel P1.2 and P1.3 for ADC
 ADCF = 0Ch

// Enable the ADC
 ADCON = 20h
```

2. Start a standard conversion

```
// The variable "channel" contains the channel to convert
// The variable "value_converted" is an unsigned int
// Clear the field SCH[2:0]
 ADCON and = F8h
// Select channel
 ADCON | = channel
// Start conversion in standard mode
 ADCON | = 08h
// Wait flag End of conversion
 while((ADCON and 01h)! = 01h)
// Clear the End of conversion flag
 ADCON and = EFh
// read the value
 value_converted = (ADDH << 2)+(ADDL)
```

3. Start a precision conversion (need interrupt ADC)

```
// The variable "channel" contains the channel to convert
// Enable ADC
```

Each of the interrupt sources can be individually enabled or disabled by setting or clearing a bit in the Interrupt Enable register. This register also contains a global disable bit which must be cleared to disable all the interrupts at the same time.

Each interrupt source can also be individually programmed to one of four priority levels by setting or clearing a bit in the Interrupt Priority registers. The Table below shows the bit values and priority levels associated with each combination.

**Table 108.** Priority Level Bit Values

| IPH.x | IPL.x | Interrupt Level Priority |
|---|---|---|
| 0 | 0 | 0 (Lowest) |
| 0 | 1 | 1 |
| 1 | 0 | 2 |
| 1 | 1 | 3 (Highest) |

A low-priority interrupt can be interrupted by a high priority interrupt but not by another low-priority interrupt. A high-priority interrupt cannot be interrupted by any other interrupt source.

If two interrupt requests of different priority levels are received simultaneously, the request of the higher priority level is serviced. If interrupt requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence, see Table 109.

**Table 109.** Interrupt priority Within level

| Interrupt Name | Interrupt Address Vector | Priority Number |
|---|---|---|
| external interrupt (INT0) | 0003h | 1 |
| Timer0 (TF0) | 000Bh | 2 |
| external interrupt (INT1) | 0013h | 3 |
| Timer1 (TF1) | 001Bh | 4 |
| PCA (CF or CCFn) | 0033h | 5 |
| UART (RI or TI) | 0023h | 6 |
| Timer2 (TF2) | 002Bh | 7 |
| CAN (Txok, Rxok, Err or OvrBuf) | 003Bh | 8 |
| ADC (ADCI) | 0043h | 9 |
| CAN Timer Overflow (OVRTIM) | 004Bh | 10 |
| SPI interrupt | 0053h | 11 |

## External Program Memory Characteristics

**Table 118.** Symbol Description

| Symbol | Parameter |
|---|---|
| T | Oscillator clock period |
| $T_{LHLL}$ | ALE pulse width |
| $T_{AVLL}$ | Address Valid to ALE |
| $T_{LLAX}$ | Address Hold After ALE |
| $T_{LLIV}$ | ALE to Valid Instruction In |
| $T_{LLPL}$ | ALE to $\overline{PSEN}$ |
| $T_{PLPH}$ | $\overline{PSEN}$ Pulse Width |
| $T_{PLIV}$ | $\overline{PSEN}$ to Valid Instruction In |
| $T_{PXIX}$ | Input Instruction Hold After $\overline{PSEN}$ |
| $T_{PXIZ}$ | Input Instruction Float After $\overline{PSEN}$ |
| $T_{AVIV}$ | Address to Valid Instruction In |
| $T_{PLAZ}$ | $\overline{PSEN}$ Low to Address Float |

**Table 119.** AC Parameters for a Fix Clock (F = 40 MHz)

| Symbol | Min | Max | Units |
|---|---|---|---|
| T | 25 | | ns |
| $T_{LHLL}$ | 40 | | ns |
| $T_{AVLL}$ | 10 | | ns |
| $T_{LLAX}$ | 10 | | ns |
| $T_{LLIV}$ | | 70 | ns |
| $T_{LLPL}$ | 15 | | ns |
| $T_{PLPH}$ | 55 | | ns |
| $T_{PLIV}$ | | 35 | ns |
| $T_{PXIX}$ | 0 | | ns |
| $T_{PXIZ}$ | | 18 | ns |
| $T_{AVIV}$ | | 85 | ns |
| $T_{PLAZ}$ | | 10 | ns |

**Table 123.** AC Parameters for a Variable Clock

| Symbol | Type | Standard Clock | X2 Clock | X parameter | Units |
|---|---|---|---|---|---|
| $T_{RLRH}$ | Min | 6 T - x | 3 T - x | 20 | ns |
| $T_{WLWH}$ | Min | 6 T - x | 3 T - x | 20 | ns |
| $T_{RLDV}$ | Max | 5 T - x | 2.5 T - x | 25 | ns |
| $T_{RHDX}$ | Min | x | x | 0 | ns |
| $T_{RHDZ}$ | Max | 2 T - x | T - x | 20 | ns |
| $T_{LLDV}$ | Max | 8 T - x | 4T -x | 40 | ns |
| $T_{AVDV}$ | Max | 9 T - x | 4.5 T - x | 60 | ns |
| $T_{LLWL}$ | Min | 3 T - x | 1.5 T - x | 25 | ns |
| $T_{LLWL}$ | Max | 3 T + x | 1.5 T + x | 25 | ns |
| $T_{AVWL}$ | Min | 4 T - x | 2 T - x | 25 | ns |
| $T_{QVWX}$ | Min | T - x | 0.5 T - x | 15 | ns |
| $T_{QVWH}$ | Min | 7 T - x | 3.5 T - x | 25 | ns |
| $T_{WHQX}$ | Min | T - x | 0.5 T - x | 10 | ns |
| $T_{RLAZ}$ | Max | x | x | 0 | ns |
| $T_{WHLH}$ | Min | T - x | 0.5 T - x | 15 | ns |
| $T_{WHLH}$ | Max | T + x | 0.5 T + x | 15 | ns |

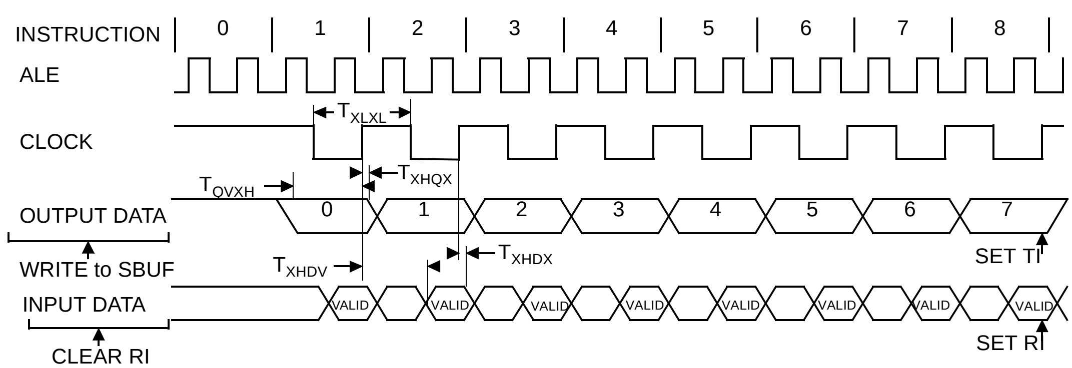
**Table 125.** AC Parameters for a Fix Clock (F = 40 MHz)

| Symbol | Min | Max | Units |
|---|---|---|---|
| $T_{XLXL}$ | 300 | | ns |
| $T_{QVHX}$ | 200 | | ns |
| $T_{XHQX}$ | 30 | | ns |
| $T_{XHDX}$ | 0 | | ns |
| $T_{XHDV}$ | | 117 | ns |

**Table 126.** AC Parameters for a Variable Clock

| Symbol | Type | Standard Clock | X2 Clock | X parameter for -M range | Units |
|---|---|---|---|---|---|
| $T_{XLXL}$ | Min | 12 T | 6 T | | ns |
| $T_{QVHX}$ | Min | 10 T - x | 5 T - x | 50 | ns |
| $T_{XHQX}$ | Min | 2 T - x | T - x | 20 | ns |
| $T_{XHDX}$ | Min | x | x | 0 | ns |
| $T_{XHDV}$ | Max | 10 T - x | 5 T- x | 133 | ns |

## Shift Register Timing Waveforms




## External Clock Drive Characteristics (XTAL1)

**Table 127.** AC Parameters

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $T_{CLCL}$ | Oscillator Period | 25 | | ns |
| $T_{CHCX}$ | High Time | 5 | | ns |
| $T_{CLCX}$ | Low Time | 5 | | ns |
| $T_{CLCH}$ | Rise Time | | 5 | ns |
| $T_{CHCL}$ | Fall Time | | 5 | ns |
| $T_{CHCX}/T_{CLCX}$ | Cyclic ratio in X2 mode | 40 | 60 | % |

STANDARD NOTES FOR PLCC

1/ CONTROLLING DIMENSIONS : INCHES

2/ DIMENSIONING AND TOLERANCING PER ANSI Y 14.5M - 1982.

3/ "D" AND "E1" DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTUSIONS. MOLD FLASH OR PROTUSIONS SHALL NOT EXCEED 0.20 mm (.008 INCH) PER SIDE.

## STANDARD NOTES FOR PQFP/ VQFP / TQFP / DQFP

1/ CONTROLLING DIMENSIONS : INCHES

2/ ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y 14.5M - 1982.

3/ "D1 AND E1" DIMENSIONS DO NOT INCLUDE MOLD PROTUSIONS.
MOLD PROTUSIONS SHALL NOT EXCEED 0.25 mm (0.010 INCH).
THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM
PACKAGE BODY SIZE BY AS MUCH AS 0.15 mm.

4/ DATUM PLANE "H" LOCATED AT MOLD PARTING LINE AND
COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT
BOTTOM OF PARTING LINE.

5/ DATUM "A" AND "D" TO BE DETERMINED AT DATUM PLANE H.

6/ DIMENSION " f " DOES NOT INCLUDE DAMBAR PROTUSION ALLOWABLE
DAMBAR PROTUSION SHALL BE 0.08mm/.003" TOTAL IN EXCESS OF THE
" f " DIMENSION AT MAXIMUM MATERIAL CONDITION .
DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.