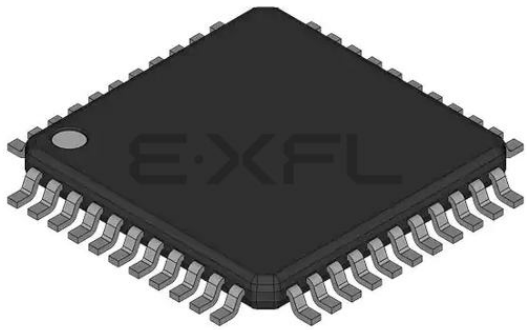


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	80C51
Core Size	8-Bit
Speed	40MHz
Connectivity	CANbus, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	36
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-VQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/atmel/at89c51cc03ua-rltum

write the new byte back to the latch. These Read-Modify-Write instructions are directed to the latch rather than the pin in order to avoid possible misinterpretation of voltage (and therefore, logic) levels at the pin. For example, a Port bit used to drive the base of an external bipolar transistor can not rise above the transistor's base-emitter junction voltage (a value lower than VIL). With a logic one written to the bit, attempts by the CPU to read the Port at the pin are misinterpreted as logic zero. A read of the latch rather than the pins returns the correct logic-one value.

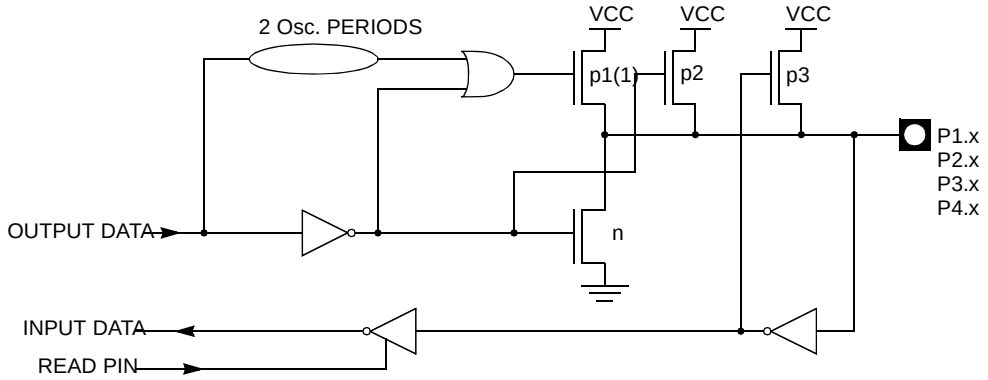
Quasi-Bidirectional Port Operation

Port 1, Port 2, Port 3 and Port 4 have fixed internal pull-ups and are referred to as "quasi-bidirectional" Ports. When configured as an input, the pin impedance appears as logic one and sources current in response to an external logic zero condition. Port 0 is a "true bidirectional" pin. The pins float when configured as input. Resets write logic one to all Port latches. If logical zero is subsequently written to a Port latch, it can be returned to input conditions by a logical one written to the latch.

Note: Port latch values change near the end of Read-Modify-Write instruction cycles. Output buffers (and therefore the pin state) update early in the instruction after Read-Modify-Write instruction cycle.

Logical zero-to-one transitions in Port 1, Port 2, Port 3 and Port 4 use an additional pull-up (p1) to aid this logic transition (see Figure 4.). This increases switch speed. This extra pull-up sources 100 times normal internal circuit current during 2 oscillator clock periods. The internal pull-ups are field-effect transistors rather than linear resistors. Pull-ups consist of three p-channel FET (pFET) devices. A pFET is on when the gate senses logical zero and off when the gate senses logical one. pFET #1 is turned on for two oscillator periods immediately after a zero-to-one transition in the Port latch. A logical one at the Port pin turns on pFET #3 (a weak pull-up) through the inverter. This inverter and pFET pair form a latch to drive logical one. pFET #2 is a very weak pull-up switched on whenever the associated nFET is switched off. This is traditional CMOS switch convention. Current strengths are 1/10 that of pFET #3.

Figure 4. Internal Pull-Up Configurations



Note: Port 2 p1 assists the logic-one output for memory bus cycles.

Data Memory

The AT89C51CC03 provides data memory access in two different spaces:

1. The internal space mapped in three separate segments:
- the lower 128 Bytes RAM segment.
- the upper 128 Bytes RAM segment.
- the expanded 2048 Bytes RAM segment (ERAM).
2. The external space.

A fourth internal segment is available but dedicated to Special Function Registers, SFRs, (addresses 80h to FFh) accessible by direct addressing mode.

Figure 8 shows the internal and external data memory spaces organization.

Figure 7. Internal Memory - RAM

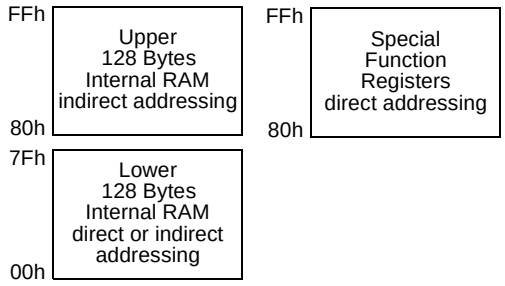
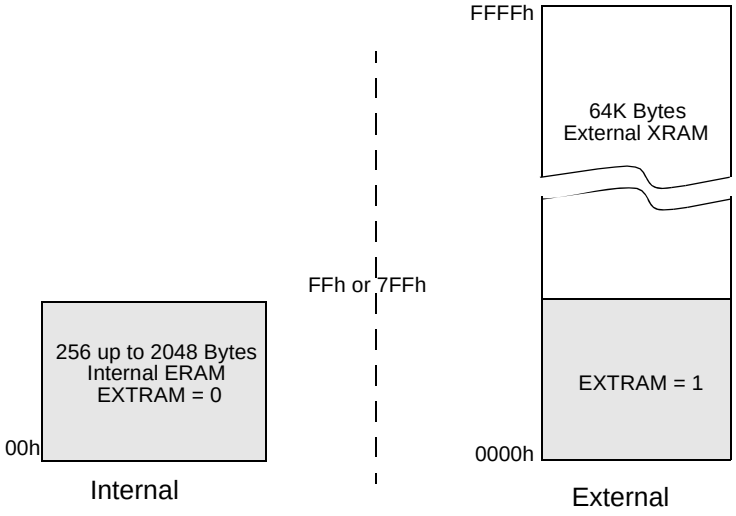


Figure 8. Internal and External Data Memory Organization ERAM-XRAM



Entering Power-Down Mode

To enter Power-Down mode, set PD bit in PCON register. The AT89C51CC03 enters the Power-Down mode upon execution of the instruction that sets PD bit. The instruction that sets PD bit is the last instruction executed.

Exiting Power-Down Mode

Note: If VCC was reduced during the Power-Down mode, do not exit Power-Down mode until VCC is restored to the normal operating level.

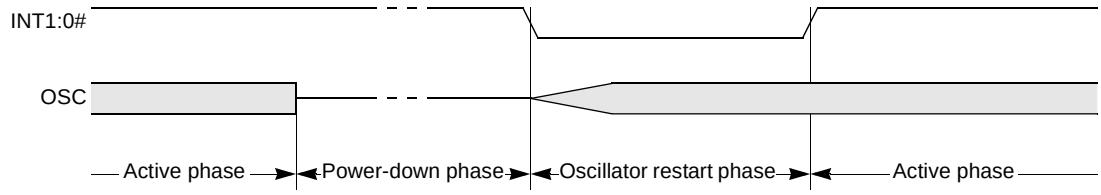
There are two ways to exit the Power-Down mode:

1. Generate an enabled external interrupt.
   – The AT89C51CC03 provides capability to exit from Power-Down using INT0#, INT1#.
   Hardware clears PD bit in PCON register which starts the oscillator and restores the clocks to the CPU and peripherals. Using INTx# input, execution resumes when the input is released (see Figure 19). Execution resumes with the interrupt service routine. Upon completion of the interrupt service routine, program execution resumes with the instruction immediately following the instruction that activated Power-Down mode.

Note: The external interrupt used to exit Power-Down mode must be configured as level sensitive (INT0# and INT1#) and must be assigned the highest priority. In addition, the duration of the interrupt must be long enough to allow the oscillator to stabilize. The execution will only resume when the interrupt is deasserted.

Note: Exit from power-down by external interrupt does not affect the SFRs nor the internal RAM content.

Figure 19. Power-Down Exit Waveform Using INT1:0#

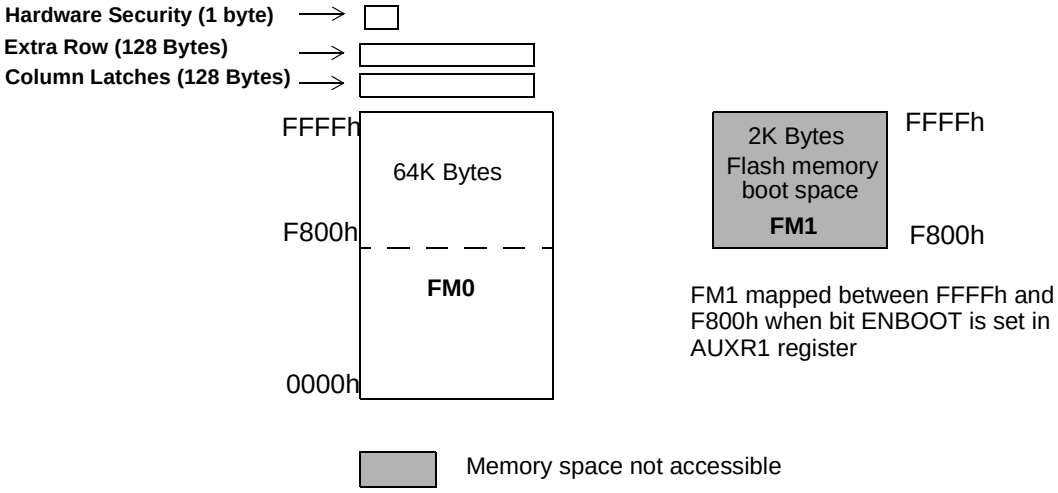


2. Generate a reset.
   – A logic high on the RST pin clears PD bit in PCON register directly and asynchronously. This starts the oscillator and restores the clock to the CPU and peripherals. Program execution momentarily resumes with the instruction immediately following the instruction that activated Power-Down mode and may continue for a number of clock cycles before the internal reset algorithm takes control. Reset initializes the AT89C51CC03 and vectors the CPU to address 0000h.

Note: During the time that execution resumes, the internal RAM cannot be accessed; however, it is possible for the Port pins to be accessed. To avoid unexpected outputs at the Port pins, the instruction immediately following the instruction that activated the Power-Down mode should not write to a Port pin or to the external RAM.

Note: Exit from power-down by reset redefines all the SFRs, but does not affect the internal RAM content.

Figure 24. Flash Memory Architecture with ENBOOT=0 (user modemode)



FM0 Memory Architecture

The Flash memory is made up of 4 blocks (see Figure 23):

- The memory array (user space) 64K Bytes
- The Extra Row
- The Hardware security bits
- The column latch registers

User Space

This space is composed of a 64K Bytes Flash memory organized in 512 pages of 128 Bytes. It contains the user's application code.

Extra Row (XRow)

This row is a part of FM0 and has a size of 128 Bytes. The extra row may contain information for boot loader usage.

Hardware security Byte (HSB)

The Hardware security Byte space is a part of FM0 and has a size of 1 byte.
The 4 MSB can be read/written by software (from FM0 and , the 4 LSB can only be read by software and written by hardware in parallel mode.

H Hardware Security Byte (HSB)

7	6	5	4	3	2	1	0
X2	**BLJB**	**-**	**-**	**-**	**LB2**	**LB1**	**LB0**

Bit Number	Bit Mnemonic	Description
7	X2	**X2 Mode** Programmed (='0') to force X2 mode (6 clocks per instruction) after reset Unprogrammed to force X1 mode, Standard Mode, afetr reset (Default)
6	BLJB	**Boot Loader Jump Bit** When unprogrammed (='1'), at the next reset : -ENBOOT=0 (see code space memory configuration) -Start address is 0000h (PC=0000h) When programmed (='0')at the nex reset: -ENBOOT=1 (see code space memory configuration) -Start address is F800h (PC=F800h)
5	-	**Reserved**
4	-	**Reserved**
3	-	**Reserved**
2-0	LB2-0	**General Memory Lock Bits (only programmable by programmer tools)** Section "Flash Protection from Parallel Programming", page 53

Column Latches

The column latches, also part of FM0, have a size of full page (128 Bytes).
The column latches are the entrance buffers of the three previous memory locations (user array, XROW and Hardware security byte). The column latches are write only and can be accessed only from FM1 (boot mode) and from external memory

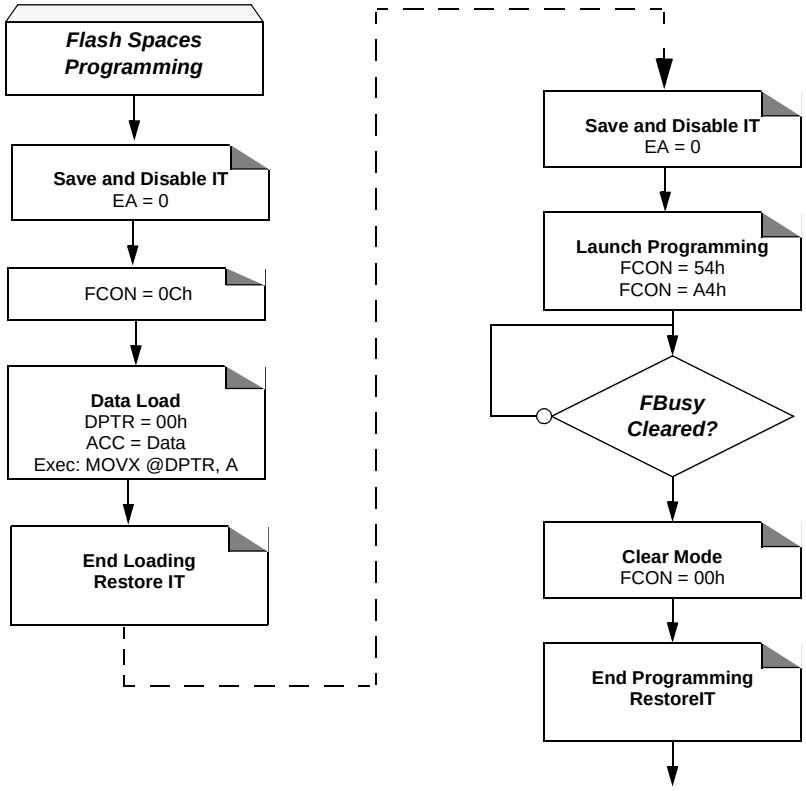
Cross Flash Memory Access Description

The FM0 memory can be program only from FM1. Programming FM0 from FM0 or from external memory is impossible.

The FM1 memory can be program only by parallel programming.

The Table show all software Flash access allowed.

Figure 27. Hardware Programming Procedure



Reset the Column Latches

An automatic reset of the column latches is performed after a successful Flash write sequence. User can also reset the column latches manually, for instance to reload the column latches before writing the Flash. The following procedure is summarized below.

- Save and disable the interrupts.
- Launch the reset by writing the data sequence 56h followed by A6h in FCON register (only from FM1).
- Restore the interrupts.

Error Reports

Flash Programming Sequence Errors

When a wrong sequence is detected, the SEQERR bit in FSTA register is set. Possible wrong sequence are :

- MOV FCON, 5xh instruction not immediately followed by a MOV FCON, Ax instruction.
- A write Flash sequence is launched while no data were loaded in the column latches

The SEQERR bit can be cleared

- By software
- By hardware when a correct programming sequence is completed

When multiple pages are written into the Flash, the user should check FSTA for errors after each write page sequences, not only at the end of the multiple write pages.

Power Down Request

Before entering in Power Down (Set bit PD in PCON register) the user should check that no write sequence is in progress (check BUSY=0), then check that the column latches are reset (FLOAD=0 in FSTA register. Launch a reset column latches to clear FLOAD if necessary.

Reading the Flash Spaces

User

The following procedure is used to read the User space:

- Read one byte in Accumulator by executing MOVC A,@A+DPTR with A+DPTR=read@.

Note: FCON is supposed to be reset when not needed.

Extra Row

The following procedure is used to read the Extra Row space and is summarized in Figure 28:

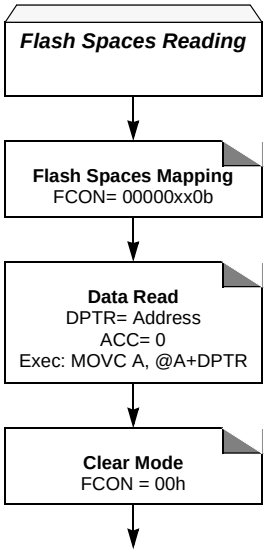
- Map the Extra Row space by writing 02h in FCON register.
- Read one byte in Accumulator by executing MOVC A,@A+DPTR with A = 0 and DPTR = FF80h to FFFFh.
- Clear FCON to unmap the Extra Row.

Hardware Security Byte

The following procedure is used to read the Hardware Security space and is summarized in Figure 28:

- Map the Hardware Security space by writing 04h in FCON register.
- Read the byte in Accumulator by executing MOVC A,@A+DPTR with A = 0 and DPTR = 0000h.

Figure 28. Clear FCON to unmap the Hardware Security Byte.Reading Procedure



Flash Protection from Parallel Programming

The three lock bits in Hardware Security Byte (see "In-System Programming" section) are programmed according to Table 17 provide different level of protection for the on-chip code and data located in FM0 and FM1.

The only way to write this bits are the parallel mode. They are set by default to level 4

Table 17. Program Lock Bit

Program Lock Bits				
Security level	LB0	LB1	LB2	**Protection Description**
1	U	U	U	No program lock features enabled.
2	P	U	U	MOVC instruction executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further parallel programming of the Flash is disabled. ISP and software programming with API are still allowed. Writing EEprom Data from external parallel programmer is disabled but still allowed from internal code execution.
3	U	P	U	Same as 2, also verify through parallel programming interface is disabled. Writing And Reading EEPROM Data from external parallel programmer is disabled but still allowed from internal code execution..
4	U	U	P	Same as 3, also external execution is disabled

Program Lock bits

U: unprogrammed

P: programmed

WARNING: Security level 2 and 3 should only be programmed after Flash and Core verification.

Table 22. Read MOVC A, @DPTR

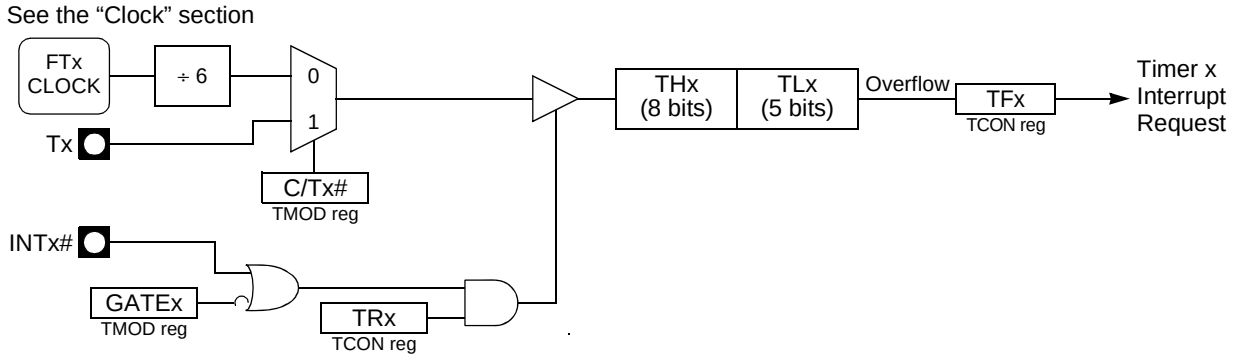
Code Execution	FCON Register			ENBOOT	DPTR	FM1	FM0	XROW	Hardware Byte	External Code
	FMOD1	FMOD0	FPS							
From FM0	0	0	X	0	0000h to FFFFh		OK			
				1	0000h to F7FF		OK			
					F800h to FFFFh	Do not use this configuration				
	0	1	X	X	0000 to 007Fh See (1)			OK		
	1	0	X	X	X				OK	
	1	1	X	0	000h to FFFFh		OK			
				1	0000h to F7FF		OK			
					F800h to FFFFh	Do not use this configuration				
From FM1 (ENBOOT =1	0	0	0	1	0000h to F7FF		OK			
					F800h to FFFFh	OK				
				0	X	NA				
			1	1	X		OK			
				0	X	NA				
	0	1	X	1	0000h to 007h See (2)			OK		
				0		NA				
	1	0	X	1	X				OK	
				0		NA				
	1	1	X	1	000h to FFFFh		OK			
				0		NA				
External code : EA=0 or Code Roll Over	X	0	X	X	X					OK

1. For DPTR higher than 007Fh only lowest 7 bits are decoded, thus the behavior is the same as for addresses from 0000h to 007Fh
2. For DPTR higher than 007Fh only lowest 7 bits are decoded, thus the behavior is the same as for addresses from 0000h to 007Fh

Mode 0 (13-bit Timer)

Mode 0 configures Timer 0 as an 13-bit Timer which is set up as an 8-bit Timer (TH0 register) with a modulo 32 prescaler implemented with the lower five bits of TL0 register (see Figure 35). The upper three bits of TL0 register are indeterminate and should be ignored. Prescaler overflow increments TH0 register.

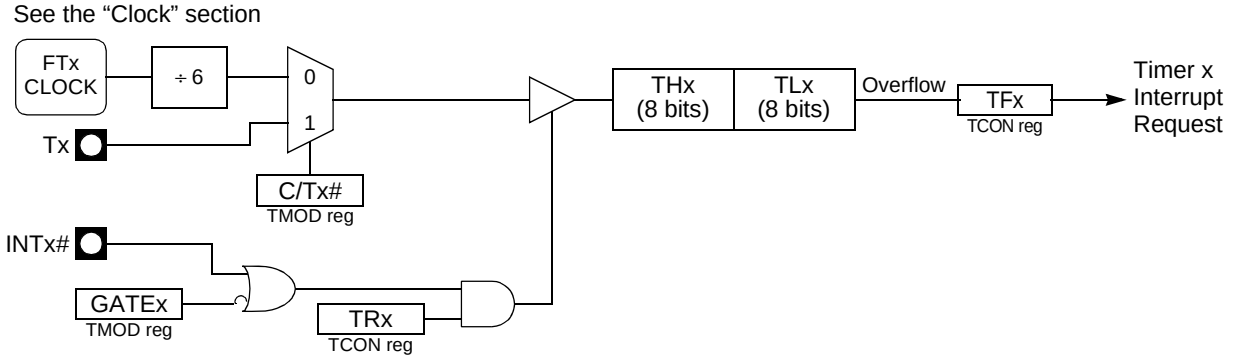
Figure 35. Timer/Counter x (x = 0 or 1) in Mode 0



Mode 1 (16-bit Timer)

Mode 1 configures Timer 0 as a 16-bit Timer with TH0 and TL0 registers connected in cascade (see Figure 36). The selected input increments TL0 register.

Figure 36. Timer/Counter x (x = 0 or 1) in Mode 1



Time Trigger Communication (TTC) and Message Stamping

The AT89C51CC03 has a programmable 16-bit Timer (CANTIMH and CANTIML) for message stamp and TTC.

This CAN Timer starts after the CAN controller is enabled by the ENA bit in the CANGCON register.

Two modes in the timer are implemented:

- Time Trigger Communication:
  - Capture of this timer value in the CANTTCH and CANTTCL registers on Start Of Frame (SOF) or End Of Frame (EOF), depending on the SYNCTTC bit in the CANGCON register, when the network is configured in TTC by the TTC bit in the CANGCON register.

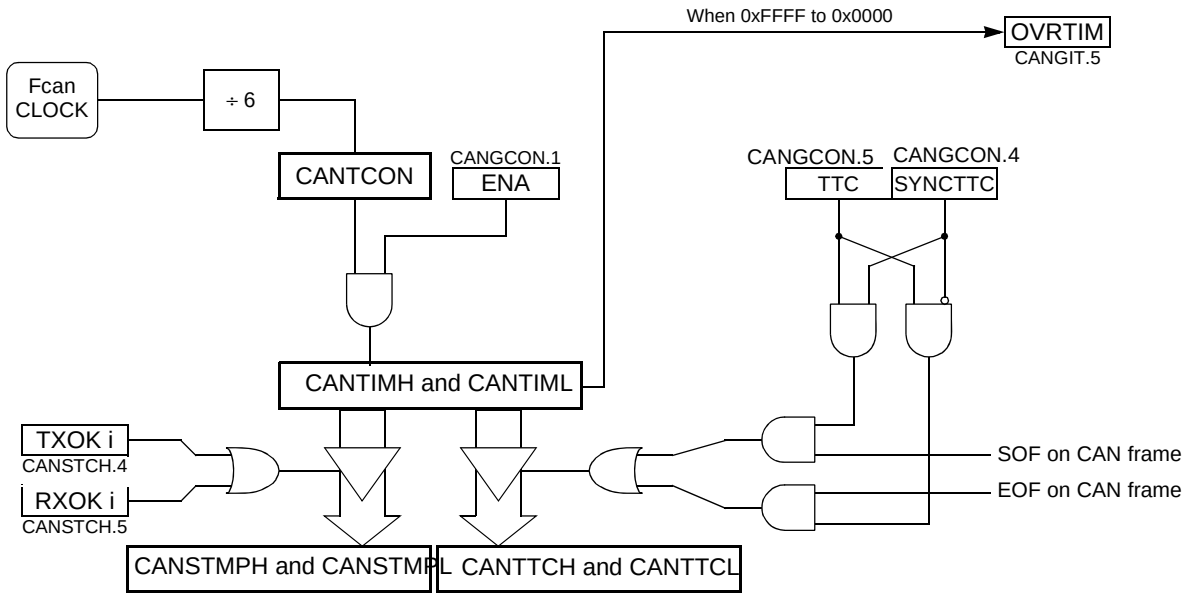
Note: In this mode, CAN ***only sends the frame once, even if an error occurs***.

- Message Stamping
  - Capture of this timer value in the CANSTMPH and CANSTMPL registers of the message object which received or sent the frame.
  - All messages can be stamps.
  - The stamping of a received frame occurs when the RxOk flag is set.
  - The stamping of a sent frame occurs when the TxOk flag is set.

The CAN Timer works in a roll-over from FFFFh to 0000h which serves as a time base.

When the timer roll-over from FFFFh to 0000h, an interrupt is generated if the ETIM bit in the interrupt enable register IEN1 is set.

Figure 55. Block Diagram of CAN Timer



CAN SFR's

Table 47. CAN SFR's With Reset Values

	0/8[1]	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
F8h	IPL1 xxxx x000	CH 0000 0000	CCAP0H 0000 0000	CCAP1H 0000 0000	CCAP2H 0000 0000	CCAP3H 0000 0000	CCAP4H 0000 0000		**FFh**
F0h	B 0000 0000		ADCLK xx00 x000	ADCON 0000 0000	ADDL xxxx xx00	ADDH 0000 0000	ADCF 0000 0000	IPH1 xxxx x000	**F7h**
E8h	IEN1 xxxx x000	CL 0000 0000	CCAP0L 0000 0000	CCAP1L 0000 0000	CCAP2L 0000 0000	CCAP3L 0000 0000	CCAP4L 0000 0000		**EFh**
E0h	ACC 0000 0000								**E7h**
D8h	CCON 00xx xx00	CMOD 00xx x000	CCAPM0 x000 0000	CCAPM1 x000 0000	CCAPM2 x000 0000	CCAPM3 x000 0000	CCAPM4 x000 0000		**DFh**
D0h	PSW 0000 0000	FCON 0000 0000	EECON xxxx xx00	FSTA xxxx xx00	SPCON 0001 0100	SPSCR 0000 0000	SPDAT xxxx xxxx		**D7h**
C8h	T2CON 0000 0000	T2MOD xxxx xx00	RCAP2L 0000 0000	RCAP2H 0000 0000	TL2 0000 0000	TH2 0000 0000	CANEN1 xx00 0000	CANEN2 0000 0000	**CFh**
C0h	P4 xxxx xx11	CANGIE 0000 0000	CANIE1 xx00 0000	CANIE2 0000 0000	CANIDM1 xxxx xxxx	CANIDM2 xxxx xxxx	CANIDM3 xxxx xxxx	CANIDM4 xxxx xxxx	**C7h**
B8h	IPL0 x000 0000	SADEN 0000 0000	CANSIT1 0x00 0000	CANSIT2 0000 0000	CANIDT1 xxxx xxxx	CANIDT2 xxxx xxxx	CANIDT3 xxxx xxxx	CANIDT4 xxxx xxxx	**BFh**
B0h	P3 1111 1111	CANPAGE 0000 0000	CANSTCH xxxx xxxx	CANCONCH xxxx xxxx	CANBT1 xxxx xxxx	CANBT2 xxxx xxxx	CANBT3 xxxx xxxx	IPH0 x000 0000	**B7h**
A8h	IEN0 0000 0000	SADDR 0000 0000	CANGSTA 0000 0000	CANGCON 0000 x000	CANTIML 0000 0000	CANTIMH 0000 0000	CANSTMPL 0000 0000	CANSTMPH 0000 0000	**AFh**
A0h	P2 1111 1111	CANTCON 0000 0000	AUXR1 xxxx 00x0	CANMSG xxxx xxxx	CANTTCL 0000 0000	CANTTCH 0000 0000	WDTRST 1111 1111	WDTPRG xxxx x000	**A7h**
98h	SCON 0000 0000	SBUF 0000 0000		CANGIT 0x00 0000	CANTEC 0000 0000	CANREC 0000 0000		CKCON1 xxxx xxx0	**9Fh**
90h	P1 1111 1111								**97h**
88h	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000	AUXR X001 0100	CKCON 0000 0000	**8Fh**
80h	P0 1111 1111	SP 0000 0111	DPL 0000 0000	DPH 0000 0000				PCON 0000 0000	**87h**
	0/8[1]	**1/9**	**2/A**	**3/B**	**4/C**	**5/D**	**6/E**	**7/F**	

Table 53. CANGIE Register

CANGIE (S:C1h)
CAN General Interrupt Enable

7	6	5	4	3	2	1	0
-	-	ENRX	ENTX	ENERCH	ENBUF	ENERG	-

Bit Number	Bit Mnemonic	Description
7-6	-	**Reserved** The values read from these bits are indeterminate. Do not set these bits.
5	ENRX	**Enable Receive Interrupt** 0 - Disable 1 - Enable
4	ENTX	**Enable Transmit Interrupt** 0 - Disable 1 - Enable
3	ENERCH	**Enable Message Object Error Interrupt** 0 - Disable 1 - Enable
2	ENBUF	**Enable BUF Interrupt** 0 - Disable 1 - Enable
1	ENERG	**Enable General Error Interrupt** 0 - Disable 1 - Enable
0	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.

Note: See Figure 50

Reset Value = xx00 000xb

Table 75. CANIDM2 Register for V2.0 part A

CANIDM2 for V2.0 part A (S:C5h)
CAN Identifier Mask Registers 2

7	6	5	4	3	2	1	0
IDMSK 2	**IDMSK 1**	**IDMSK 0**	**-**	**-**	**-**	**-**	**-**

Bit Number	Bit Mnemonic	Description
7-5	IDTMSK2:0	**IDentifier Mask Value** 0 - comparison true forced. 1 - bit comparison enabled. See Figure 54.
4-0	-	**Reserved** The values read from these bits are indeterminate. Do not set these bits.

No default value after reset.

Table 76. CANIDM3 Register for V2.0 part A

CANIDM3 for V2.0 part A (S:C6h)
CAN Identifier Mask Registers 3

7	6	5	4	3	2	1	0
-	**-**	**-**	**-**	**-**	**-**	**-**	**-**

Bit Number	Bit Mnemonic	Description
7-0	-	**Reserved** The values read from these bits are indeterminate.

No default value after reset.

Table 81. CANIDM4 Register for V2.0 part B

CANIDM4 for V2.0 part B (S:C7h)
CAN Identifier Mask Registers 4

7	6	5	4	3	2	1	0
IDMSK 4	IDMSK 3	IDMSK 2	IDMSK 1	IDMSK 0	RTRMSK	-	IDEMSK

Bit Number	Bit Mnemonic	Description
7-3	IDMSK4:0	**IDentifier Mask Value** 0 - comparison true forced. 1 - bit comparison enabled. See Figure 54.
2	RTRMSK	**Remote Transmission Request Mask Value** 0 - comparison true forced. 1 - bit comparison enabled.
1	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
0	IDEMSK	**IDentifier Extension Mask Value** 0 - comparison true forced. 1 - bit comparison enabled.

Note: The ID Mask is only used for reception.

No default value after reset.

Table 82. CANMSG Register

CANMSG (S:A3h)
CAN Message Data Register

7	6	5	4	3	2	1	0
MSG 7	MSG 6	MSG 5	MSG 4	MSG 3	MSG 2	MSG 1	MSG 0

Bit Number	Bit Mnemonic	Description
7-0	MSG7:0	**Message Data** This register contains the mailbox data byte pointed at the page message object register. After writing in the page message object register, this byte is equal to the specified message location (in the mailbox) of the pre-defined identifier + index. If auto-incrementation is used, at the end of the data register writing or reading cycle, the mailbox pointer is auto-incremented. The range of the counting is 8 with no end loop (0, 1,..., 7, 0,...)

No default value after reset.

Table 105. ADCLK Register

ADCLK (S:F2h)
ADC Clock Prescaler

7	6	5	4	3	2	1	0
-	-	-	PRS 4	PRS 3	PRS 2	PRS 1	PRS 0

Bit Number	Bit Mnemonic	Description
7-5	-	**Reserved** The value read from these bits are indeterminate. Do not set these bits.
4-0	PRS4:0	**Clock Prescaler** See Note (1)

Reset Value = XXX0 0000b

Note: 1. In X1 mode:

For PRS > 0 $F_{ADC} = \frac{FXTAL}{4xPRS}$

For PRS = 0 $F_{ADC} = \frac{FXTAL}{128}$

In X2 mode:

For PRS > 0 $F_{ADC} = \frac{FXTAL}{2xPRS}$

For PRS = 0 $F_{ADC} = \frac{FXTAL}{64}$

Table 106. ADDH Register

ADDH (S:F5h Read Only)
ADC Data High Byte Register

7	6	5	4	3	2	1	0
ADAT 9	ADAT 8	ADAT 7	ADAT 6	ADAT 5	ADAT 4	ADAT 3	ADAT 2

Bit Number	Bit Mnemonic	Description
7-0	ADAT9:2	**ADC result** bits 9-2

Reset Value = 00h

Table 107. ADDL Register

ADDL (S:F4h Read Only)
ADC Data Low Byte Register

7	6	5	4	3	2	1	0
-	-	-	-	-	-	ADAT 1	ADAT 0

Table 115. IPH1 Register

IPH1 (S:F7h)
Interrupt High Priority Register 1

7	6	5	4	3	2	1	0
-	-	-	-	SPIH	POVRH	PADCH	PCANH

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	SPIH	**SPI Interrupt Priority Level Most Significant bit** SPIH SPIL Priority level 0 0 Lowest 0 1 1 0 1 1 Highest
2	POVRH	**Timer overrun Interrupt Priority Level Most Significant bit** POVRH POVRL Priority level 0 0 Lowest 0 1 1 0 1 1 Highest
1	PADCH	**ADC Interrupt Priority Level Most Significant bit** PADCH PADCL Priority level 0 0 Lowest 0 1 1 0 1 1 Highest
0	PCANH	**CAN Interrupt Priority Level Most Significant bit** PCANH PCANL Priority level 0 0 Lowest 0 1 1 0 1 1 Highest

Reset Value = XXXX 0000b

External Program Memory Characteristics

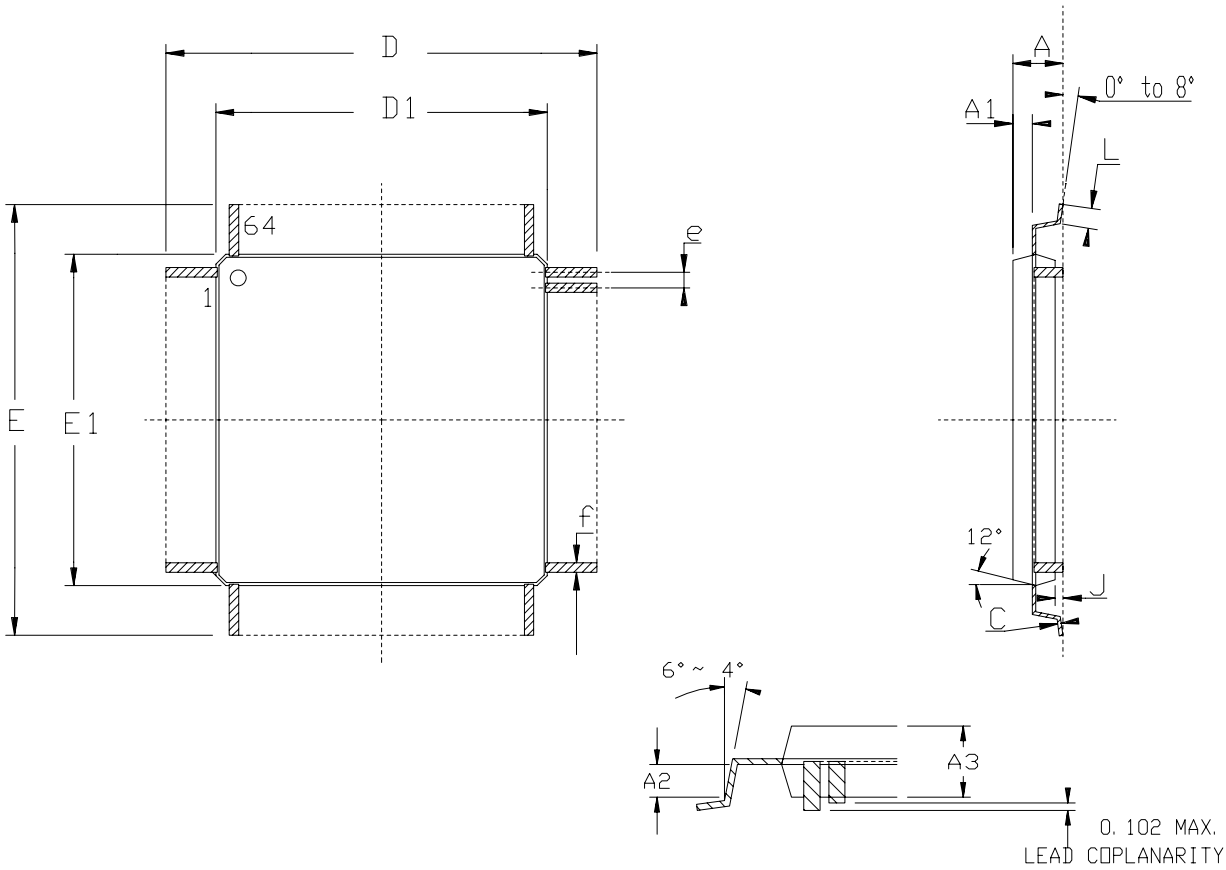
Table 118. Symbol Description

Symbol	Parameter
T	Oscillator clock period
T_{LHLL}	ALE pulse width
T_{AVLL}	Address Valid to ALE
T_{LLAX}	Address Hold After ALE
T_{LLIV}	ALE to Valid Instruction In
T_{LLPL}	ALE to $\overline{PSEN}$
T_{PLPH}	$\overline{PSEN}$ Pulse Width
T_{PLIV}	$\overline{PSEN}$ to Valid Instruction In
T_{PXIX}	Input Instruction Hold After $\overline{PSEN}$
T_{PXIZ}	Input Instruction Float After $\overline{PSEN}$
T_{AVIV}	Address to Valid Instruction In
T_{PLAZ}	$\overline{PSEN}$ Low to Address Float

Table 119. AC Parameters for a Fix Clock (F = 40 MHz)

Symbol	Min	Max	Units
T	25		ns
T_{LHLL}	40		ns
T_{AVLL}	10		ns
T_{LLAX}	10		ns
T_{LLIV}		70	ns
T_{LLPL}	15		ns
T_{PLPH}	55		ns
T_{PLIV}		35	ns
T_{PXIX}	0		ns
T_{PXIZ}		18	ns
T_{AVIV}		85	ns
T_{PLAZ}		10	ns

VQFP64



	MM		INCH	
	Min	Max	Min	Max
A	–	1.60	–	.063
A1	0.64 REF		.025 REF	
A2	0.64 REF		.025 REF	
A3	1.35	1.45	.053	.057
D	11.75	12.25	.463	.483
D1	9.90	10.10	.390	.398
E	11.75	12.25	.463	.483
E1	9.90	10.10	.390	.398
J	0.05	–	.002	–
L	0.45	0.75	.018	.030
e	0.50 BSC		.0197 BSC	
f	0.25 BSC		.010 BSC	

Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Europe
Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards
Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive
Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/
High Speed Converters/RF Datacom
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-30-00
Fax: (33) 4-76-58-34-80

Literature Requests
www.atmel.com/literature

Printed on recycled paper.

4182O–CAN–09/08