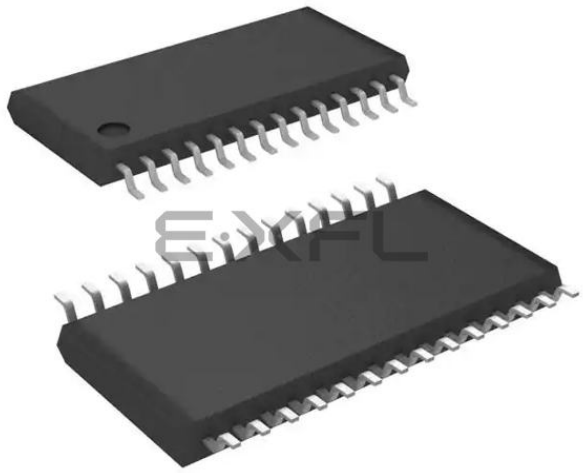

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Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	28-TSSOP
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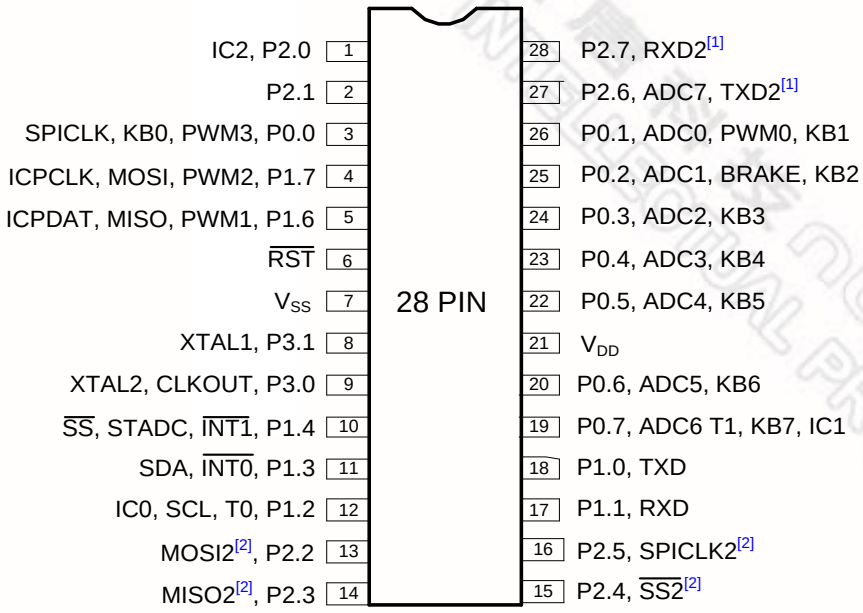
5 Pin Configuration



[1] These pins are switched from RXD2 and TXD2 by S/W setting

[2] These pins are switched from MOSI2, MISO2, /SS2 and SPICLK2 by S/W setting.

Figure 5–1 TSSOP/SOP 28-pin Assignment

Table 5–1 Pin Description

Pin No.	Symbol	Alternate Function				Type	Description
SOP28 TSSOP28		1	2	3			
14	P2.3				MISO2	I/O	The SPI-2 ports are by software switched from SPI-1 port. ADC7: ADC channel input. IC2: Input Capture pin
15	P2.4				/SS2	I/O	
16	P2.5				SPICLK2	I/O	
27	P2.6	TXD2	ADC7			I/O	
28	P2.7	RXD2				I/O	
9	P3.0	XTAL2	CLKOUT			I/O	**PORT3:** Port 3 has 4-type I/O port. Its multifunction pins are for XTAL1, XTAL2 and CLKOUT, **CLKOUT:** Internal RC OSC/4 output pin. **XTAL2:** This is the output pin from the internal inverting amplifier. It emits the inverted signal of XTAL2. **XTAL1:** This is the output pin from the internal inverting amplifier. It emits the inverted signal of XTAL1.
8	P3.1	XTAL1				I/O	

[1] I/O type description – I: input, O: output, I/O: quasi bi-direction, D: open-drain, P: power pins, ST: Schmitt trigger.

6.5 On-chip XRAM

The N79E855/854 provides additional on-chip 256 bytes auxiliary RAM called XRAM to enlarge the RAM space. It occupies the address space from 00H through FFH. The 256 bytes of XRAM are indirectly accessed by move external instruction MOVX @DPTR or MOVX @Ri. (See the demo code below.) Note that the stack pointer may not be located in any part of XRAM. Figure 6-1 shows the memory map for this product series.

XRAM demo code:

```
MOV    R0,#23H              ;write #5AH to XRAM with address @23H
MOV    A,#5AH
MOVX   @R0,A

MOV    R1,#23H             ;read from XRAM with address @23H
MOVX   A,@R1

MOV    DPTR,#0023H         ;write #5BH to XRAM with address @0023H
MOV    A,#5BH
MOVX   @DPTR,A

MOV    DPTR,#0023H         ;read from XRAM with address @0023H
MOVX   A,@DPTR
```

6.6 On-chip scratch-pad RAM and SFR

The N79E855/854 provides the on-chip 256 bytes scratch pad RAM and Special Function Registers (SFRs) which be accessed by software. The SFRs be accessed only by direct addressing, while the on-chip RAM be accessed by either direct or indirect addressing.

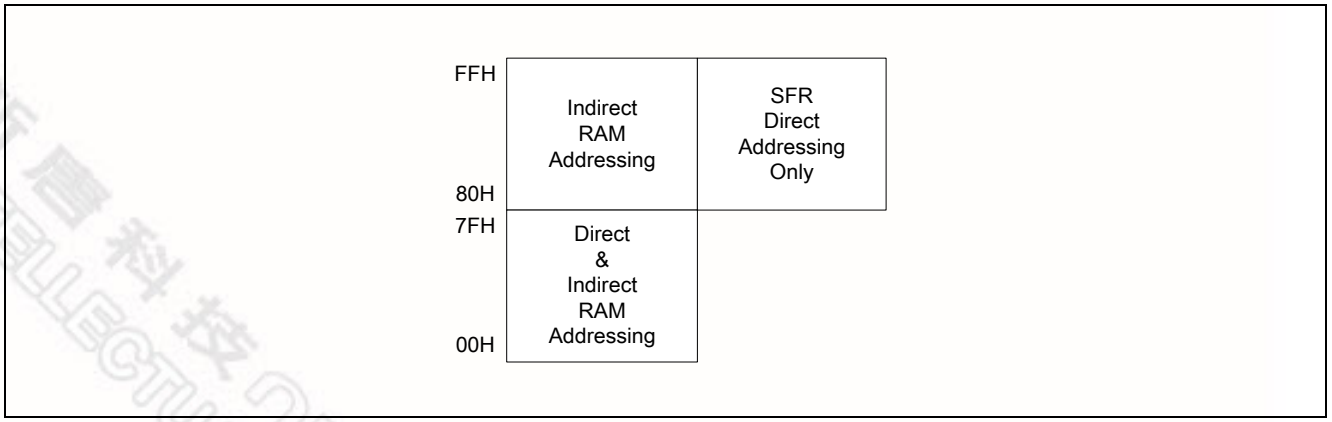


Figure 6-3 256 bytes RAM and SFR

Since the scratch-pad RAM is only 256 byte it can be used only when data contents are small. There are several other special purpose areas within the scratch-pad RAM, which are described as follows.

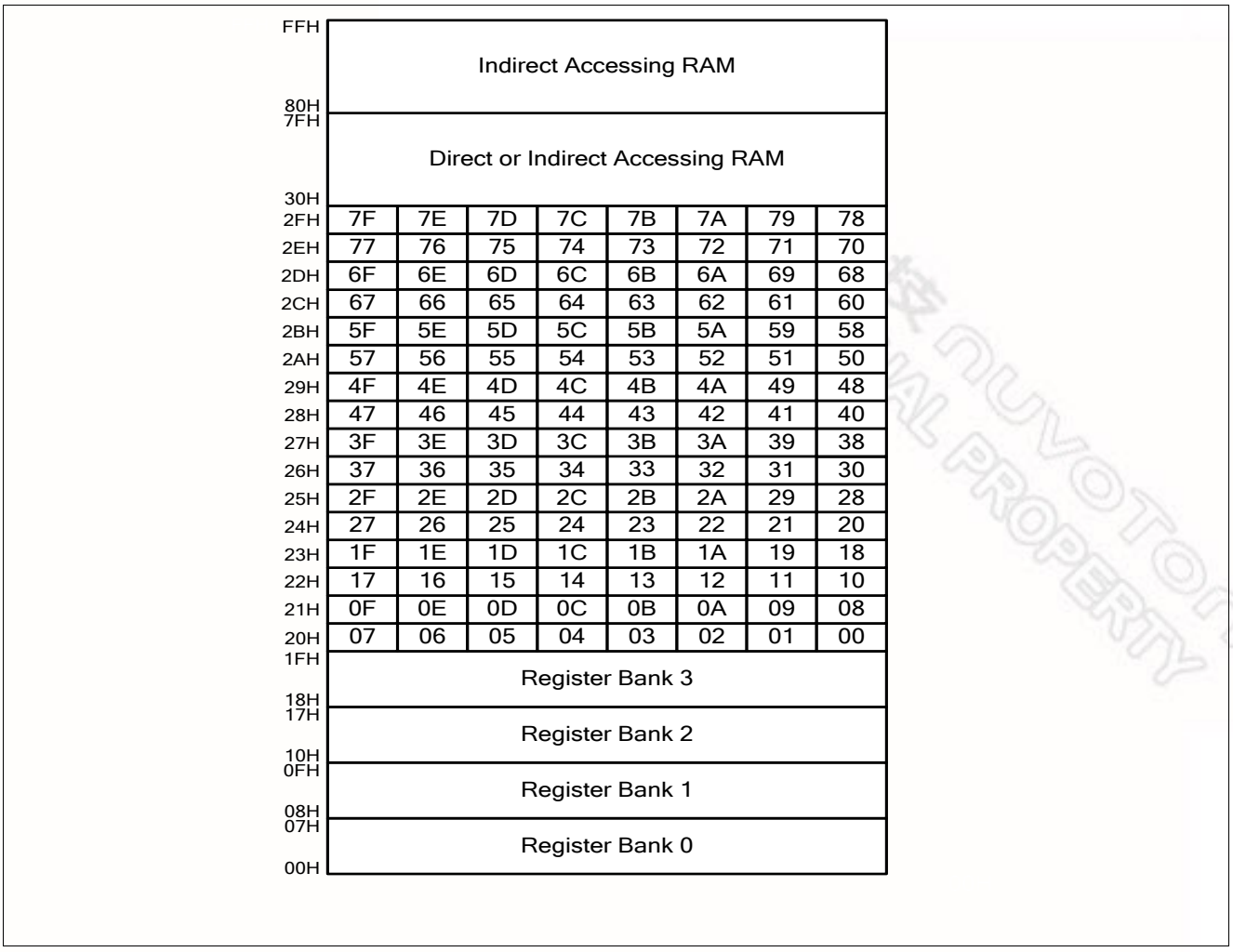


Figure 6-4 Data Memory and Bit-addressable Region

6.7 Working Registers

There are four sets of working registers, each consisting of eight 8-bit registers, which are termed as Banks 0, 1, 2, and 3. Individual registers within these banks can be directly accessed by separate instructions. These individual registers are named as R0, R1, R2, R3, R4, R5, R6 and R7. However, at one time the N79E855/854 can work with only one particular bank. The bank selection is done by setting RS1-RS0 bits in the PSW. The R0 and R1 registers are used to store the address for indirect accessing.

6.8 Bit-addressable Locations

The Scratch-pad RAM area from location 20h to 2Fh is byte as well as bit-addressable. This means that a bit in this area can be individually addressed. In addition, some of the SFRs are also bit-addressable. The instruction decoder is able to distinguish a bit access from a byte access by the type of the instruction itself. In the SFR area, any existing SFR whose address ends in a 0 or 8 is bit-addressable.

Instruction	CY	OV	AC	Instruction	CY	OV	AC
RLC A	X			CJNE	X		
SETB C	1						

[1] X indicates the modification is dependent on the result of the instruction

PCON – Power Control

7	6	5	4	3	2	1	0
SMOD	SMOD0	-	POF	GF1	GF0	PD	IDL
R/W	R/W	-	R/W	R/W	R/W	R/W	R/W

Address: 87H Reset value: see Table 7–2 N79E855/854 SFR Description and Reset Values

Bit	Name	Description
3	GF1	**General Purpose Flag 1** The general purpose flag that can be set or cleared by the user.
2	GF0	**General Purpose Flag 0** The general purpose flag that can be set or cleared by the user.

General 80C51 support one DPTR but the N79E855/854 support two DPTRs by switching AUXR1.DPS. The setting is as follows.

AUXR1 – AUX Function Resgister-1

7	6	5	4	3	2	1	0
SPI_Sel	UART_Sel	-	-	DisP26	-	0	DPS
R/W	R/W	-	-	R/W	-	R	R/W

Address: A2H Reset value: 0000 0000B

Bit	Name	Description
0	DPS	**Dual Data Pointer Selection** 0 = Select DPTR of standard 8051. 1 = Select DPTR1

TH0 – Timer 0 High Byte

7	6	5	4	3	2	1	0
TH0[7:0]							
R/W							

Address: 8CH Reset value: 0000 0000B

Bit	Name	Description
7:0	TH0[7:0]	**Timer 0 High Byte** The TH0 register is the high byte of the 16-bit Timer 0.

TL1 – Timer 1 Low Byte

7	6	5	4	3	2	1	0
TL1[7:0]							
R/W							

Address: 8BH Reset value: 0000 0000B

Bit	Name	Description
7:0	TL1[7:0]	**Timer 1 Low Byte** The TL1 register is the low byte of the 16-bit Timer 1.

TH1 – Timer 1 High Byte

7	6	5	4	3	2	1	0
TH1[7:0]							
R/W							

Address: 8DH Reset value: 0000 0000B

Bit	Name	Description
7:0	TH1[7:0]	**Timer 1 High Byte** The TH1 register is the high byte of the 16-bit Timer 1.

P3M1 – Port3 Output Mode1

7	6	5	4	3	2	1	0
P3S	P2S	P1S	P0S	T1OE	T0OE	P3M1.1	P3M1.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 96H Reset value: 0000 0000B

Bit	Name	Description
3	T1OE	P0.7 pin is toggled whenever Timer 1 overflows. The output frequency is therefore one half of the Timer 1 overflow rate.
2	T0OE	P1.2 pin is toggled whenever Timer 0 overflows. The output frequency is therefore one-half of the Timer 0 overflow rate.

10.1.1 Mode 0 (13-bit Timer)

In Mode 0, the timers/counters act as a 8-bit counter with a 5-bit, divide by 32 pre-scale. In this mode we have a 13-bit timer/counter. The 13-bit counter consists of 8 bits of THx and 5 lower bits of TLx. The upper 3 bits of TLx are ignored.

The negative edge of the clock is increments count in the TLx register. When the fifth bit in TLx moves from 1 to 0, then the count in the THx register is incremented. When the count in THx moves from FFh to 00h, then the overflow flag TFx in TCON SFR is set. The counted input is enabled only if TRx is set and either GATE = 0 or $\overline{INTx}$ = 1. When $C/\overline{T}$ is set to 0, then it will count clock cycles, and if $C/\overline{T}$ is set to 1, then it will count 1 to 0 transitions on T0 (P1.2) for timer 0 and T1 (P0.7) for timer 1. When the 13-bit count reaches 1FFFh, the next count will cause it to rollover to 0000h. The timer overflow flag TFx of the relevant timer is set and if enabled an interrupts will occur.

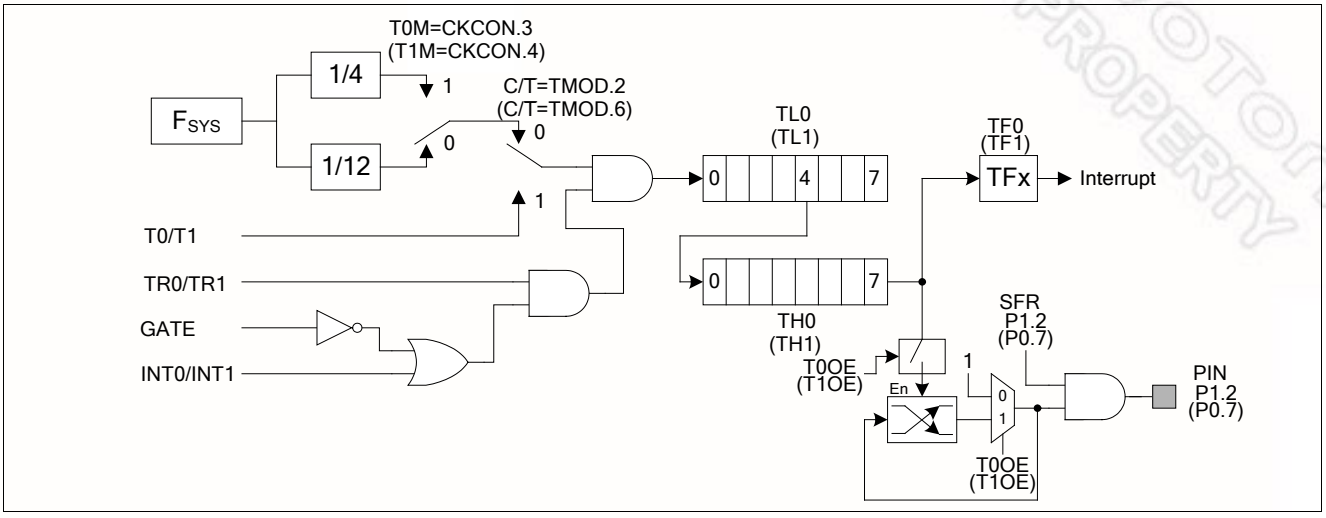


Figure 10–1 Timers/Counters 0 and 1 in Mode 0

10.1.2 Mode 1 (16-bit Timer)

Mode 1 is similar to Mode 0 except that the counting registers are fully used as a 16-bit counter. Rollover occurs when a count moves FFFFH to 0000H. The Timer overflow flag TFx of the relevant Timer/Counter is set and an interrupt will occurs if enabled.

(TMOD.2). TH0 is forced as a clock cycle counter (clock/12 or clock/4) and takes over the use of TR1 and TF1 from Timer/Counter 1. Mode 3 is used in cases where an extra 8 bit timer is needed. With Timer 0 in Mode 3, Timer 1 can still be used in Modes 0, 1 and 2, but its flexibility is somewhat limited. While its basic functionality is maintained, it no longer has control over its overflow flag TF1 and the enable bit TR1. Timer 1 can still be used as a timer/counter and retains the use of GATE and INT1 pin. In this condition it can be turned on and off by switching it out of and into its own Mode 3. It can also be used as a baud rate generator for the serial port.

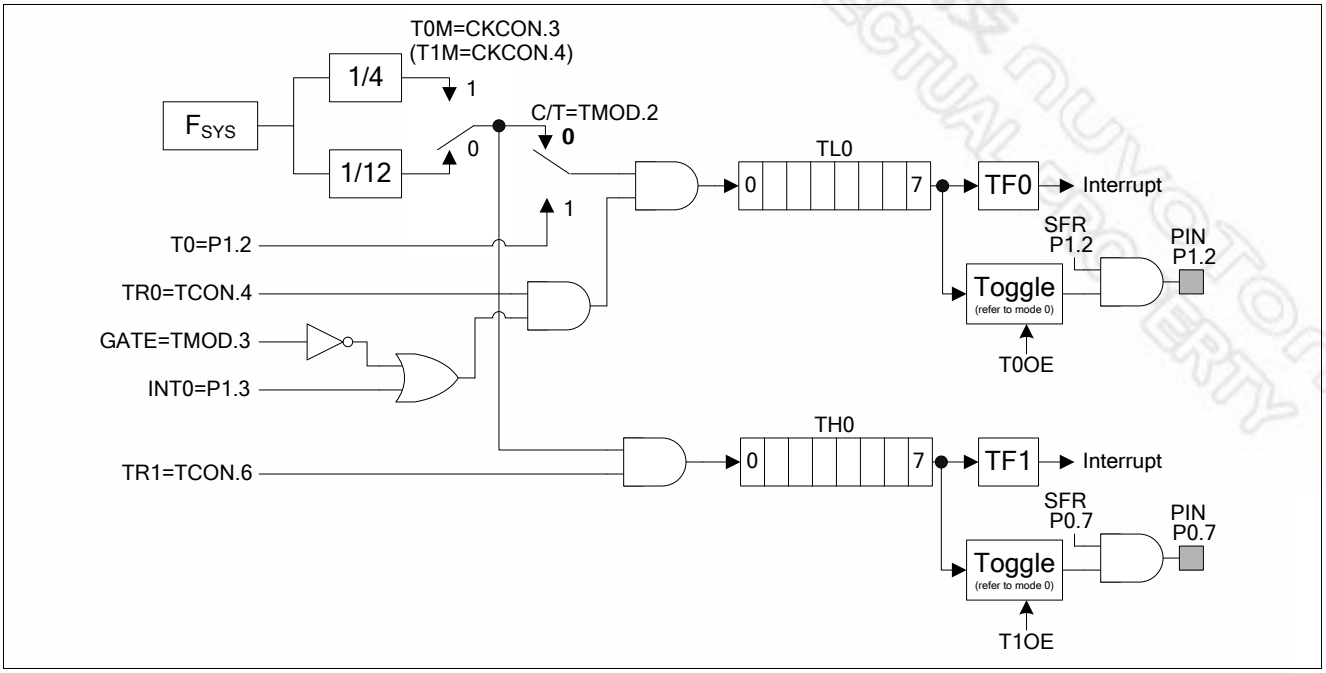


Figure 10–4 Timer/Counter 0 in Mode 3

Bit	Name	Description
6:4	T2DIV[2:0]	**Timer 2 Clock Divider** 000 = Timer 2 clock divider is 1/4. 001 = Timer 2 clock divider is 1/8. 010 = Timer 2 clock divider is 1/16. 011 = Timer 2 clock divider is 1/32. 100 = Timer 2 clock divider is 1/64. 101 = Timer 2 clock divider is 1/128. 110 = Timer 2 clock divider is 1/256. 111 = Timer 2 clock divider is 1/512.
3	CAPCR	**Capture Auto-clear** This bit enables auto-clear Timer 2 value in TH2 and TL2 when a determined input capture event occurs. 0 = Timer 2 continues counting when a capture event occurs. 1 = Timer 2 value is auto-cleared as 0000H when a capture event occurs.
2	COMPCR	**Compare Match Auto-clear** This bit enables auto-clear Timer 2 value in TH2 and TL2 when a compare match occurs. 0 = Timer 2 continues counting when a compare match occurs. 1 = Timer 2 value is auto-cleared as 0000H when a compare match occurs.
1:0	LDTS[1:0]	**Auto-reload Trigger Selection** These bits select the reload trigger event. 00 = Reload when Timer 2 overflows. 01 = Reload when input capture 0 event occurs. 10 = Reload when input capture 1 event occurs. 11 = Reload when input capture 2 event occurs.

RCOMP2L – Timer 2 Reload/Compare Low Byte

7	6	5	4	3	2	1	0
RCOMP2L[7:0]							
R/W							

Address: CAH Reset value: 0000 0000B

Bit	Name	Description
7:0	RCOMP2L[7:0]	**Timer 2 Reload/Compare Low Byte** This register stores the low byte of compare value when Timer 2 is configured in compare mode, It holds the low byte of the reload value when auto-reload mode.

RCOMP2H – Timer 2 Reload/Compare High Byte

7	6	5	4	3	2	1	0
RCOMP2H[7:0]							
R/W							

Address: CBH Reset value: 0000 0000B

Bit	Name	Description
7:0	RCOMP2H[7:0]	**Timer 2 Reload/Compare High Byte** This register stores the high byte of compare value when Timer 2 is configured in compare mode. And it holds the high byte of the reload value when auto-reload mode.

13 Serial Peripheral Interface (SPI)

13.1 Features

The N79E855/854 exists a Serial Peripheral Interface (SPI) block to support high-speed serial communication. SPI is a full-duplex, high-speed, synchronous communication bus between MCUs or other peripheral devices such as serial EEPROM, LCD driver, or D/A converter. It provides either Master or Slave mode, high-speed rate up to F_{SYS}/16 for Master mode and F_{SYS}/4 for Slave mode, transfer complete and write collision flag. For a multi-master system, SPI supports Master Mode Fault to protect a multi-master conflict.

13.2 Functional Description

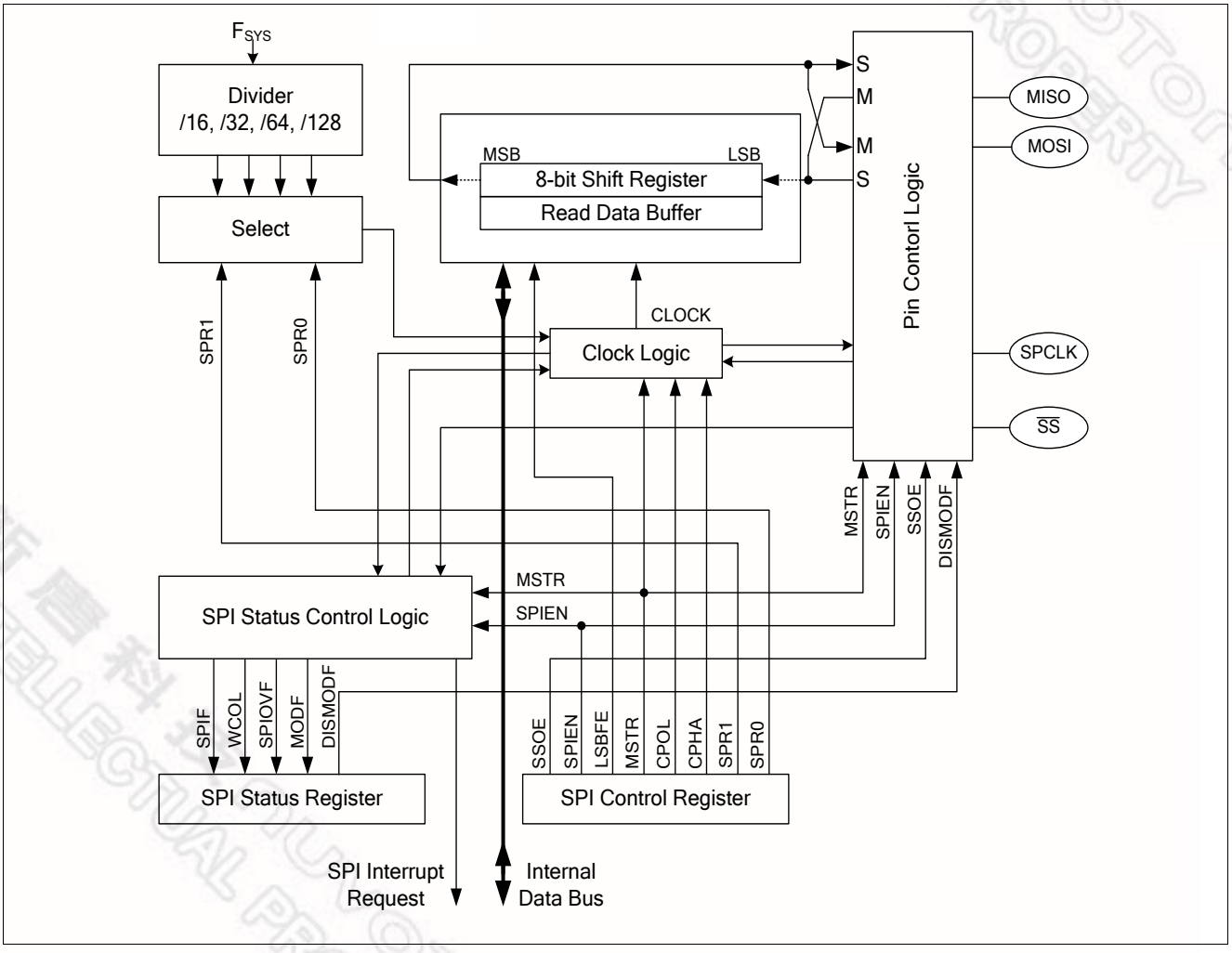


Figure 13–1 SPI Block Diagram

Figure 13–1 shows SPI block diagram and provides an overview of SPI architecture in this device. The main blocks of SPI are the SPI control register logic, SPI status logic, clock rate control logic, and pin control logic. For a serial data transfer

Bit	Name	Description
1:0	PWMPH	PWM Counter Bits Register bit[9:8]

The user should follow the initialization steps below to start generating the PWM signal output. In the first step by setting CLRPWM (PWMCON0.4), it ensures the 10-bit down counter a determined value. After setting all period and duty registers, PWMRUN (PWMCON0.7) can be set as logic 1 to trigger the 10-bit down counter running. In the beginning the PWM output remains high until the counter value is less than the value in duty control registers of PWMnH and PWMnL. At this point the PWM output goes low until the next underflow. When the 10-bit down counter underflows, PWMP buffer register will be reloaded in 10-bit down counter. It continues PWM signal output by repeating this routine.

The hardware for all period and duty control registers is double buffered designed. Therefore the PWMP and PWMn registers can be written to at any time, but the period and duty cycle of PWM will not updated immediately until the Load (PWMCON0.6) is set and previous period is complete. This allows updating the PWM period and duty glitch less operation.

PWM0L – PWM 0 Low Register

7	6	5	4	3	2	1	0
PWM0.7	PWM0.6	PWM0.5	PWM0.4	PWM0.3	PWM0.2	PWM0.1	PWM0.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: DAH Reset value: 0000 0000B

Bit	Name	Description
7:0	PWM0L	PWM 0 Low Bits Register bit[7:0].

PWM0H – PWM 0 High Register

7	6	5	4	3	2	1	0
-	-	-	-	-	-	PWM0.9	PWM0.8
-	-	-	-	-	-	R/W	R/W

Address: D2H Reset value: 0000 0000B

Bit	Name	Description
7:2	-	**Reserved**
1:0	PWM0H	PWM 0 High Bits Register bit[9:8].

PWM1L – PWM 1 Low Register

7	6	5	4	3	2	1	0
PWM1.7	PWM1.6	PWM1.5	PWM1.4	PWM1.3	PWM1.2	PWM1.1	PWM1.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: DBH Reset value: 0000 0000B

Bit	Name	Description
7:0	PWM1L	PWM 0 Low Bits Register bit[7:0].

19 Interrupt System

The N79E855/854 has four priority level of interrupts structure with 14 interrupt sources. Each of the interrupt sources has an individual priority bit, flag, interrupt vector and enable bit. In addition, the interrupts can be globally enabled or disabled.

19.1 Interrupt Sources

The External Interrupts $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ can be either edge triggered or level triggered, depending on bits IT0 and IT1. The bits IE0 and IE1 in the TCON register are the flags which are checked to generate the interrupt. In the edge triggered mode, the INTx inputs are sampled in every machine-cycle. If the sample is high in one cycle and low in the next, then a high to low transition is detected and the interrupts request flag IEx in TCON is set. The flag bit requests the interrupt. Since the external interrupts are sampled every machine-cycle, they have to be held high or low for at least one complete machine-cycle. The IEx flag is automatically cleared when the service routine is called. If the level triggered mode is selected, then the requesting source has to hold the pin low till the interrupt is serviced. The IEx flag will not be cleared by the hardware on entering the service routine. If the interrupt continues to be held low even after the service routine is completed, then the processor may acknowledge another interrupt request from the same source.

The Timer 0 and 1 Interrupts are generated by the TF0 and TF1 flags. These flags are set by the overflow in the Timer 0 and Timer 1. The TF0 and TF1 flags are automatically cleared by the hardware when the timer interrupt is serviced.

The Watchdog timer can be used as a system monitor or a simple timer. In either case, when the timeout count is reached, the Watchdog Timer interrupt flag WDTRF (WDCON0.3) is set. If the interrupt is enabled by the enable bit EIE.4, then an interrupt will occur.

The Serial block can generate interrupt on reception or transmission. There are two interrupt sources from the Serial block, which are obtained by the RI and TI bits in the SCON SFR. These bits are not automatically cleared by the hardware, and the user will have to clear these bits using software.

I^2C will generate an interrupt due to a new SIO state present in I2STA register, if both EA and ES bits (in IE register) are both enabled.

SPI asserts interrupt flag, SPIF, upon completion of data transfer with an external device. If SPI interrupt is enabled (ESPI at EIE.6), a serial peripheral interrupt is generated. SPIF flag is software clear, by writing 0. MODF and SPIOVF will also generate interrupt if occur. They share the same vector address as SPIF.

The ADC can generate interrupt after finished ADC converter. There is one interrupt source, which is obtained by the ADCI bit in the ADCCON0 SFR. This bit is not automatically cleared by the hardware, and the user will have to clear this bit using software.

PWM brake interrupt flag BKF is generated if P0.2 (Brake pin) detects a high (BKPS=1) or low (BKPS=0) at port pin. At this moment, BKF (PWMCON2.0) is set by hardware and it should be cleared by software. PWM period interrupt flag CF is set by hardware when its' 10-bit down counter underflow and is only cleared by software. BKF is set the PWM interrupt is requested If PWM interrupt is enabled (EPWM=1).

other interrupt source. So, if two requests of different priority levels are received simultaneously, the request of higher priority level is serviced.

If requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. This is called the arbitration ranking. Note that the arbitration ranking is only used to resolve simultaneous requests of the same priority level.

The following table summarizes the interrupt sources, flag bits, vector addresses, enable bits, priority bits, arbitration ranking, and whether each interrupt may wake up the CPU from Power-down mode.

Table 19-3 Summary of interrupt sources

Description	Interrupt Flag Bit(s)	Vector Address	Interrupt Enable Bit(s)	Flag cleared by	Interrupt Priority	Arbitration Ranking	Power-down Wake-up
External Interrupt 0	IE0	0003H	EX0 (IE0.0)	Hardware, Software	IPH.0, IP.0	1 (highest)	Yes
BOD Detect	BOF	0043H	EBOD (IE.5)	Software	IPH.5, IP.5	2	Yes
Watchdog Timer	WDTF	0053H	EWDI (EIE.4)	Software	EIPH.4, EIP.4	3	Yes
Timer 0 Interrupt	TF0	000BH	ET0 (IE.1)	Hardware, Software	IPH.1, IP.1	4	No
I^2C Interrupt	SI I2TOF	0033H	EI2C (EIE.0)	Software	EIPH.0, EIP.0	5	No
ADC Converter	ADCI	005BH	EADC (IE.6)	Software	IPH.6, IP.6	6	Yes[1]
External Interrupt 1	IE1	0013H	EX1 (IE.2)	Hardware, Software	IPH.2, IP.2	7	Yes
KBI Interrupt	KBIF[7:0]	003BH	EKB (EIE.1)	Software	EIPH.1, EIP.1	8	Yes
Timer 1 Interrupt	TF1	001BH	ET1 (IE.3)	Hardware, Software	IPH.3, IP.3	9	No
Serial Port Tx and Rx	TI & RI	0023H	ES (IE.4)	Software	IPH.4, IP.4	10	No
PWM Interrupt	BKF	0073H	EPWM (EIE.5)	Software	EIPH.5, EIP.5	11	No
SPI	SPIF + MODF + SPIOVF	004BH	ESPI (EIE.6)	Software	EIPH.6, EIP.6	12	No
Timer 2 Overflow/Match	TF2	002Bh	ET2 (EIE.7)	Software	EIPH.7, EIP.7	13	No
Capture	CAPF0-2	0063H	ECPTF (EIE.2)	Software	IPH.7, IP.7	14 (lowest)	No

[1] The ADC Converter can wake up “Power-down mode” when its clock source is from internal RC.

19.3 Interrupt Response Time

The response time for each interrupt source depends on several factors, such as the nature of the interrupt and the instruction underway. In the case of external interrupts $\overline{\text{INT0}}$ to RI+TI, they are sampled at C3 of every machine-cycle and then their corresponding interrupt flags IEx will be set or reset. The Timer 0 and 1 overflow flags are set at C3 of the machine-cycle in which overflow has occurred. These flag values are polled only in the next machine-cycle. If a request is active and all three conditions are met, then the hardware generated LCALL is executed. This LCALL itself takes four machine-cycles to be completed. Thus there is a minimum time of five machine-cycles between the interrupt flag being set and the interrupt service routine being executed.

A longer response time should be anticipated if any of the three conditions are not met. If a higher or equal priority is being serviced, the interrupt latency time is obviously dependent on the nature of the service routine currently being executed. If the polling cycle is not the last machine-cycle of the instruction being executed, an additional delay is introduced. The maximum response time (if no other interrupt is in service) occurs if the N79E855/854 performs a write to IE, EIE, IP, IPH, EIP or EIPH and then executes a MUL or DIV instruction. From the time an interrupt source is activated, the longest reaction time is 12 machine-cycles. This includes 1 machine-cycle to detect the interrupt, 3 machine-cycles to complete the IE, EIE, IP, IPH, EIP or EIPH access, 5 machine-cycles to complete the MUL or DIV instruction and 4 machine-cycles to complete the hardware LCALL to the interrupt vector location.

Thus in a single-interrupt system the interrupt response time will always be more than 5 machine-cycles and not more than 12 machine-cycles. The maximum latency of 12 machine-cycle is 48 clock cycles. Note that in the standard 8051 the maximum latency is 8 machine-cycles which equals 96 machine-cycles. This is a 50% reduction in terms of clock periods.

19.4 SFR of Interrupt

The SFRs associated with these interrupts are listed below.

IE – Interrupt Enable (Bit-addressable)

7	6	5	4	3	2	1	0
EA	EADC	EBOD	ES	ET1	EX1	ET0	EX0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: A8H Reset value: 0000 0000B

Bit	Name	Description
7	EA	**Enable All Interrupt** This bit globally enables/disables all interrupts. It overrides the individual interrupt mask settings. 0 = Disable all interrupt sources. 1 = Enable each interrupt depending on its individual mask setting. Individual interrupts will occur if enabled.

Bit	Name	Description
		0 = Enable ISP function. 1 = Disable ISP function. To enable ISP function will start the internal 22.1184 MHz RC oscillator for timing control. To clear ISPEN should always be the last instruction after ISP operation to stop internal RC for reducing power consumption.

ISPCN – ISP Control

7	6	5	4	3	2	1	0
ISPA17	ISPA16	FOEN	FCEN	FCTRL.3	FCTRL.2	FCTRL.1	FCTRL.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: AFH Reset value: 0011 0000B

Bit	Name	Description
7:6	ISPA[17:16]	**ISP Control** This byte is for ISP controlling command to decide ISP destinations and actions.
5	FOEN	
4	FCEN	
3:0	FCTRL[3:0]	

ISPAH – ISP Address High Byte

7	6	5	4	3	2	1	0
ISPA[15:8]							
R/W							

Address: A7H Reset value: 0000 0000B

Bit	Name	Description
7:0	ISPA[15:8]	**ISP Address High Byte** ISPAH contains address ISPA[15:8] for ISP operations.

ISPAL – ISP Address Low Byte

7	6	5	4	3	2	1	0
ISPA[7:0]							
R/W							

Address: A6H Reset value: 0000 0000B

Bit	Name	Description
7:0	ISPA[7:0]	**ISP Address Low Byte** ISPAL contains address ISPA[7:0] for ISP operations.

```
MOV    ISPCN,#00001100b    ;select “Read Device ID” mode
MOV    ISPAH,#00H          ;fill address with 0000H for low-byte DID
MOV    ISPAL,#00H          ;
CALL   Trigger_ISP
MOV    A,ISPFD             ;now, ISPFD contains low-byte DID, move to ACC for further use
MOV    ISPAH,#00H          ;fill address with 0001H for high-byte DID
MOV    ISPAL,#01H          ;
CALL   Trigger_ISP
MOV    A,ISPFD             ;now, ISPFD contains high-byte DID, move to ACC for further use
CALL   Disable_ISP
```

FLASH Page Erase (target address in APROM/Data Flash/LDROM area)

```
CALL   Enable_ISP
MOV    ISPCN,#00100010b    ;select “FLASH Page Erase” mode, (A17,A16)=(0,0) for APROM/Data
                           ;Flash/LDROM
MOV    ISPAH,#??H          ;fill page address
MOV    ISPAL,#??H
CALL   Trigger_ISP
CALL   Disable_ISP
```

FLASH Program (target address in APROM/Data Flash/LDROM area)

```
CALL   Enable_ISP
MOV    ISPCN,#00100001b    ;select “FLASH Program” mode, (A17,A16)=(0,0) for APROM/Data
                           ;Flash/LDROM
MOV    ISPAH,#??H          ;fill byte address
MOV    ISPAL,#??H
MOV    ISPFD,#??H          ;fill data to be programmed
CALL   Trigger_ISP
CALL   Disable_ISP
```

FLASH Read (target address in APROM/Data Flash/LDROM area)

```
CALL   Enable_ISP
MOV    ISPCN,#00000000b    ;select “FLASH Read” mode, (A17,A16)=(0,0) for APROM/Data
                           ;Flash/LDROM
MOV    ISPAH,#??H          ;fill byte address
MOV    ISPAL,#??H
CALL   Trigger_ISP
MOV    A,ISPFD             ;now, ISPFD contains the Flash data, move to ACC for further use
CALL   Disable_ISP
```

CONFIG Page Erase (target address in CONFIG area)

```
CALL   Enable_ISP
MOV    ISPCN,#11100010b    ;select “CONFIG Page Erase” mode, (A17,A16)=(1,1) for CONFIG
MOV    ISPAH,#00H          ;fill page address #0000H, because there is only one page
MOV    ISPAL,#00H
CALL   Trigger_ISP
CALL   Disable_ISP
```

CONFIG Program (target address in CONFIG area)

```
CALL   Enable_ISP
MOV    ISPCN,#11100001b    ;select “CONFIG Program” mode, (A17,A16)=(1,1) for CONFIG
MOV    ISPAH,#00H          ;fill byte address, 0000H/0001H/0002H/0003H for CONFIG0/1/2/3,
                           ;respectively
```

logical states they had at the time Idle was activated. Generally it saves considerable power of typical half of the full operating power.

Since the clock provided for peripheral function logic circuit like timer or serial port still remain in Idle mode, the CPU can be released from the Idle mode using any of the interrupt sources if enabled. The user can put the device into Idle mode by writing 1 to the bit IDL (PCON.0). The instruction that sets the IDL bit is the last instruction that will be executed before the device goes into Idle mode.

The Idle mode can be terminated in two ways. First, any interrupt if enabled will cause an exit. This will automatically clear the IDL bit, terminate the Idle mode, and the interrupt service routine (ISR) will be executed. After using the RETI instruction to jump out of the ISR, execution of the program will be the one following the instruction which put the CPU into Idle mode. The second way to terminate the Idle mode is with any reset other than software reset.

21.2 Power-down Mode

Power-down mode is the lowest power state that N79E855/854 can enter. It remain the power consumption as a ”μA” level. This is achieved by stopping the clock system no matter internal RC clock or external crystal. Both of CPU and peripheral functions like Timers or UART are frozen. Flash memory stops. All activity is completely stopped and the power consumption is reduced to the lowest possible value. The device can be put into Power-down mode by writing 1 to bit PD (PCON.1). The instruction that does this action will be the last instruction to be executed before the device goes into Power-down mode. In Power-down mode, RAM maintains its content. The port pins output the values held by their respective.

There are two ways to exit N79E855/854 from Power-down mode. The first is with all resets except software reset. BOD reset will also wake up CPU from Power-down mode. Make sure that BOD detection is enabled before the system enters into Power-down. However, for a principle of least power consumption, it is uncommon to enable BOD detection in Power-down mode, which is not a recommended application. Of course, the RST pin reset and power-on reset will remove the Power Down status. After RST pin reset or power-on reset, the CPU is initialized and starts executing program code from the beginning.

The N79E855/854 can be woken up from Power-down mode by forcing an external interrupt pin activated, providing the corresponding interrupt enabled and the global enable EA bit (IE.7) is set. If these conditions are met, the trigger on the external pin will asynchronously restart the clock system. Then device executes the interrupt service routine (ISR) for the corresponding external interrupt. After the ISR is completed, the program execution returns to the instruction after the one that puts the device into Power-down mode and continues.

BOD, Watchdog and KBI interrupt are other sources to wake up CPU from Power Down. As mentioned before the user will endure the current of BOD detection circuit. Using KBI interrupt to wake up CPU from Power Down has a

Maximum total I_{OL}/I_{OH} for all outputs: 100mA (Through V_{DD} total current)
Maximum total I_{OL}/I_{OH} for all outputs: 150mA (Through V_{SS} total current)

[4] If I_{OH} exceeds the test condition, V_{OH} will be lower than the listed specification.
If I_{OL} exceeds the test condition, V_{OL} will be higher than the listed specification.

[5] Tested while CPU is kept in reset state.

[6] general purpose I/O mean the general purpose I/O, such as P0, P1, P2, P3.

[7] These parameters are characterized but not tested.

Other: P1.2 and P1.3 are open drain structure. They have not quasi or push pull modes.

28.3 AC Electrical Characteristics

28.3.1 Specification of 10-bits SAR-ADC

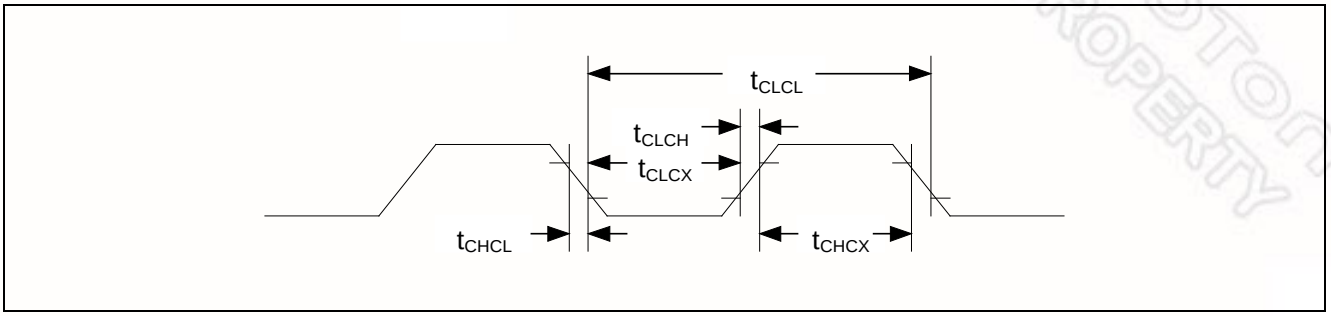
	Symbol	MIN	TYP	MAX	Unit
Operation voltage	V_{DD}	2.7		5.5	V
Resolution				10	bit
Conversion time			$35t_{ADC}$[1]		us
Sampling rate				150K	Hz
Integral Non-Linearity Error	INL	-1		1	LSB
Differential Non-Linearity	DNL	-1		1	LSB
Gain error	Ge	-1		1	LSB
Offset error	Ofe	-4		4	LSB
Clock frequency	ADCCLK			5.25	MHz
Absolute error		-4		4	LSB
Band-gap	V_{BG}	1	1.3	1.6	V

[1] t_{ADC} The period time of ADC input clock

28.3.2 4 ~ 24 MHz XTAL Specifications

Parameter	Condition	MIN.	TYP.	MAX.	Unit
Input clock frequency	External crystal	4		24	MHz

Parameter	Symbol	MIN.	TYP.	MAX.	Units	Notes
External crystal Frequency	$1/t_{CLCL}$	4		24	MHz	
Clock High Time	t_{CHCX}	20.8	-	-	nS	
Clock Low Time	t_{CLCX}	20.8	-	-	nS	
Clock Rise Time	t_{CLCH}	-	-	10	nS	
Clock Fall Time	t_{CHCL}	-	-	10	nS	



Note: Duty cycle is 50%.

28.3.3 Internal RC Oscillator Specifications – 22.1184 MHz/11.0592 MHz

Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Center Frequency			22.1184/11.0592		MHz
Internal Oscillator Frequency	$+25^0C$ at V_{DD} = 5V	-1		+1	%
	$+25^0C$ at V_{DD} = 2.7~5.5V	-3		+3	%
	-10^0C~$+70^0C$ at V_{DD} = 2.7~5.5V	-5		+5	%
	-40^0C~$+85^0C$ at V_{DD} = 2.7~5.5V	-8		+8	%