Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOP
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/n79e855asg

Table of Contents

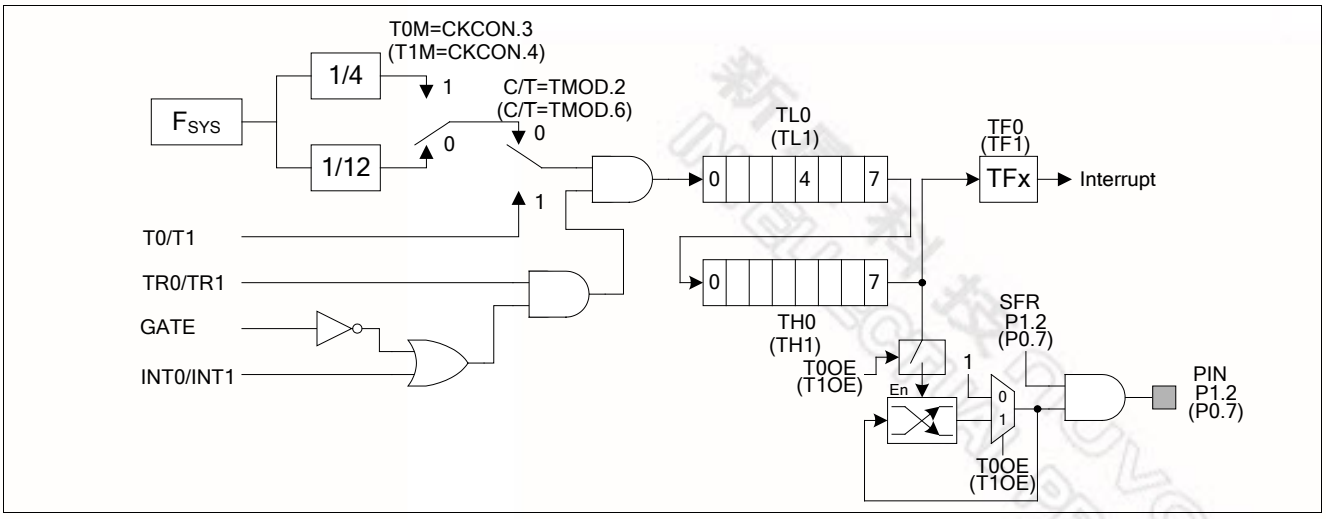


Figure 10–2 Timers/Counters 0 and 1 in Mode 1

10.1.3 Mode 2 (8-bit Auto-Reload Timer)

In Mode 2, the Timer/Counter is in auto-reload mode. In this mode, TLx acts as an 8-bit count register whereas THx holds the reload value. When the TLx register overflows from FFH to 00H, the TFx bit in TCON is set and TLx is reloaded with the contents of THx and the counting process continues from here. The reload operation leaves the contents of the THx register unchanged. This feature is best suitable for UART baud rate generator for it runs without continuous software intervention. Note that only Timer1 can be the baud rate source for UART. Counting is enabled by the TRx bit and proper setting of GATE and $\overline{INTx}$ pins. The functions of GATE and $\overline{INTx}$ pins are just the same as Mode 0 and 1.

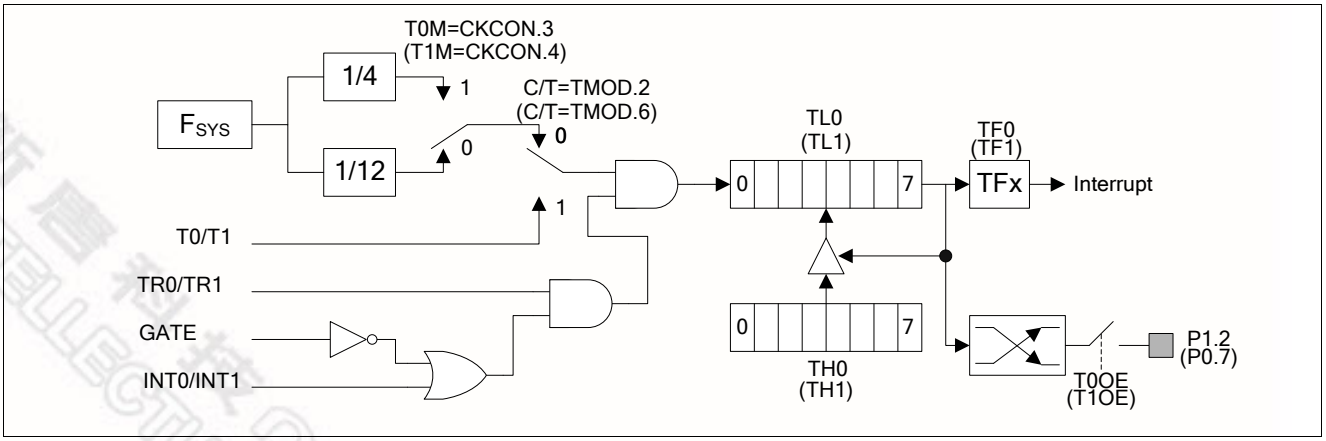


Figure 10–3 Timer/Counter 0 and 1 in Mode 2

10.1.4 Mode 3 (Two Separate 8-bit Timers)

Mode 3 has different operating methods for the two timers/counters. For timer/counter 1, mode 3 simply freezes the counter. Timer/Counter 0, however, configures TL0 and TH0 as two separate 8 bit count registers in this mode. The logic for this mode is shown in the following figure. TL0 uses the Timer/Counter 0 control bits $C/\overline{T}$, GATE, TR0, $\overline{INT0}$ and TF0. The TL0 can be used to count clock cycles (clock/12 or clock/4) or 1-to-0 transitions on pin T0 as determined by C/T

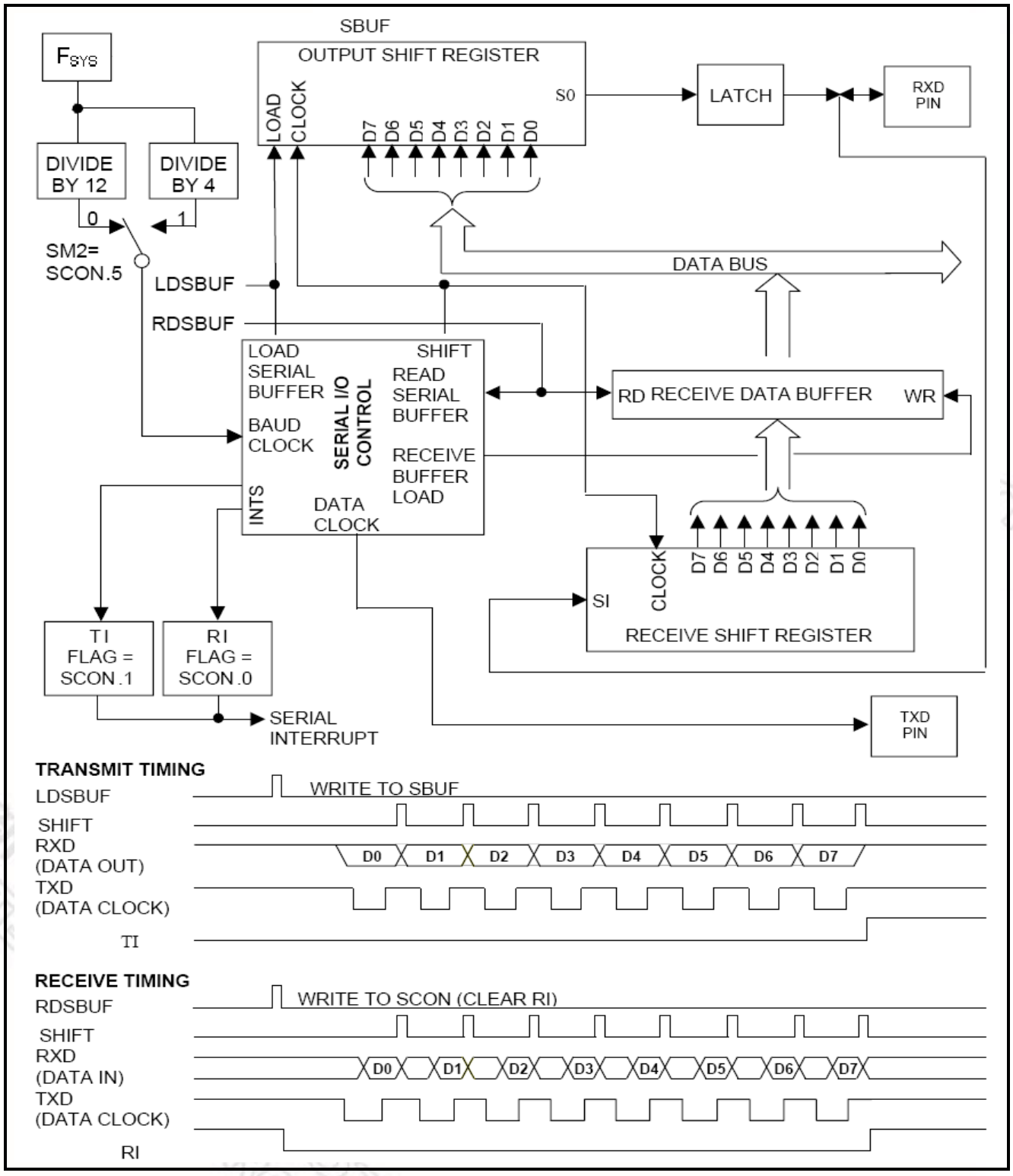


Figure 12–1 Serial Port Mode 0 Function Block

R/W	R/W	-	-	R/W	-	R	R/W

Address: A2H Reset value: 0000 0000B

Bit	Name	Description
3	DisP26	0 = Enable P2.6 digital input and output. 1 = Disable P2.6 digital input and output for ADC channel 7 used.

The demo code of ADC channel 0 with clock source = Fsys/4 is as follows:

```
    ORG     0000H
    LJMP    START

    ORG     005BH           ;ADC Interrupt Service Routine
    CLR     ADCI            ;Clear ADC flag
    reti

START:
    ORL     P0DIDS,#02H     ; Disable digital function for P0.1
    ORL     P0M1,#02H       ; ADC0(P0.1) is input-only mode
    ANL     P0M2,#0FDH
    ANL     ADCCON0,#0F8H    ;ADC0(P0.1) as ADC Channel
    ANL     ADCCON1,#0FDH   ;The FSYS/4 clock is used as ADC clock.
    SETB    EADC            ;Enable ADC Interrupt
    SETB    EA
    ORL     ADCCON1,#80H    ;Enable ADC Function

Convert_LOOP:
    SETB    ADCS            ;Trigger ADC
    ORL     PCON,#01H       ;Enter idle mode
    MOV     P0,ADCH         ;Converted Data put in P0 and P1
    MOV     P1,ADCL
    SJMP    Convert_LOOP

    END
```

I2STA – I²C Status

7	6	5	4	3	2	1	0
I2STA[7:3]					0	0	0
R					R	R	R

Address: BDH Reset value: 1111 1000B

Bit	Name	Description
7:3	I2STA[7:3]	**I²C Status Code** The most five bits of I2STA contains the status code. There are 26 possible status codes. When I2STA is F8H, no relevant state information is available and SI flag keeps 0. All other 25 status codes correspond to the I²C states. When each of the status is entered, SI will be set as logic 1 and a interrupt is requested.
2:0	-	**Reserved** The least three bits of I2STA are always read as 0.

I2DAT – I²C Data

7	6	5	4	3	2	1	0
I2DAT[7:0]							
R/W							

Address: BCH Reset value: 0000 0000B

Bit	Name	Description
7:0	I2DAT[7:0]	**I²C Data** I2DAT contains a byte of the I²C data to be transmitted or a byte which has just received. Data in I2DAT remains as long as SI is logic 1. The result of reading or writing I2DAT during I²C transceiving progress is unpredicted. While data in I2DAT is shifted out, data on the bus is simultaneously being shifted in to update I2DAT. I2DAT always shows the last byte that presented on the I²C bus. Thus the event of lost arbitration, the original value of I2DAT changes after the transaction.

I2ADDR – I²C Own Slave Address

7	6	5	4	3	2	1	0
I2ADDR[7:1]							GC
R/W							R/W

Address: C1H Reset value: 0000 0000B

Bit	Name	Description
7:1	I2ADDR[7:1]	**I²C device's own Slave Address** In Master mode: These bits have no effect. In Slave mode: The 7 bits define the slave address of this I²C device by the user. The master should address this I²C device by sending the same address in the first byte data after a START or a repeated START condition. If the AA flag is set, this I²C device will acknowledge the master after receiving its own address and become an addressed slave. Otherwise, the addressing from the master will be ignored.

Bit	Name	Description
0	GC	**General Call Bit** In Master mode: This bit has no effect. In Slave mode: 0 = General Call is always ignored. 1 = General Call is recognized if AA flag is 1; otherwise, it is ignored if AA is 0.

I2CLK – I²C Clock

7	6	5	4	3	2	1	0
I2CLK[7:0]							
R/W							

Address: BEH Reset value: 0000 1110B

Bit	Name	Description
7:0	I2CLK[7:0]	**I²C Clock Setting** In Master mode: This register determines the clock rate of I²C bus when the device is in Master mode. The clock rate follows the formula below. $F_{I^2C} = \frac{F_{PHERI}}{1+I2CLK}$ The default value will make the clock rate of I²C bus 400kbps if the clock system 24 MHz with DIVM 1/4 mode is used. Note that the I2CLK value of 00H and 01H are not valid. This is an implement limitation. In Slave mode: This byte has no effect. In slave mode, the I²C device will automatically synchronize with any given clock rate up to 400kps.

16.4 Operation Modes

In I²C protocol definitions, there are four operating modes including master transmitter, master receiver, slave receive, and slave transmitter. There is also a special mode called General Call. Its operation is similar to master transmitter mode.

16.4.1 Master Transmitter Mode

In Master Transmitter mode, several bytes of data are transmitted to a slave receiver. The master should prepare by setting desired clock rate in I2CLK and enabling I²C bus by writing I2CEN (I2CON.6) as logic 1. The master transmitter mode may now be entered by setting STA (I2CON.5) bit as 1. The hardware will test the bus and generate a START condition as soon as the bus becomes free. After a START condition is successfully produced, the SI flag (I2CON.3) will be set and the status code in I2STA show 08H. The progress is continued by loading I2DAT with the target slave address and the data direction bit “write” (SLA+W). The SI bit should then be cleared to commence SLA+W transaction.

PWM1H – PWM 1 High Register

7	6	5	4	3	2	1	0
-	-	-	-	-	-	PWM1.9	PWM1.8
-	-	-	-	-	-	R/W	R/W

Address: D3H Reset value: 0000 0000B

Bit	Name	Description
7:2	-	**Reserved**
1:0	PWM1H	PWM 1 High Bits Register bit[9:8]

PWM2L – PWM 2 Low Register

7	6	5	4	3	2	1	0
PWM2.7	PWM2.6	PWM2.5	PWM2.4	PWM2.3	PWM2.2	PWM2.1	PWM2.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: DDH Reset value: 0000 0000B

Bit	Name	Description
7:0	PWM2L	PWM 2 Low Bits Register bit[7:0]

PWM2H – PWM 2 High Register

7	6	5	4	3	2	1	0
-	-	-	-	-	-	PWM2.9	PWM2.8
-	-	-	-	-	-	R/W	R/W

Address: D5H Reset value: 0000 0000B

Bit	Name	Description
7:2	-	**Reserved**
1:0	PWM2H	PWM 2 High Bits Register bit[9:8]

PWM3L – PWM 3 Low Register

7	6	5	4	3	2	1	0
PWM3.7	PWM3.6	PWM3.5	PWM3.4	PWM3.3	PWM3.2	PWM3.1	PWM3.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: DEH Reset value: 0000 0000B

Bit	Name	Description
7:0	PWM3L	PWM 0 Low Bits Register bit[7:0]

PWM3H – PWM 3 High Register

7	6	5	4	3	2	1	0
-	-	-	-	-	-	PWM3.9	PWM3.8

PWM demo code is as follows:

```
    ORG     0H
    SJMP    START
    ORG     100H
START:
    MOV     PWMPH,#0              ;PWM Frequency = Fsys/(1+PWMP)
    MOV     PWMPL,#0FFH           ;If Fsys=20MHz, PWM Frequency=78.1kHz
    MOV     PWM0H,#0
    MOV     PWM0L,#080H           ;PWM0(P0.1) duty = PWM0/(1+PWMP)
    MOV     PWM1H,#0
    MOV     PWM1L,#0A0H           ;PWM1(P1.6) duty = PWM1/(1+PWMP)
    MOV     PWM2H,#0
    MOV     PWM2L,#0C0H           ;PWM2(P1.7) duty = PWM2/(1+PWMP)
    MOV     PWM3H,#0
    MOV     PWM3L,#0F0H           ;PWM3(P0.0) duty = PWM3/(1+PWMP)

    ORL     PWMCON0,#0D0H         ;Start PWM

    MOV     PWMCON1,#30H          ;PWM will be stopped when P0.2 is low level.
                                  ;PWM output condition is follow PWMNB setting.
                                  ;In this case, PWM0B=PWM1B=PWM2B=PWM3B=0
    END
```

20.2 ISP Command Table

ISP Command		ISPCN				ISPAH, ISPAL	ISPFD
		A17, A16	FOEN	FCEN	FCTRL[3:0]	A[15:0]	D[7:0]
Read Company ID		x, x[1]	0	0	1011	x[1]	Data out D[7:0]=DAH
APROM & Data Flash	FLASH Page Erase	0, 0	1	0	0010	Address in A[15:0]	x[1]
	FLASH Program	0, 0	1	0	0001	Address in A[15:0]	Data in D[7:0]
	FLASH Read	0, 0	0	0	0000	Address in A[15:0]	Data out D[7:0]
LDROM	FLASH Page Erase	0, 1	1	0	0010	Address in A[15:0]	x[1]
	FLASH Program	0, 1	1	0	0001	Address in A[15:0]	Data in D[7:0]
	FLASH Read	0, 1	0	0	0000	Address in A[15:0]	Data out D[7:0]
CONFIG[2] Page Erase		1, 1	1	0	0010	Address in A[15:0]=0000H	x[1]
CONFIG[2] Program		1, 1	1	0	0001	Address in A[15:0]	Data in D[7:0]
CONFIG[2] Read		1, 1	0	0	0000	Address in A[15:0]	Data out D[7:0]

Note:
[1] 'x' means '*don't care*'.
[2] The 'CONFIG' means the MCU hardware configuration.
[3] Each page has 128 bytes. So, the address for Page Erase should be 0000, 0080H, 0100H, 0180H, 0200H, .., which is incremented by 0080H.

20.3 Access Table of ISP Programming

Destination	UNLOCK		LOCK	
	ISP Code Residence		ISP Code Residence	
	APROM	LDROM	APROM	LDROM
APROM				
LDROM	[1]		[1]	
Data Flash				
CONFIGs		[2]		[2]
ID (read)				
Block color	Comment			
	Fully accessing			
	Read only			
	Accessing inhibit			
[1]	LDUE should be 1, or it will be read only.			
[2]	New CONFIG functions after POR, WDT, Reset pin or software reset			

Note:

I. CONFIG full accessing by LDROM while LOCK.
II. Inhibit APROM jump to LDROM or LDROM jump to APROM.
III. MCU run in APROM cannot read CONFIGs.

20.4 ISP User Guide

ISP facilitates the updating flash contents in a convenient way; however, the user should follow some restricted laws in order that the ISP operates correctly. Without noticing warnings will possible cause undetermined results even serious damages of devices. Be attention of these notices. Furthermore, this paragraph will also support useful suggestions during ISP procedures.

(1) If no more ISP operation needs, the user should clear ISPEN (CHPCON.0) to zero. It will make the system void to trigger ISP unaware. Furthermore, ISP requires internal 22.1184MHZ RC oscillator running. If the external clock source is chosen, disabling ISP will stop internal 22.1184 MHz RC for saving power consumption. Note that a write to ISPEN is TA protected.

(2) CONFIG bytes can be ISP fully accessed only when loader code executing in LDROM. New CONFIG bytes other than CBS bit activate after all resets. New CBS bit activates after resets other than software reset.

logical states they had at the time Idle was activated. Generally it saves considerable power of typical half of the full operating power.

Since the clock provided for peripheral function logic circuit like timer or serial port still remain in Idle mode, the CPU can be released from the Idle mode using any of the interrupt sources if enabled. The user can put the device into Idle mode by writing 1 to the bit IDL (PCON.0). The instruction that sets the IDL bit is the last instruction that will be executed before the device goes into Idle mode.

The Idle mode can be terminated in two ways. First, any interrupt if enabled will cause an exit. This will automatically clear the IDL bit, terminate the Idle mode, and the interrupt service routine (ISR) will be executed. After using the RETI instruction to jump out of the ISR, execution of the program will be the one following the instruction which put the CPU into Idle mode. The second way to terminate the Idle mode is with any reset other than software reset.

21.2 Power-down Mode

Power-down mode is the lowest power state that N79E855/854 can enter. It remain the power consumption as a ”μA” level. This is achieved by stopping the clock system no matter internal RC clock or external crystal. Both of CPU and peripheral functions like Timers or UART are frozen. Flash memory stops. All activity is completely stopped and the power consumption is reduced to the lowest possible value. The device can be put into Power-down mode by writing 1 to bit PD (PCON.1). The instruction that does this action will be the last instruction to be executed before the device goes into Power-down mode. In Power-down mode, RAM maintains its content. The port pins output the values held by their respective.

There are two ways to exit N79E855/854 from Power-down mode. The first is with all resets except software reset. BOD reset will also wake up CPU from Power-down mode. Make sure that BOD detection is enabled before the system enters into Power-down. However, for a principle of least power consumption, it is uncommon to enable BOD detection in Power-down mode, which is not a recommended application. Of course, the RST pin reset and power-on reset will remove the Power Down status. After RST pin reset or power-on reset, the CPU is initialized and starts executing program code from the beginning.

The N79E855/854 can be woken up from Power-down mode by forcing an external interrupt pin activated, providing the corresponding interrupt enabled and the global enable EA bit (IE.7) is set. If these conditions are met, the trigger on the external pin will asynchronously restart the clock system. Then device executes the interrupt service routine (ISR) for the corresponding external interrupt. After the ISR is completed, the program execution returns to the instruction after the one that puts the device into Power-down mode and continues.

BOD, Watchdog and KBI interrupt are other sources to wake up CPU from Power Down. As mentioned before the user will endure the current of BOD detection circuit. Using KBI interrupt to wake up CPU from Power Down has a

23 Power Monitoring

To prevent incorrect execution during power up and power drop, N79E855/854 provide three power monitor functions, power-on detection and BOD detection.

23.1 Power-on Detection

The power-on detection function is designed for detecting power up after power voltage reaches to a level where system can work. After power-on detected, the POF (PCON.4) will be set 1 to indicate a cold reset, a power-on reset complete. The POF flag can be cleared via software.

23.2 Brown-out Detection

The other power monitoring function, BOD detection circuit is for monitoring the V_{DD} level during execution. There are two programmable BOD trigger levels available for wide voltage applications. The two nominal levels are 2.7V and 3.8V selected via setting CBOV in CONFIG2. When V_{DD} drops to the selected BOD trigger level (V_{BOD}), the BOD detection logic will either reset the CPU or request a BOD interrupt. The user may determine BOD reset or interrupt enable according to different application systems.

The BOD detection will request the interrupt while V_{DD} drops below V_{BOD} while BORST (PMCR.4) is 0. In this case, BOF (PMCR.3) will set as 1. After the user clears this flag whereas V_{DD} remains below V_{BOD}, BOF will not set again. BOF just acknowledge the user a power drop occurs. The BOF will set 1 after V_{DD} goes higher than V_{BOD} to indicate a power resuming. V_{BOD} has a hysteresis of 20~200mV.

CONFIG2

7	6	5	4	3	2	1	0
CBODEN	CBOV	-	CBORST	-	-	-	-
R/W	R/W	-	R/W	-	-	-	-

Unprogrammed value: 1111 1111B

Bit	Name	Description
7	CBODEN	**CONFIG BOD Detection Enable** 1 = Disable BOD detection. 0 = Enable BOD detection. BODEN is initialized by inverted CBODEN (CONFIG2, bit-7) at any resets.

24.2 BOD Reset

BOD detection circuit is for monitoring the V_{DD} level during execution. When V_{DD} drops to the selected BOD trigger level (V_{BOD}) or V_{DD} rises over V_{BOD}, the BOD detection logic will reset the CPU if BORST (PMCR.4) setting 1.

PMCR – Power Monitoring Control (TA Protected)

7	6	5	4	3	2	1	0
BODEN	BOV	-	BORST	BOF	-	-	-
R/W	R/W	-	R/W	R/W	-	-	-

Address: A3H Reset value: see Table 7–2 N79E855/854 SFR Description and Reset Values

Bit	Name	Description
7	BODEN	**BOD-detect Function Control** BODEN is initialized by inverted CBODEN (CONFIG2, bit-7) at any resets. 1 = Enable BOD detection. 0 = Disable BOD detection.
6	BOV	**BOD Voltage Select Bits** BOD are initialized at reset with the value of bits CBOV in CONFIG3-bits BOD Voltage Select bits:
5	-	**Reserved**
4	BORST	**BOD Reset Enable** This bit decides if a BOD reset is caused after a BOD event. 0 = Disable BOD reset when V_{DD} drops below V_{BOD} or V_{DD} rises above V_{BOD}. Chip will assert BOF when V_{DD} drops below V_{BOD}. 1 = Enable BOD reset when V_{DD} drops below V_{BOD} or V_{DD} rises above V_{BOD}.
3	BOF	**BOD Flag** This flag will be set as logic 1 via hardware after a V_{DD} dropping below or rising above V_{BOD} event occurs. If both EBOD (IE.5) and EA (IE.7) are set, a BOD interrupt requirement will be generated. This bit should be cleared via software.
2	-	**It should be set to logic 0.**
1	-	**Reserved**
0	-	**Reserved**

CONFIG-bits CBOV	SFR BOV	BOD Voltage
1	0	Enable BOD= 2.7V
0	1	Enable BOD= 3.8V

24.3 RST Pin Reset

The hardware reset input is RST pin which is the input with a Schmitt trigger. A hardware reset is accomplished by holding the RST pin low for at least two machine-cycles to ensure detection of a valid hardware reset signal. The reset circuitry then synchronously applies the internal reset signal. Thus the reset is a synchronous operation and requires the clock to be running to cause an external reset.

Once the device is in reset condition, it will remain so as long as RST pin is 1. After the RST low is removed, the CPU will exit the reset state with in two machine-cycles and begin code executing from address 0000H. There is no flag associated with the RST pin reset condition. However since the other reset sources have flags, the external reset can be considered as the default reset if those reset flags are cleared.

If a RST pin reset applies while CPU is in Power-down mode, the way to trigger a hardware reset is slightly different. Since the Power-down mode stops clock system, the reset signal will asynchronously cause the clock system resuming. After the clock system is stable, CPU will enter into the reset state, then exit and start to execute program code from address 0000H.

Note: Because reset pin has internal pull-up resistor (about 200KΩ at V_{DD} = 5V), this pin cannot be floating. Reset pin should be connected to a 100Ω pull-up resistor and a 10uF pull-low capacitor.

24.4 Watchdog Timer Reset

The Watchdog Timer is a free running timer with programmable time-out intervals. The user can clear the Watchdog Timer at any time, causing it to restart the count. When the selected time-out occurs, the Watchdog Timer will reset the system directly. The reset condition is maintained via hardware for two machine-cycles. After the reset is removed the device will begin execution from 0000H.

Once a reset due to Watchdog Timer occurs the Watchdog Timer reset flag WDTRF (WDCON0.3) will be set. This bit keeps unchanged after any reset other than a power-on reset. The user may clear WDTRF via software.

26 Instruction Sets

The N79E855/854 executes all the instructions of the standard 8051 family. All instructions are coded within an 8-bit field called an OPCODE. This single byte should be fetched from Program Memory. The OPCODE is decoded by the CPU. It determines what action the microcontroller will take and whether more operation data is needed from memory. If no other data is needed, then only one byte was required. Thus the instruction is called a one byte instruction. In some cases, more data is needed. These will be two or three byte instructions.

Table 26–1 lists all instructions in details. The note of the instruction sets and addressing modes are shown below.

Rn (n = 0~7)	Register R0~R7 of the currently selected Register Bank.
	Direct 8-bit internal data location's address. This could be an internal data RAM location (0~127) or a SFR (e.g. I/O port, control register, status register, etc.) (128~255).
@Ri (i = 0, 1)	8-bit internal data RAM location (0~255) addressed indirectly through register R0 or R1.
#data	8-bit constant included in the instruction.
#data16	16-bit constant included in the instruction.
addr16	16-bit destination address. Used by LCALL and LJMP. A branch can be any within the 16 Kbytes Program Memory address space.
addr11	11-bit destination address. Used by ACALL and AJMP. The branch will be within the same 2 Kbytes page of Program Memory as the first byte of the following instruction.
rel	Signed (2's complement) 8-bit offset byte. Used by SJMP and all conditional branches. The range is -128 to +127 bytes relative to first byte of the following instruction.
bit	Direct addressed bit in internal data RAM or SFR.

Table 26–1 Instruction Set for N79E855/854

Instruction	OPCODE	Bytes	Clock Cycles	N79E855/854 vs. Tradition 80C51 Speed Ratio
NOP	00	1	4	3.0
ADD A, Rn	28~2F	1	4	3.0
ADD A, @Ri	26, 27	1	4	3.0
ADD A, direct	25	2	8	1.5
ADD A, #data	24	2	8	1.5
ADDC A, Rn	38~3F	1	4	3.0
ADDC A, @Ri	36, 37	1	4	3.0
ADDC A, direct	35	2	8	1.5
ADDC A, #data	34	2	8	1.5
SUBB A, Rn	98~9F	1	4	3.0

Table 26–1 Instruction Set for N79E855/854

Instruction	OPCODE	Bytes	Clock Cycles	N79E855/854 vs. Tradition 80C51 Speed Ratio
SWAP A	C4	1	4	3.0
MOV A, Rn	E8~EF	1	4	3.0
MOV A, @Ri	E6, E7	1	4	3.0
MOV A, direct	E5	2	8	1.5
MOV A, #data	74	2	8	1.5
MOV Rn, A	F8~FF	1	4	3.0
MOV Rn, direct	A8~AF	2	8	3.0
MOV Rn, #data	78~7F	2	8	1.5
MOV @Ri, A	F6, F7	1	4	3.0
MOV @Ri, direct	A6, A7	2	8	3.0
MOV @Ri, #data	76, 77	2	8	1.5
MOV direct, A	F5	2	8	1.5
MOV direct, Rn	88~8F	2	8	3.0
MOV direct, @Ri	86, 87	2	8	3.0
MOV direct, direct	85	3	12	2.0
MOV direct, #data	75	3	12	2.0
MOV DPTR, #data16	90	3	12	2.0
MOVC A, @A+DPTR	93	1	8	3.0
MOVC A, @A+PC	83	1	8	3.0
MOVX A, @Ri[1]	E2, E3	1	8	3.0
MOVX A, @DPTR[1]	E0	1	8	3.0
MOVX @Ri, A[1]	F2, F3	1	8	3.0
MOVX @DPTR, A[1]	F0	1	8	3.0
PUSH direct	C0	2	8	3.0
POP direct	D0	2	8	3.0
XCH A, Rn	C8~CF	1	4	3.0
XCH A, @Ri	C6, C7	1	4	3.0
XCH A, direct	C5	2	8	1.5
XCHD A, @Ri	D6, D7	1	4	3.0
CLR C	C3	1	4	3.0
CLR bit	C2	2	8	1.5
SETB C	D3	1	4	3.0
SETB bit	D2	2	8	1.5
CPL C	B3	1	4	3.0
CPL bit	B2	2	8	1.5
ANL C, bit	82	2	8	3.0
ANL C, /bit	B0	2	8	3.0
ORL C, bit	72	2	8	3.0
ORL C, /bit	A0	2	8	3.0
MOV C, bit	A2	2	8	1.5

27 In-Circuit Program (ICP)

The ICP (In-Circuit-Program) mode is another approach to access the Flash EPROM. There are only 3 pins needed to perform the ICP function. One is input /RST pin, which should be fed to GND in the ICP working period. One is clock input, shared with P1.7, which accepts serial clock from external device. Another is data I/O pin, shared with P1.6, that an external ICP program tool shifts in/out data via P1.6 synchronized with clock(P1.7) to access the Flash EPROM of N79E855/854.

Upon entry into ICP program mode, all pin will be set to quasi-bidirectional mode, and output to level "1". The N79E855/854 support programming of Flash EPROM (16K/8K bytes APROM EPROM), Data Flash memory (**128** bytes per page) and LDROM. User has the option to program the APROM, Data Flash and LDROM.

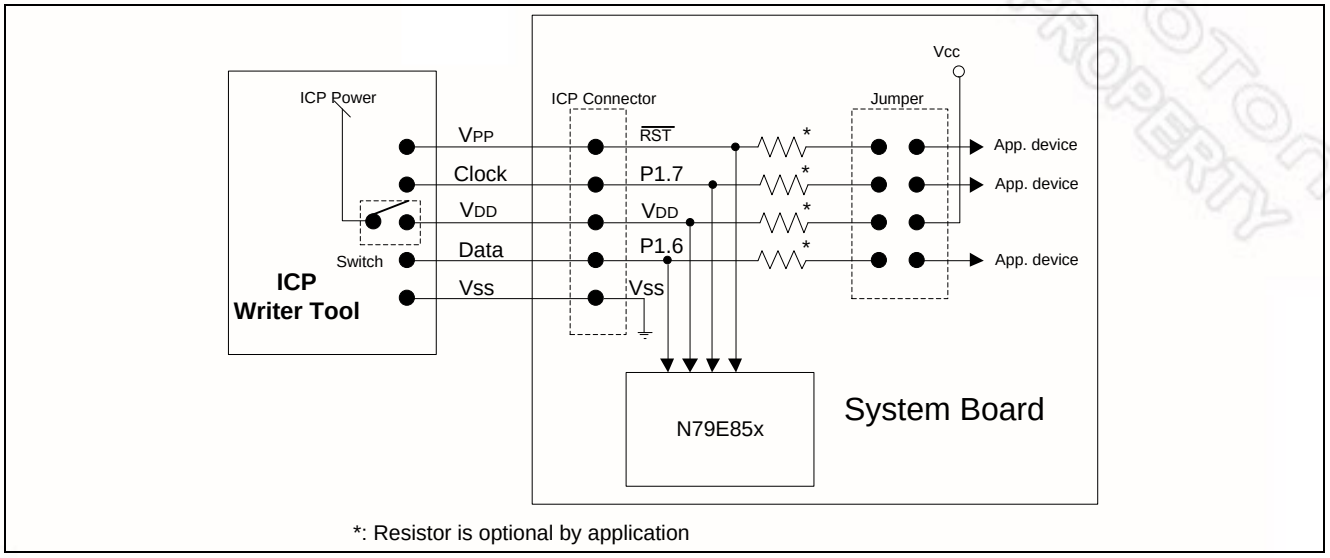


Figure 27–1 ICP Connection with N79E85xA

Note:

1. When using ICP to upgrade code, the /RST, P1.6 and P1.7 should be taken within design system board.
2. After program finished by ICP, to suggest system power should power off and remove ICP connector then power on.
3. It is recommended that user perform erase function and programming configure bits continuously without any interruption.

Table 28–3 DC Characteristics

(V_{DD}–V_{SS} = 2.4~5.5V, TA = -40~85°C, unless otherwise specified.)

Sym	Parameter	Test Conditions	MIN	TYP	MAX	Unit
V_{IL1}	Input Low Voltage (general purpose I/O with Schmitt trigger input)	2.4 < V_{DD} < 5.5V	-0.5		0.3V_{DD}	V
V_{IL2}	Input Low Voltage (/RST, XTAL1)	2.4 < V_{DD} < 5.5V	-0.5		0.2V_{DD}-0.1	V
V_{IH}	Input High Voltage (general purpose I/O with TTL input)	2.4 < V_{DD} < 5.5V	0.2V_{DD}+0.9		V_{DD}+0.5	V
V_{IH1}	Input High Voltage (general purpose I/O with Schmitt trigger input)	2.4 < V_{DD} < 5.5V	0.7V_{DD}		V_{DD}+0.5	V
V_{IH2}	Input High Voltage (/RST, XTAL1)	2.4 < V_{DD} < 5.5V	0.7V_{DD}		V_{DD}+0.5	V
V_{OL}	Output Low Voltage (general purpose I/O of P0,P2,P3, all modes except input only)	V_{DD}=4.5V, I_{OL}= **20**mA[3], [4]			0.45	V
		V_{DD}=3.0V, I_{OL}= **14**mA[3], [4]			0.45	V
		V_{DD}=2.4V, I_{OL}= **10**mA[3], [4]			0.45	V
V_{OL1}	Output Low Voltage (P10, P11, P14, P16, P17) (All modes except input only)	V_{DD}=4.5V, I_{OL}= **38**mA[3], [4]			0.45	V
		V_{DD} =3.0V, I_{OL}= **27**mA[3], [4]			0.45	V
		V_{DD} =2.4V, I_{OL}= **20**mA[3], [4]			0.45	V
V_{OH}	Output High Voltage (general purpose I/O, quasi bidirectional)	V_{DD}=4.5V I_{OH}= **-380**µA[4]	2.4			V
		V_{DD}=3.0V I_{OH}= **-90**µA[4]	2.4			V
		V_{DD}=2.4V I_{OH}= **-48**µA[4]	2.0			V

Table 28–3 DC Characteristics

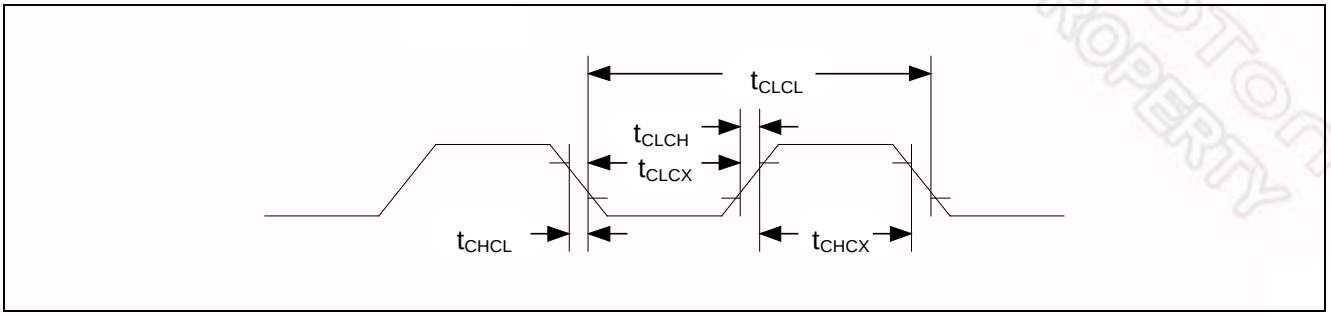
(V_{DD}–V_{SS} = 2.4~5.5V, TA = -40~85°C, unless otherwise specified.)

Sym	Parameter	Test Conditions	MIN	TYP	MAX	Unit
V_{OH1}	Output High Voltage (general purpose I/O, push-pull)	V_{DD}=4.5V I_{OH}= **-28.0**mA[3], [4]	2.4			V
		V_{DD}=3.0V I_{OH}= **-7**mA[3], [4]	2.4			V
		V_{DD} = 2.4V I_{OH} = **-3.5** mA[3], [4]	2.0			V
I_{IL}	Logical 0 Input Current (general purpose I/O, quasi bi-direction)	V_{DD}=5.5V, V_{IN} = 0.4V		**-40 at 5.5V**	-50	µA
I_{TL}	Logical 1 to 0 Transition Current (general purpose I/O, quasi bi-direction)	V_{DD} = 5.5V, V_{IN} = 2.0V[2]		**-550 at 5.5V**	-650	µA
I_{LI}	Input Leakage Current (general purpose I/O, open-drain or input only)	0 < V_{IN} < V_{DD}		**<1**	±10	µA
I_{OP}	OP Current (Active mode[5])	XTAL 12 MHz, V_{DD} = 5.0V		**3.1**		mA
		XTAL 24 MHz, V_{DD} = 5.5V		**4.3**		mA
		XTAL 12 MHz, V_{DD} = 3.3V		**1.7**		mA
		XTAL 24 MHz, V_{DD} = 3.3V		**3.2**		mA
		Internal 22.1184 MHz, V_{DD} = 5V		**2.3**		mA
		Internal 22.1184 MHz, V_{DD} = 3.3V		**2.2**		mA
I_{IDLE}	IDLE Current	XTAL 12 MHz, V_{DD} = 5.0V		**2.7**		mA
		XTAL 24 MHz, V_{DD} = 5.5V		**3.7**		mA

28.3.2 4 ~ 24 MHz XTAL Specifications

Parameter	Condition	MIN.	TYP.	MAX.	Unit
Input clock frequency	External crystal	4		24	MHz

Parameter	Symbol	MIN.	TYP.	MAX.	Units	Notes
External crystal Frequency	$1/t_{CLCL}$	4		24	MHz	
Clock High Time	t_{CHCX}	20.8	-	-	nS	
Clock Low Time	t_{CLCX}	20.8	-	-	nS	
Clock Rise Time	t_{CLCH}	-	-	10	nS	
Clock Fall Time	t_{CHCL}	-	-	10	nS	



Note: Duty cycle is 50%.

28.3.3 Internal RC Oscillator Specifications – 22.1184 MHz/11.0592 MHz

Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Center Frequency			22.1184/11.0592		MHz
Internal Oscillator Frequency	$+25^0C$ at V_{DD} = 5V	-1		+1	%
	$+25^0C$ at V_{DD} = 2.7~5.5V	-3		+3	%
	-10^0C~$+70^0C$ at V_{DD} = 2.7~5.5V	-5		+5	%
	-40^0C~$+85^0C$ at V_{DD} = 2.7~5.5V	-8		+8	%