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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CSI, EBI/EMI, I²C, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	56
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 10x12b, 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3453gf-r-gas-ax

2.3 Pin I/O Circuits and Recommended Connection of Unused Pins

It is recommended that 1 to 10 kΩ resistors be used when connecting to AV_{SS2}, EV_{DD0}, EV_{DD1}, EV_{DD2} (V850E/IG3 only) or EV_{SS0}, EV_{SS1}, EV_{SS2} (V850E/IG3 only) via resistors.

(1/4)

Pin	Alternate-Function Pin Name	Pin No.				I/O Circuit Type	Recommended Connection
		IF3	IG3				
		GC	GC	GF	F1		
P00	TOA20/TIA20/TOA2OFF/INTP00	70	91	19	A6	5-AH	Input: Independently connect to EV_{DD0}, EV_{DD1}, EV_{DD2}[Note 1] or EV_{SS0}, EV_{SS1}, EV_{SS2}[Note 1] via a resistor.
P01	TOA21/TIA21/INTP01	69	90	18	B6		
P02[Note 1]	TOA30[Note 1]/TIA30[Note 1]/TOA3OFF[Note 1]/INTP02[Note 1]	–	89	17	C6		Output: Leave open.
P03[Note 1]	TOA31[Note 1]/TIA31[Note 1]/INTP03[Note 1]	–	88	16	C7		
P04[Note 1]	TECR0[Note 1]/TIT00[Note 1]/TOT00[Note 1]/INTP04[Note 1]	–	84	12	C8		
P05[Note 1]	TENC00[Note 1]/EVTT0[Note 1]/INTP05[Note 1]	–	83	11	C9		
P06[Note 1]	TENC01[Note 1]/TIT01[Note 1]/TOT01[Note 1]/INTP06[Note 1]	–	82	10	C10		
P07[Note 1]	INTP07[Note 1]/CLKOUT[Note 2]	–	63	91	G12		
P10	TOB0T1/TIB01/TOB01/A0[Note 2]	78	99	27	B3		
P11	TOB0B1/TIB02/TOB02/A1[Note 2]	77	98	26	C3		
P12	TOB0T2/TIB03/TOB03/A2[Note 2]	76	97	25	A4		
P13	TOB0B2/TIB00/A3[Note 2]	75	96	24	B4		
P14	TOB0T3/EVTB0/A4[Note 2]	74	95	23	C4		
P15	TOB0B3/TRGB0/A5[Note 2]	73	94	22	A5		
P16	TOB0OFF/INTP08/ADTRG0/INTADT0/A6[Note 2]	72	93	21	B5		
P17	TOB00/INTP09/A7[Note 2]	71	92	20	C5		
P20	TOB1T1/TIB11/TOB11	23	28	56	P3		
P21	TOB1B1/TIB12/TOB12	24	29	57	N3		
P22	TOB1T2/TIB13/TOB13	25	30	58	P4		
P23	TOB1B2/TIB10	26	31	59	N4		
P24	TOB1T3/EVTB1	27	32	60	M4		
P25	TOB1B3/TRGB1	28	33	61	M5		
P26	TOB10/TOB1OFF/INTP10/ADTRG1/INTADT1	29	34	62	M6		
P27	DMS[Note 1]	36	45	73	M11		

Notes 1. V850E/IG3 only

2. μPD70F3454GC-8EA-A and 70F3454F1-DA9-A only

Remark IF3: V850E/IF3

IG3: V850E/IG3

GC (V850E/IF3): 80-pin plastic LQFP (14 × 14)

GC (V850E/IG3): 100-pin plastic LQFP (fine pitch) (14 × 14)

GF (V850E/IG3): 100-pin plastic LQFP (14 × 20)

F1 (V850E/IG3): 161-pin plastic FBGA (10 × 10)

Figure 6-18. Basic Timing in External Event Count Mode

Remarks 1. This figure shows the basic timing when the rising edge is specified as the valid edge of the external event count input.
2. V850E/IF3: m = 2, 4
V850E/IG3: m = 2 to 4
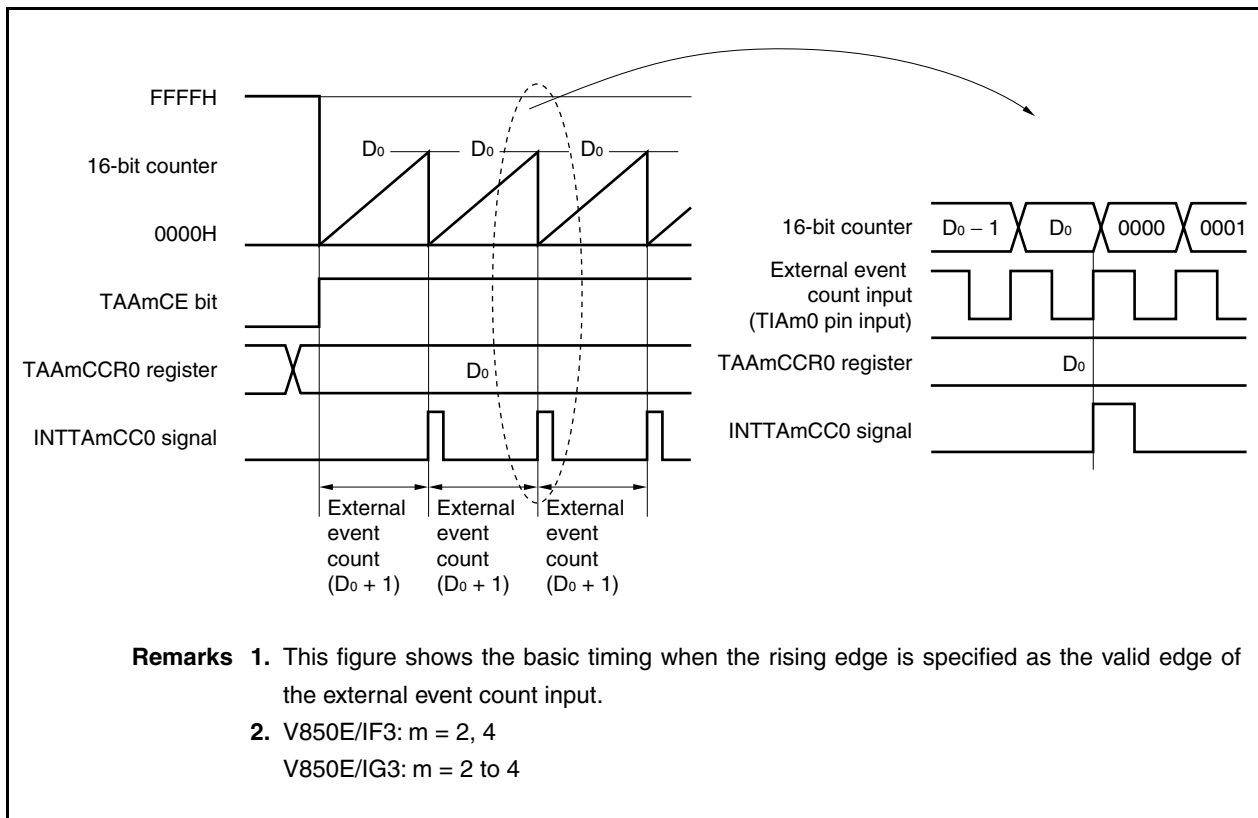
(d) Conflict between trigger detection and match with CCR0 buffer register

If the trigger is detected immediately after the INTTAmCC0 signal is generated, the 16-bit counter is cleared to 0000H and continues counting up. Therefore, the active period of the TOAm1 pin is extended by time from generation of the INTTAmCC0 signal to trigger detection.

16-bit counter | FFFF | 0000 | $D_0 - 1$ | D_0 | 0000 | 0000

External trigger input
(TIAm0 pin input)

CCR0 buffer register D_0

INTTAmCC0 signal

TOAm1 pin output

Extended
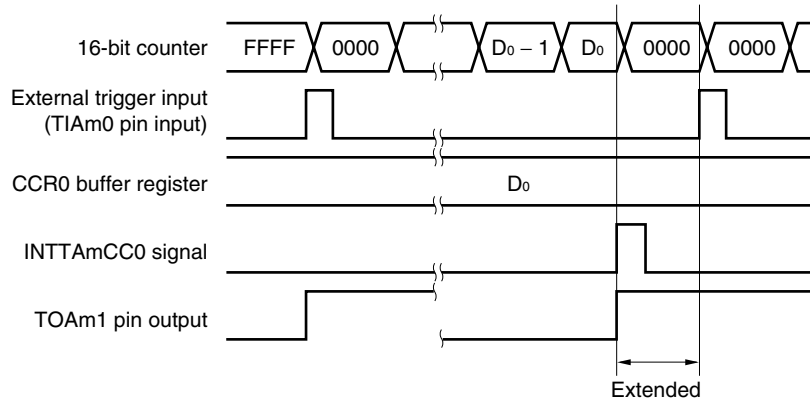
Remark V850E/IF3: m = 2, 4
V850E/IG3: m = 2 to 4

If the trigger is detected immediately before the INTTAmCC0 signal is generated, the INTTAmCC0 signal is not generated. The 16-bit counter is cleared to 0000H, the TOAm1 pin is asserted, and the counter continues counting. Consequently, the inactive period of the PWM waveform is shortened.

16-bit counter | FFFF | 0000 | $D_0 - 1$ | D_0 | 0000 | 0001

External trigger input
(TIAm0 pin input)

CCR0 buffer register D_0

INTTAmCC0 signal

TOAm1 pin output

Shortened
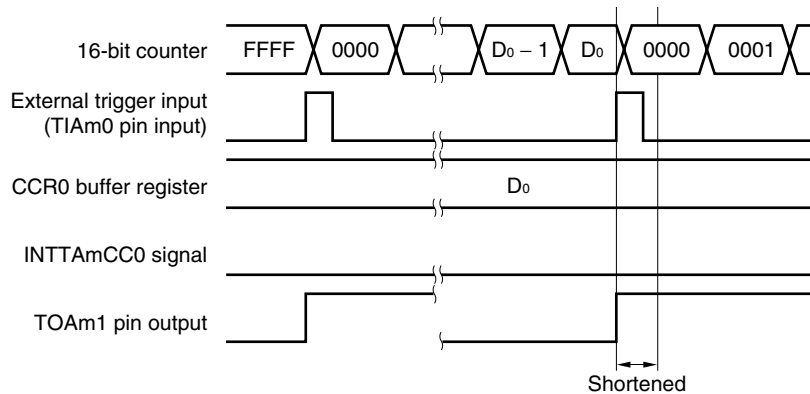
Remark V850E/IF3: m = 2, 4
V850E/IG3: m = 2 to 4

Figure 6-29. Basic Timing in One-Shot Pulse Output Mode
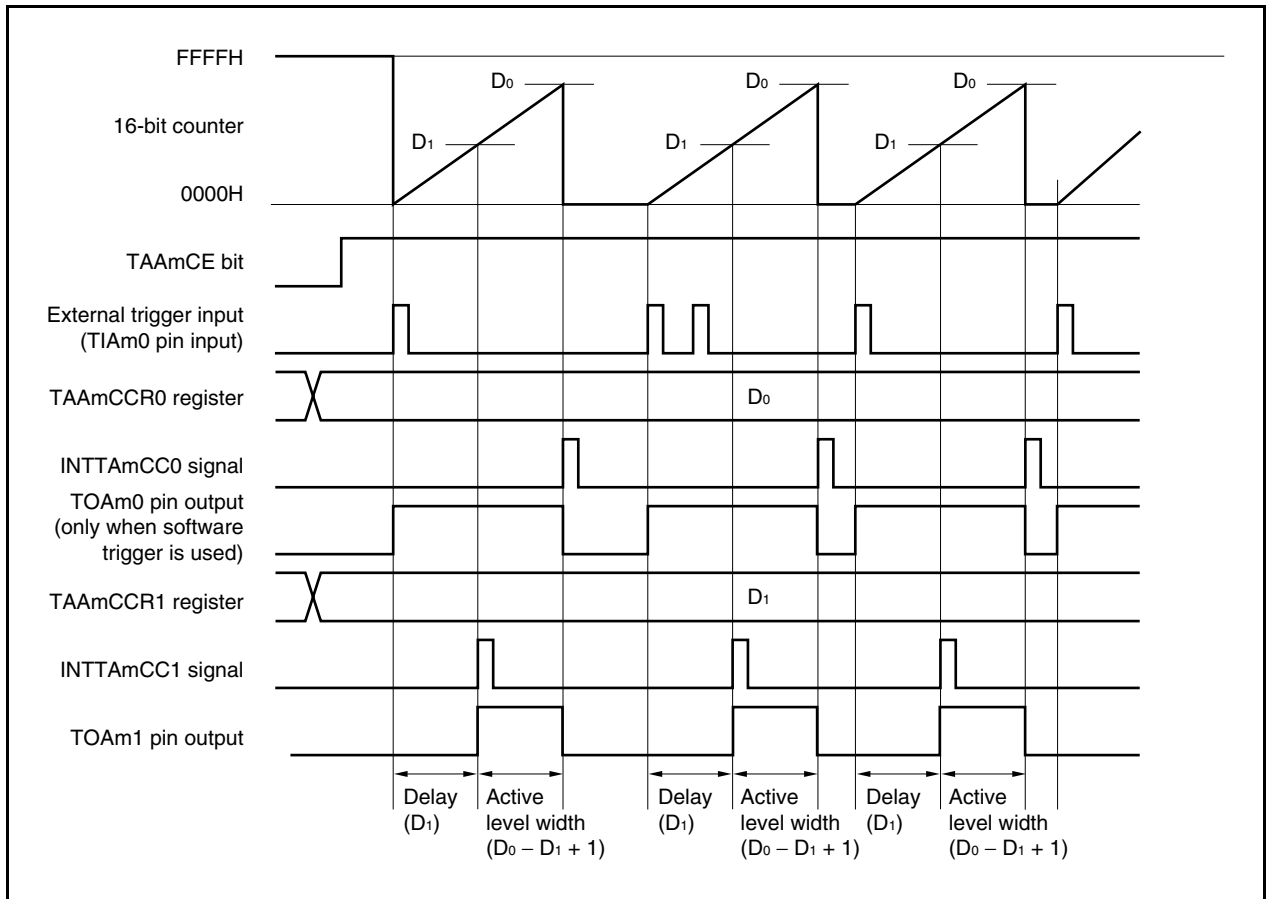
When the TAAmCE bit is set to 1, 16-bit timer/event counter AA waits for a trigger. When the trigger is generated, the 16-bit counter is cleared from FFFFH to 0000H, starts counting, and outputs a one-shot pulse from the TOAm1 pin. After the one-shot pulse is output, the 16-bit counter is cleared to 0000H, stops counting, and waits for a trigger. When the trigger is generated again, the 16-bit counter starts counting from 0000H. If a trigger is generated again while the one-shot pulse is being output, it is ignored.

The output delay period and active level width of the one-shot pulse can be calculated as follows.

Output delay period = (Set value of TAAmCCR1 register) × Count clock cycle
Active level width = (Set value of TAAmCCR0 register − Set value of TAAmCCR1 register + 1) × Count clock
cycle

The compare match interrupt request signal (INTTAmCC0) is generated when the 16-bit counter counts after its count value matches the value of the CCR0 buffer register. The compare match interrupt request signal (INTTAmCC1) is generated when the count value of the 16-bit counter matches the value of the CCR1 buffer register.

The valid edge of an external trigger input (TIAm0 pin) or setting the software trigger (TAAmCTL1.TAAnEST bit) to 1 is used as the trigger.

Remark V850E/IF3: m = 2, 4
V850E/IG3: m = 2 to 4

Figure 6-35. Software Processing Flow in PWM Output Mode (2/2)

<1> Count operation start flow

START

Register initial setting
TAAmCTL0 register
(TAAmCKS0 to TAAmCKS2 bits)
TAAmCTL1 register,
TAAmIOC0 register,
TAAmIOC2 register,
TAAmCCR0 register,
TAAmCCR1 register

Initial setting of these registers is performed before setting the TAAmCE bit to 1.

TAAmCE bit = 1

The TAAmCKS0 to TAAmCKS2 bits can be set at the same time when counting is enabled (TAAmCE bit = 1).

<2> TAAmCCR0, TAAmCCR1 register
setting change flow (cycle only)

Setting of TAAmCCR0 register

Writing same value (same as preset value of the TAAmCCR1 register) to the TAAmCCR1 register is necessary when only the set cycle is changed.

Setting of TAAmCCR1 register

When the counter is cleared after setting, the value of the TAAmCCRa register is transferred to the CCRa buffer register.

<3> TAAmCCR0, TAAmCCR1 register
setting change flow (duty only)

Setting of TAAmCCR1 register

Only writing of the TAAmCCR1 register must be performed when only the set duty factor is changed. When the counter is cleared after setting, the value of compare register a is transferred to the CCRa buffer register.

<4> TAAmCCR0, TAAmCCR1 register
setting change flow (cycle and duty)

Setting of TAAmCCR0 register

When the counter is cleared after setting, the value of compare register a is transferred to the CCRa buffer register.

Setting of TAAmCCR1 register

<5> Count operation stop flow

TAAmCE bit = 0

Counting is stopped.

STOP

Remark   V850E/IF3: m = 2, 4, a = 0, 1
V850E/IG3: m = 2 to 4, a = 0, 1

Figure 7-29. Basic Timing in PWM Output Mode

Remark n = 0, 1
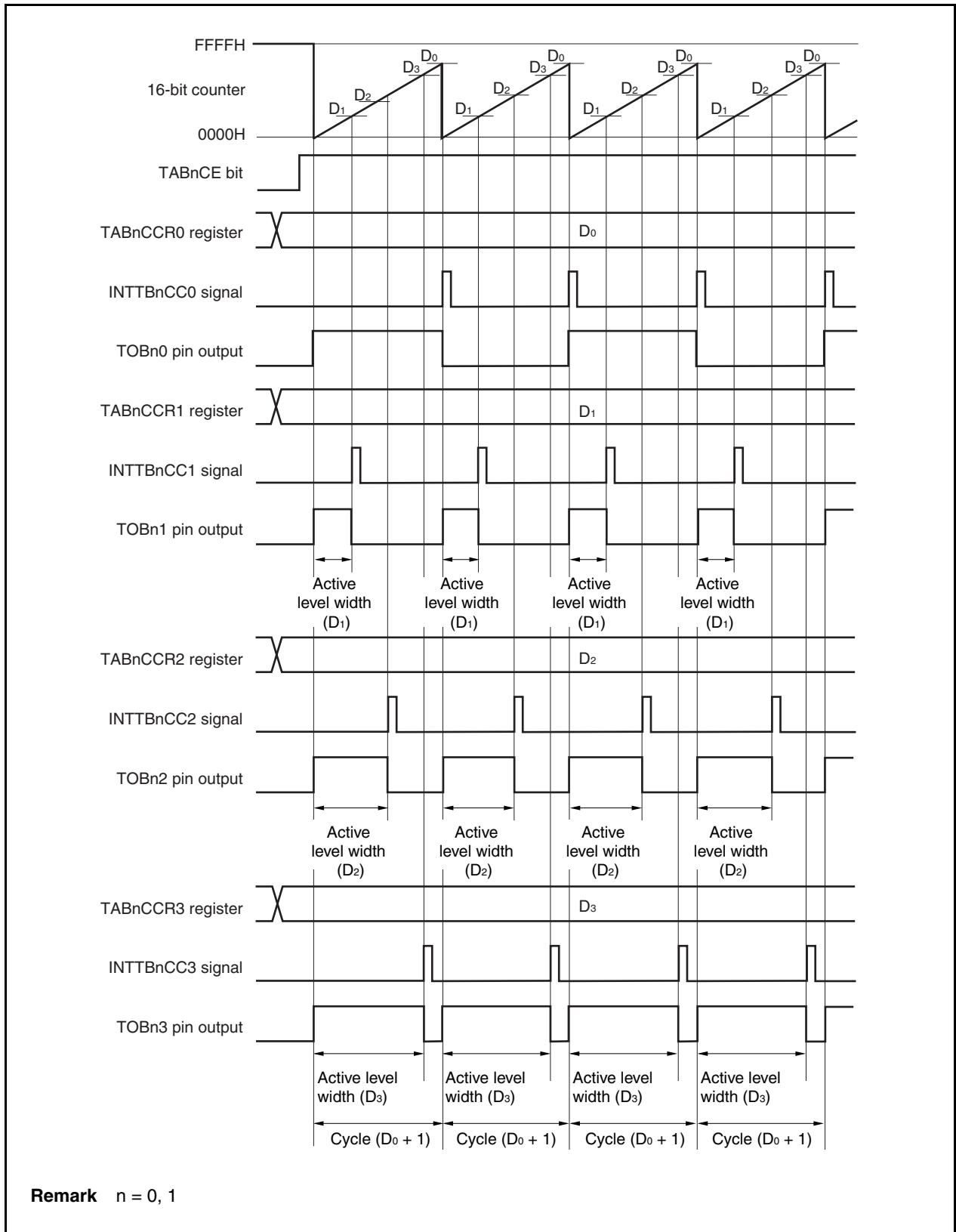
(2) PWM output mode operation timing

(a) Changing pulse width during operation

To change the PWM waveform while the counter is operating, write the TABnCCR1 register last.

Rewrite the TABnCCRa register after writing the TABnCCR1 register after the INTTBnCC0 signal is detected.
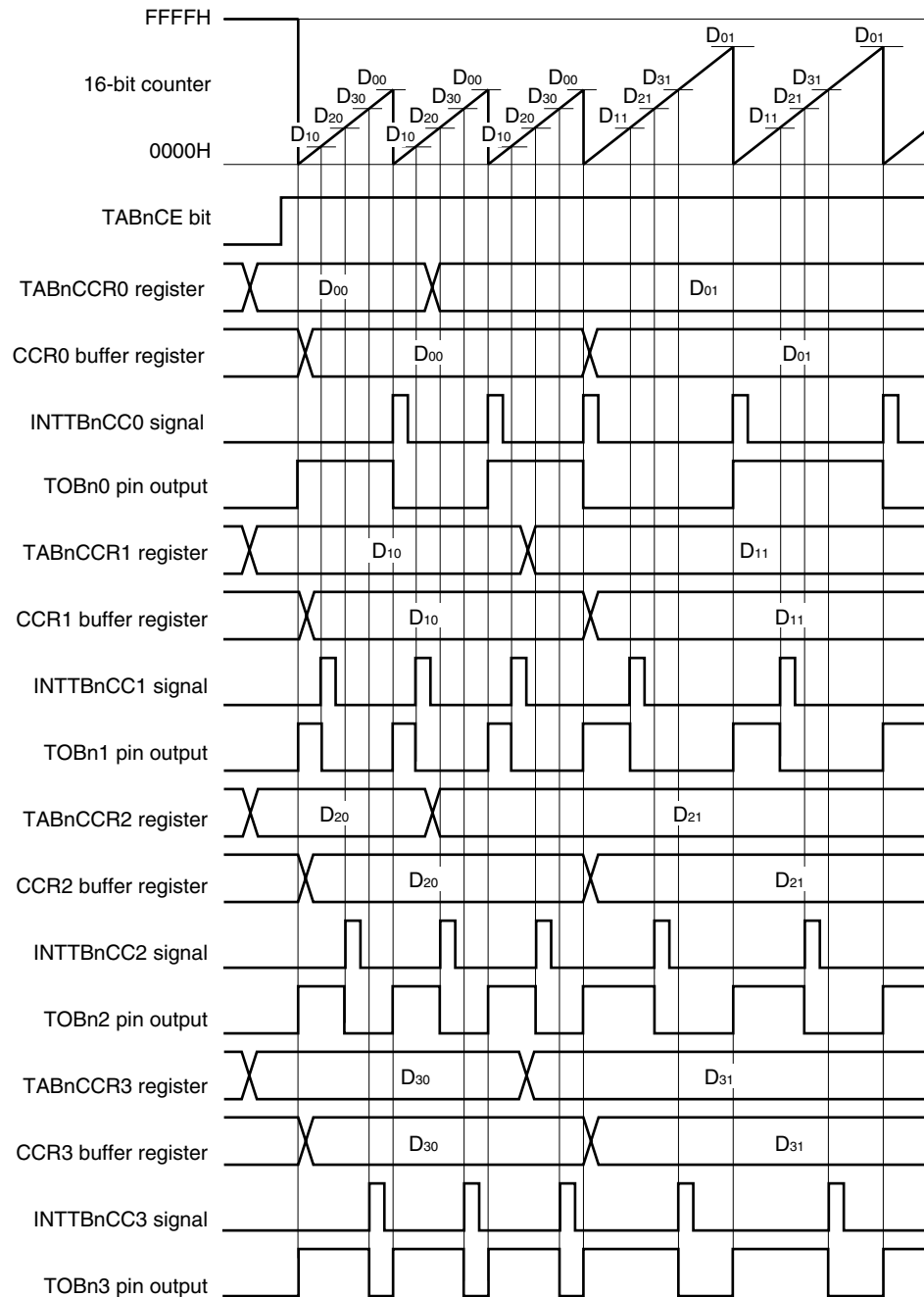
Remark n = 0, 1

(b) Pulse width measurement with capture register

When pulse width measurement is performed with the TABnCCRa register used as a capture register, software processing is necessary for reading the capture register each time the INTTBnCCa signal has been detected and for calculating an interval.

(1) 16-bit counter

This 16-bit counter can count internal clocks or external events.

The count value of this counter can be read by using the TTnCNT register.

When the TTnCTL0.TTnCE bit = 0, the value of the 16-bit counter is FFFFH. If the TTnCNT register is read at this time, 0000H is read.

Reset sets the TTnCE bit to 0.

(2) CCR0 buffer register
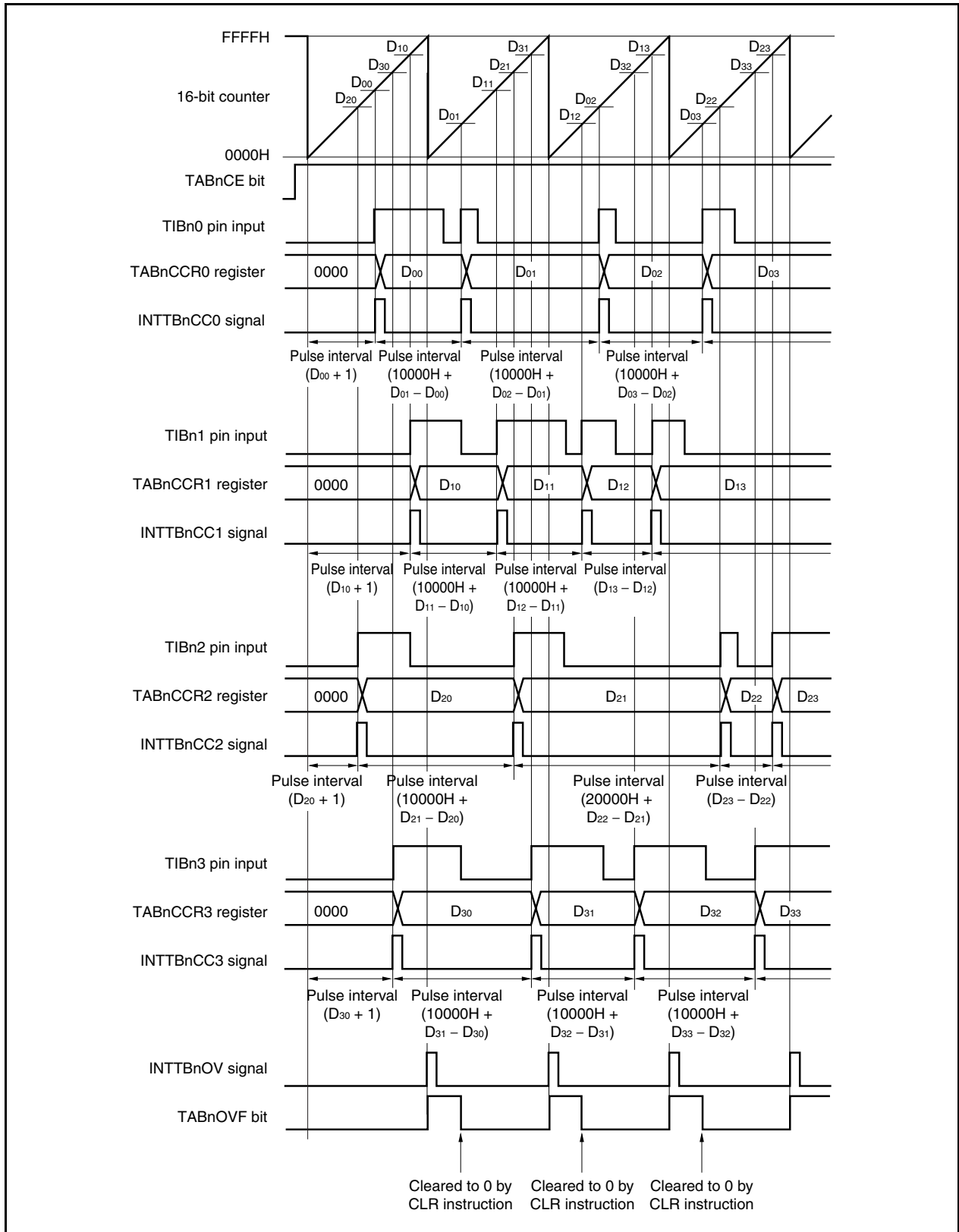
This is a 16-bit compare register that compares the count value of the 16-bit counter.

When the TTnCCR0 register is used as a compare register, the value written to the TTnCCR0 register is transferred to the CCR0 buffer register. When the count value of the 16-bit counter matches the value of the CCR0 buffer register, a compare match interrupt request signal (INTTTEQCn0) is generated.

The CCR0 buffer register cannot be read or written directly.

The CCR0 buffer register is set to 0000H after reset, and the TTnCCR0 register is set to 0000H.

(3) CCR1 buffer register

This is a 16-bit compare register that compares the count value of the 16-bit counter.

When the TTnCCR1 register is used as a compare register, the value written to the TTnCCR1 register is transferred to the CCR1 buffer register. When the count value of the 16-bit counter matches the value of the CCR1 buffer register, a compare match interrupt request signal (INTTTEQCn1) is generated.

The CCR1 buffer register cannot be read or written directly.

The CCR1 buffer register is set to 0000H after reset, and the TTnCCR1 register is set to 0000H.

(4) Edge detector

This circuit detects the valid edges input to the TIT00 (V850E/IG3 only), TIT01 (V850E/IG3 only), TIT10, TIT11, EVTT0 (V850E/IG3 only), EVTT1, TENC00 (V850E/IG3 only), TENC01 (V850E/IG3 only), TENC10, TENC11, TECR0 (V850E/IG3 only), and TECR1 pins. No edge, rising edge, falling edge, or both the rising and falling edges can be selected as the valid edge by using the TTmIOC1, TTmIOC2, and TTmIOC3 registers.

(5) Output controller

This circuit controls the output of the TOT00 (V850E/IG3 only), TOT01 (V850E/IG3 only), TOT10, and TOT11 pins. The output controller is controlled by the TTmIOC0 registers.

(6) Selector

This selector selects the count clock for the 16-bit counter. Eight types of internal clocks or an external event can be selected as the count clock.

(7) Counter control

The count operation is controlled by the timer mode selected by the TTnCTL1 register.

8.4 Registers

(1) TMTn control register 0 (TTnCTL0)

The TTnCTL0 register is an 8-bit register that controls the operation of TMTn.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

The same value can always be written to the TTnCTL0 register by software.

After reset: 00H   R/W   Address: TT0CTL0 FFFFF580H, TT1CTL0 FFFFF5C0H

	<7>	6	5	4	3	2	1	0
TTnCTL0	TTnCE	0	0	0	0	TTnCKS2	TTnCKS1	TTnCKS0

(n = 0, 1)

TTnCE	TMTn operation control
0	TMTn operation disabled (TMTn reset asynchronously[Note])
1	TMTn operation enabled. TMTn operation start

TTnCKS2	TTnCKS1	TTnCKS0	Internal count clock selection
0	0	0	$f_{XX}/2$
0	0	1	$f_{XX}/4$
0	1	0	$f_{XX}/8$
0	1	1	$f_{XX}/16$
1	0	0	$f_{XX}/64$
1	0	1	$f_{XX}/256$
1	1	0	$f_{XX}/1024$
1	1	1	$f_{XX}/2048$

Note The TTnOPT0.TTnOVF bit and the 16-bit counter are reset simultaneously. Moreover, timer outputs (TOT00 (V850E/IG3 only), TOT01 (V850E/IG3 only), TOT10, and TOT11 pins) are reset to the TTmIOC0 register set status at the same time as the 16-bit counter is reset (V850E/IF3: m = 1, V850E/IG3: m = 0, 1).

Cautions 1. **Set the TTnCKS2 to TTnCKS0 bits when the TTnCE bit = 0.**
When the value of the TTnCE bit is changed from 0 to 1, the TTnCKS2 to TTnCKS0 bits can be set simultaneously.
    2. **Be sure to set bits 3 to 6 to "0".**

Remark f_{XX}: Peripheral clock

(2) Anytime write and batch write

The TTnCCR0 and TTnCCR1 registers in TMTn can be rewritten during timer operation (TTnCTL0.TTnCE bit = 1), but the write method (anytime write, batch write) of the CCR0 and CCR1 buffer registers differs depending on the mode.

(a) Anytime write

In this mode, data is transferred at any time from the TTnCCR0 and TTnCCR1 registers to the CCR0 and CCR1 buffer registers during timer operation (n = 0, 1).

Figure 8-3. Flowchart of Basic Operation for Anytime Write

Note The 16-bit counter is not cleared upon a match between the 16-bit counter value and the CCR1 buffer register value. It is cleared upon a match between the 16-bit counter value and the CCR0 buffer register value.

Remarks 1. The above flowchart illustrates an example of the operation in the interval timer mode.

2. n = 0, 1

a = 0, 1
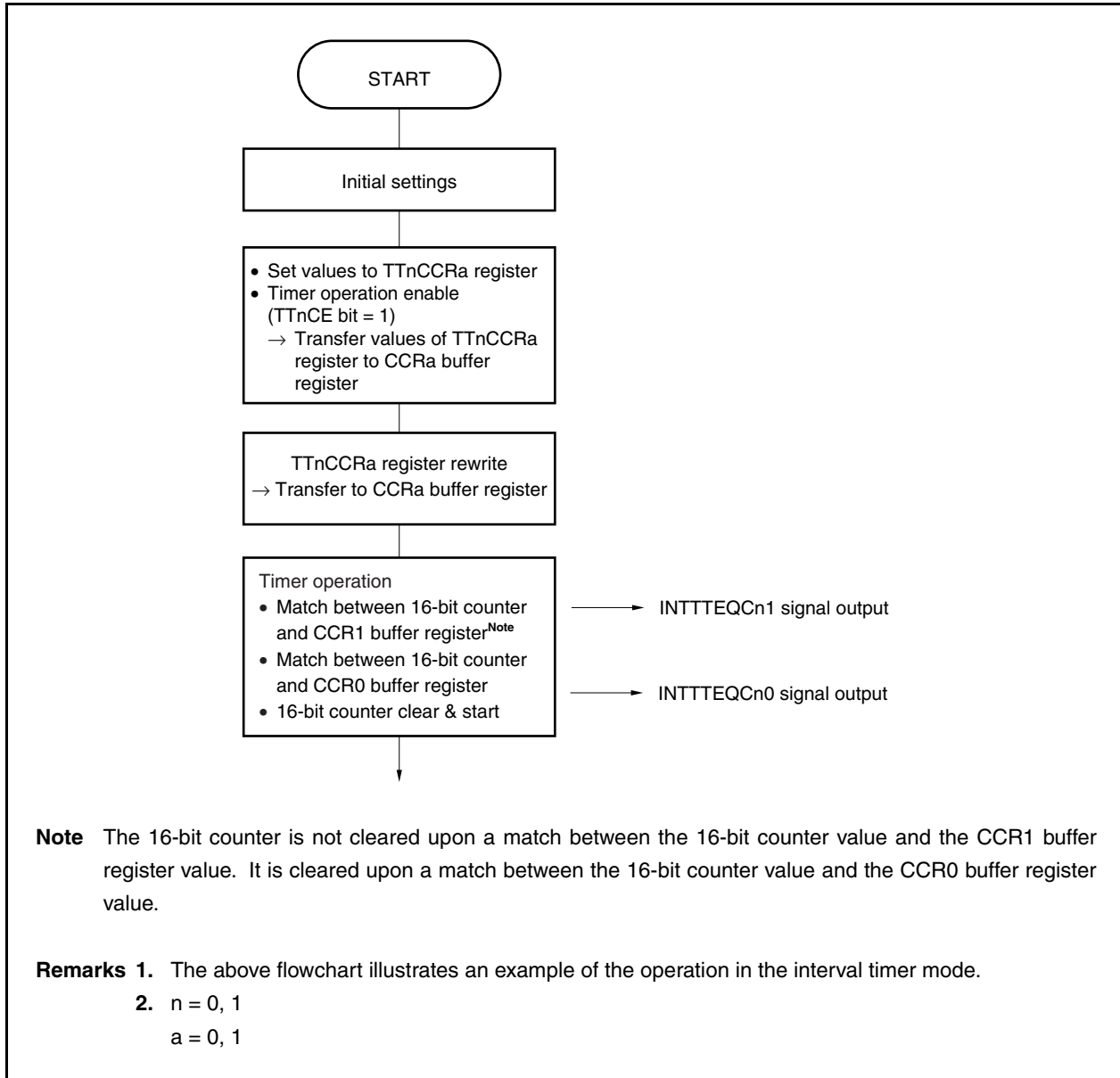
When the TTnCCR1 register is set to the same value as the TTnCCR0 register, the INTTTEQCn0 signal is generated at the same timing as the INTTTEQCn1 signal and the TOTm1 pin output is inverted. In other words, a PWM waveform with a duty factor of 50% can be output from the TOTm1 pin.

The following shows the operation when the TTnCCR1 register is set to other than the value set in the TTnCCR0 register.

If the set value of the TTnCCR1 register is less than the set value of the TTnCCR0 register, the INTTTEQCn1 signal is generated once per cycle. At the same time, the output of the TOTm1 pin is inverted.

The TOTm1 pin outputs a PWM waveform with a duty factor of 50% after outputting a short-width pulse.

Figure 8-12. Timing Chart When $D_{01} \geq D_{11}$
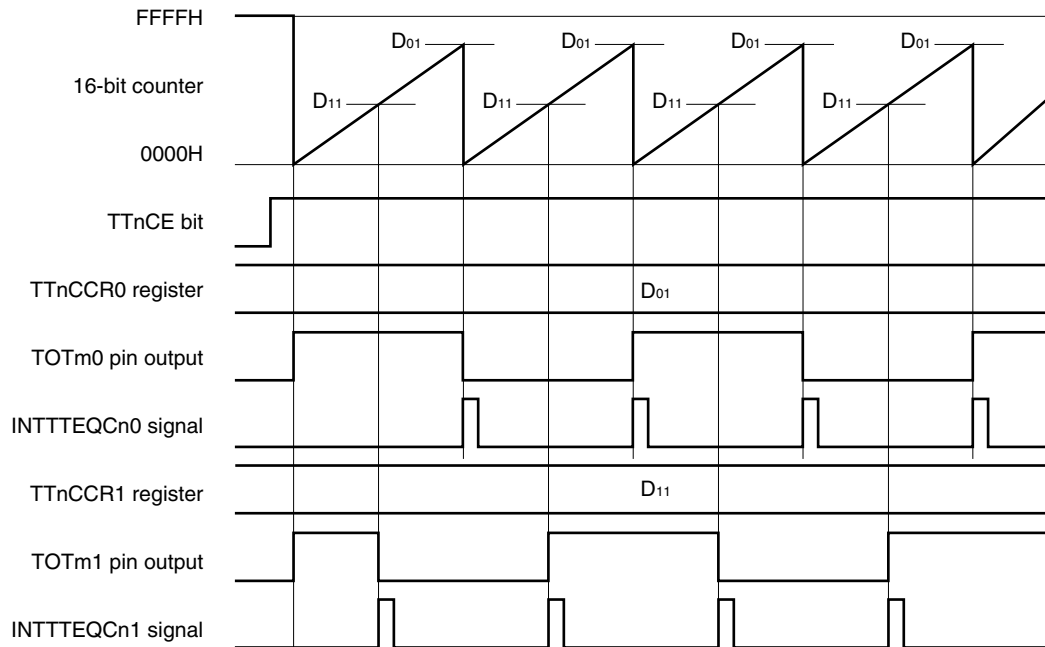
Remark V850E/IF3: n = 0, 1, m = 1
V850E/IG3: n = 0, 1, m = 0, 1

Figure 12-11. Relationship Between Analog Input Voltage and A/D Conversion Results
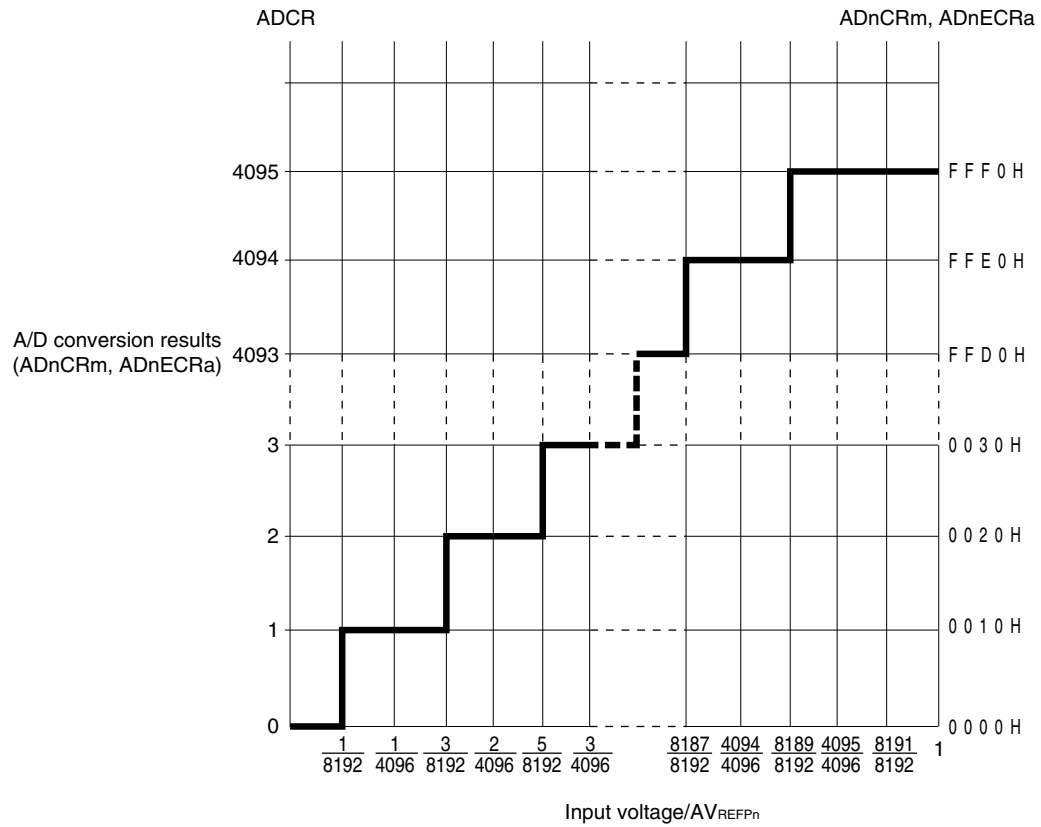
Remark A/D converter 0: n = 0, m = 0 to 15, k = 0 to 5, a = 0 to 4

A/D converter 1: n = 1, m = 0 to 15, k = 0 to 7, a = 0 to 4

CHAPTER 14 ASYNCHRONOUS SERIAL INTERFACE A (UARTA)

14.1 Mode Switching Between UARTA and Other Serial Interface

14.1.1 Mode switching between UARTA0 and CSIB0

In the V850E/IF3 and V850E/IG3, UARTA0 and CSIB0 function alternately, and these pins cannot be used at the same time. To switch between UARTA0 and CSIB0, the PMC4, PFC4, and PFCE4 registers must be set in advance.

Caution **The operations related to transmission and reception of UARTA0 or CSIB0 are not guaranteed if the mode is switched during transmission or reception. Be sure to disable the unit that is not used.**

Figure 14-1. Mode Switch Settings of UARTA0 and CSIB0

After reset: 00H R/W Address: FFFFF448H

	7	6	5	4	3	2	1	0
PMC4	PMC47	PMC46	PMC45	PMC44	PMC43	PMC42	PMC41	PMC40

After reset: 00H R/W Address: FFFFF468H

	7	6	5	4	3	2	1	0
PFC4	PFC47	PFC46	PFC45	PFC44	PFC43	PFC42	PFC41	PFC40

After reset: 00H R/W Address: FFFFF708H

	7	6	5	4	3	2	1	0
PFCE4	PFCE47	PFCE46	PFCE45	PFCE44	PFCE43	PFCE42	PFCE41	PFCE40

PMC42	PFCE42	PFC42	Specification of alternate function of P42 pin
0	×	×	I/O port
1	0	0	$\overline{SCKB0}$ I/O
1	0	1	INTP13 input
1	1	0	Setting prohibited
1	1	1	Setting prohibited

PMC41	PFCE41	PFC41	Specification of alternate function of P41 pin
0	×	×	I/O port
1	0	0	SOB0 output
1	0	1	TXDA0 output
1	1	0	Setting prohibited
1	1	1	Setting prohibited

PMC40	PFC40	Specification of alternate function of P40 pin
0	×	I/O port
1	0	SIB0 input
1	1	RXDA0 input

Remark × = don't care

(2) Operation timing
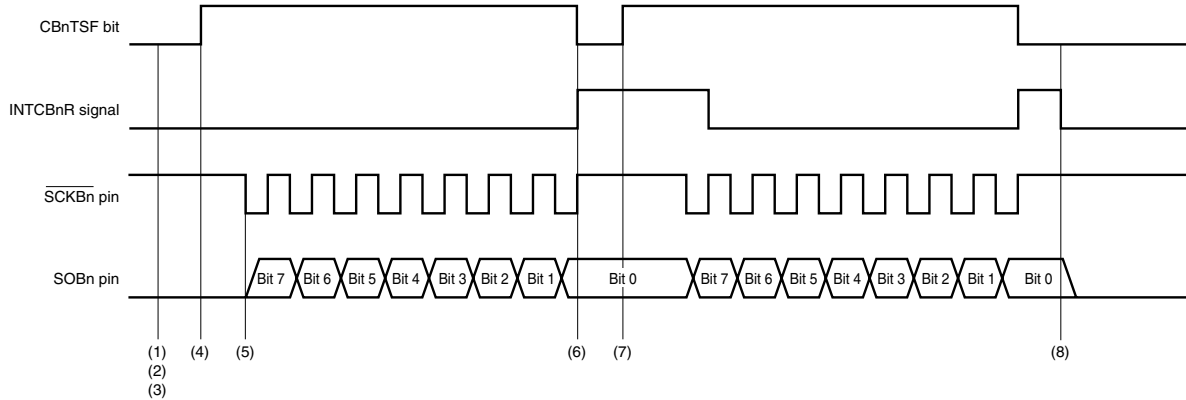
(1) Write 07H to the CBnCTL1 register, and select communication type 1, communication clock (f_{CCLK}) = external clock ($\overline{SCKBn}$), and slave mode.

(2) Write 00H to the CBnCTL2 register, and set the transfer data length to 8 bits.

(3) Write C1H to the CBnCTL0 register, and select the transmission mode and MSB first at the same time as enabling the operation of the communication clock (f_{CCLK}).

(4) The CBnSTR.CBnTSF bit is set to 1 by writing the transmit data to the CBnTX register, and the device waits for a serial clock input.

(5) When a serial clock is input, output the transmit data from the SOBn pin in synchronization with the serial clock.

(6) When transmission of the transfer data length set with the CBnCTL2 register is completed, stop the serial clock input and transmit data output, generate the reception end interrupt request signal (INTCBnR) at the last edge of the serial clock, and clear the CBnTSF bit to 0.

(7) To continue transmission, write the transmit data to the CBnTX register again after the INTCBnR signal is generated, and wait for a serial clock input.

(8) To end transmission, write the CBnCTL0.CBnPWR bit = 0 and the CBnCTL0.CBnTXE bit = 0.

Remark n = 0 to 2

17.3 Configuration

I²C includes the following hardware.

Table 17-1. Configuration of I²C

Item	Configuration
Registers	IIC shift register 0 (IIC0) Slave address register 0 (SVA0)
Control registers	IIC control register 0 (IICC0) IIC status register 0 (IICS0) IIC flag register 0 (IICF0) IIC clock select register 0 (IICCL0) IIC function expansion register 0 (IICX0) IICOPS clock select register (IICOCKS)

(1) IIC shift register 0 (IIC0)

The IIC0 register is used to convert 8-bit serial data to 8-bit parallel data and to convert 8-bit parallel data to 8-bit serial data. The IIC0 register can be used for both transmission and reception.

Write and read operations to the IIC0 register are used to control the actual transmit and receive operations.

The IIC0 register can be read or written in 8-bit units.

Reset sets IIC0 to 00H.

(2) Slave address register 0 (SVA0)

The SVA0 register sets local addresses when in slave mode.

The SVA0 register can be read or written in 8-bit units.

Reset sets SVA0 to 00H.

(3) SO latch

The SO latch is used to retain the SDA pin's output level.

(4) Wakeup controller

This circuit generates an interrupt request signal (INTIIC) when the address received by this register matches the address value set to the SVA0 register or when an extension code is received.

(5) Prescaler

This selects the sampling clock to be used.

(6) Serial clock counter

This counter counts the serial clocks that are output and the serial clocks that are input during transmit/receive operations and is used to verify that 8-bit data was sent or received.
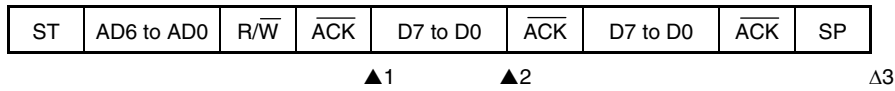
(7) Interrupt request signal generator

This circuit controls the generation of interrupt request signals (INTIIC).

An I²C interrupt is generated following either of two triggers.

- Falling of the eighth or ninth clock of the serial clock (set by IICC0.WTIM0 bit)
- Interrupt request generated when a stop condition is detected (set by IICC0.SPIE0 bit)

(3) When arbitration loss occurs during data transfer

<1> When IICC0.WTIM0 bit = 0

ST	AD6 to AD0	R/$\overline{\text{W}}$	$\overline{\text{ACK}}$	D7 to D0	$\overline{\text{ACK}}$	D7 to D0	$\overline{\text{ACK}}$	SP

▲1   ▲2   △3

▲1: IICS0 register = 10001110B

▲2: IICS0 register = 01000000B

△3: IICS0 register = 00000001B

Remark ▲: Always generated

△: Generated only when SPIE0 bit = 1

<2> When WTIM0 bit = 1

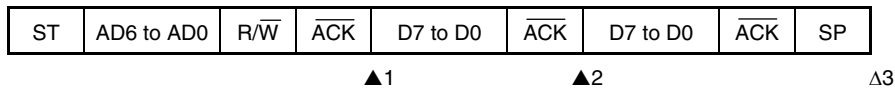| ST	AD6 to AD0	R/$\overline{\text{W}}$	$\overline{\text{ACK}}$	D7 to D0	$\overline{\text{ACK}}$	D7 to D0	$\overline{\text{ACK}}$	SP

▲1   ▲2   △3

▲1: IICS0 register = 10001110B

▲2: IICS0 register = 01000100B

△3: IICS0 register = 00000001B

Remark ▲: Always generated

△: Generated only when SPIE0 bit = 1

(2) Address wait control register (AWC)

This register is used to secure the setup and hold time for the address latch.

The AWC register can set an address setup wait state or address hold wait state that is to be inserted in each bus cycle. The address setup wait state is inserted before T1 state and the address hold wait state is inserted after T1 state.
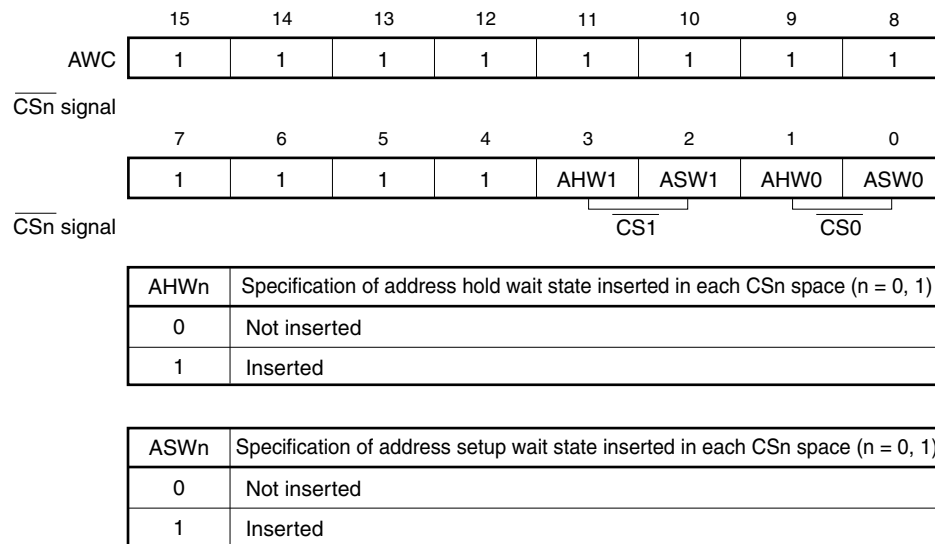
Address setup wait state and address hold wait state insertion can be set with the AWC register for each CS space.

This register can be read or written in 16-bit units.

Reset sets this register to FFFFH.

Cautions 1. The internal ROM, internal RAM, and on-chip peripheral I/O areas are not subject to address setup wait state and address hold wait state insertion.

2. During address setup wait state and address hold wait state, the $\overline{\text{WAIT}}$ pin-based external wait function is disabled.

3. Write to the AWC register after reset, and then do not change the set values. Also, when changing the initial values of the AWC register, do not access an external memory area until the settings are complete.

After reset: FFFFH   R/W   Address: FFFFF488H

	15	14	13	12	11	10	9	8
AWC	1	1	1	1	1	1	1	1

$\overline{\text{CSn}}$ signal

	7	6	5	4	3	2	1	0
	1	1	1	1	AHW1	ASW1	AHW0	ASW0

$\overline{\text{CSn}}$ signal $\overline{\text{CS1}}$ $\overline{\text{CS0}}$

AHWn	Specification of address hold wait state inserted in each CSn space (n = 0, 1)
0	Not inserted
1	Inserted

ASWn	Specification of address setup wait state inserted in each CSn space (n = 0, 1)
0	Not inserted
1	Inserted

Caution   Be sure to set bits 4 to 15 to "1". If they are set to "0", the operation is not guaranteed.

21.4 IDLE Mode

21.4.1 Setting and operation status

The IDLE mode is set by clearing (0) the PSMR.PSM0 bit and setting (1) the PSC.STB bit in the normal operation mode.

In the IDLE mode, the clock generator and PLL continue operation but clock supply to the CPU and other on-chip peripheral functions stops.

As a result, program execution stops and the contents of the internal RAM before the IDLE mode was set are retained. The CPU and other on-chip peripheral functions stop operating. However, the on-chip peripheral functions that can operate with an external clock continue operating.

Table 21-5 shows the operation status in the IDLE mode.

The IDLE mode can reduce the power consumption more than the HALT mode because it stops the operation of the on-chip peripheral functions. The clock generator and PLL do not stop, so the normal operation mode can be restored without waiting for the oscillation stabilization time after the IDLE mode has been released, in the same manner as when the HALT mode is released.

Caution   Insert five or more NOP instructions after the instruction that stores data in the PSC register to set the IDLE mode.

21.4.2 Releasing IDLE mode

The IDLE mode is released by an unmasked external interrupt request signal (INTP00, INTP01, INTP02 to INTP07 (V850E/IG3 only), INTP08 to INTP13, INTP17, INTP18, INTADT0, or INTADT1 pin input), an unmasked internal interrupt request signal (CSIB-related interrupt request signal in the slave mode) from the peripheral functions operable in the IDLE mode, or a reset signal ($\overline{\text{RESET}}$ pin input, reset signal (LVIRES) generation by low-voltage detector (LVI), or reset signal (POCRES) generation by power-on-clear circuit (POC)).

After the IDLE mode has been released, the normal operation mode is restored.

(1) Releasing IDLE mode by unmasked maskable interrupt request signal

The IDLE mode is released by an unmasked maskable interrupt request signal, regardless of the priority of the interrupt request. If the IDLE mode is set in an interrupt servicing routine, however, an interrupt request that is issued later is processed as follows.

Caution   When PSC.INTM bit = 1, the IDLE mode cannot be released by the unmasked maskable interrupt request signal.

(a) If an interrupt request with a priority lower than or same as the interrupt request signal currently being serviced is generated, the IDLE mode is released, but the newly generated interrupt is not acknowledged. The interrupt request signal itself is retained. Therefore, execution starts at the next instruction after the IDLE instruction.

(b) If an interrupt request signal with a priority higher than that of the interrupt request signal currently being serviced is issued (including a non-maskable interrupt request signal), the IDLE mode is released and that interrupt request signal is acknowledged. Therefore, execution branches to the handler address.