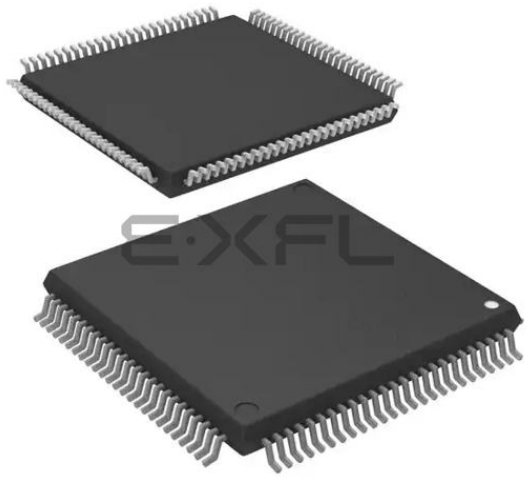
Renesas Electronics America Inc - UPD70F3454F1(R)-DA9-A Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CSI, EBI/EMI, I²C, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	64
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 10x12b, 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	161-LFBGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3454f1-r-da9-a

1.2.2 Application fields (V850E/IF3)

- Consumer equipment (such as inverter air conditioners, washing machines, driers, refrigerators, etc.)
- Industrial equipment (such as motor control, general-purpose inverters, etc.)

1.2.3 Ordering information (V850E/IF3)

Part Number	Package	Internal ROM
μPD70F3451GC-UBT-A	80-pin plastic LQFP (14 × 14)	Flash memory (128 KB)
μPD70F3452GC-UBT-A	80-pin plastic LQFP (14 × 14)	Flash memory (256 KB)

Remark The V850E/IF3 microcontrollers are lead-free products.

(d) Port 0 function control register (PFC0)

After reset: 00H R/W Address: FFFFF460H

	7	6	5	4	3	2	1	0
PFC0	PFC07[Note]	PFC06[Note]	PFC05[Note]	PFC04[Note]	PFC03[Note]	PFC02[Note]	PFC01	PFC00

Note Valid only in the V850E/IG3.
With the V850E/IF3, be sure to set these bits to 0.

Remark For the specifications of alternate functions, see **4.3.1 (1) (f) Settings of alternate functions of port 0**.

(e) Port 0 function control expansion register (PFCE0)

After reset: 00H R/W Address: FFFFF700H

	7	6	5	4	3	2	1	0
PFCE0	0	PFCE06[Note]	PFCE05[Note]	PFCE04[Note]	PFCE03[Note]	PFCE02[Note]	PFCE01	PFCE00

Note Valid only in the V850E/IG3.
With the V850E/IF3, be sure to set these bits to 0.

Remark For the specifications of alternate functions, see **4.3.1 (1) (f) Settings of alternate functions of port 0**.

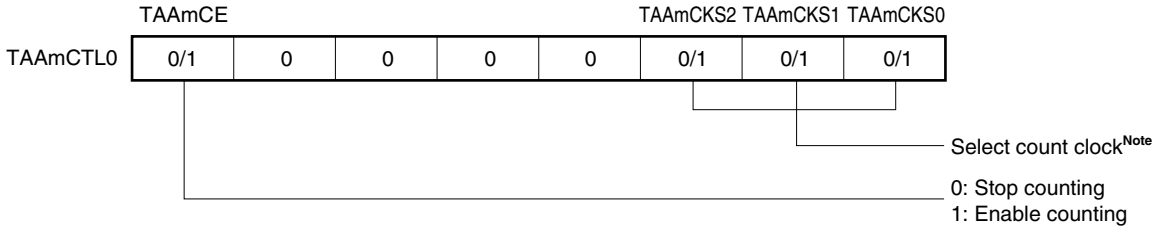
(e) Interrupt operation

TAAn generates the following three types of interrupt request signals.

- INTTAnCC0 interrupt: This signal functions as a match interrupt request signal of the CCR0 buffer register and as a capture interrupt request signal to the TAAnCCR0 register.
- INTTAnCC1 interrupt: This signal functions as a match interrupt request signal of the CCR1 buffer register and as a capture interrupt request signal to the TAAnCCR1 register.
- INTTAnOV interrupt: This signal functions as an overflow interrupt request signal.

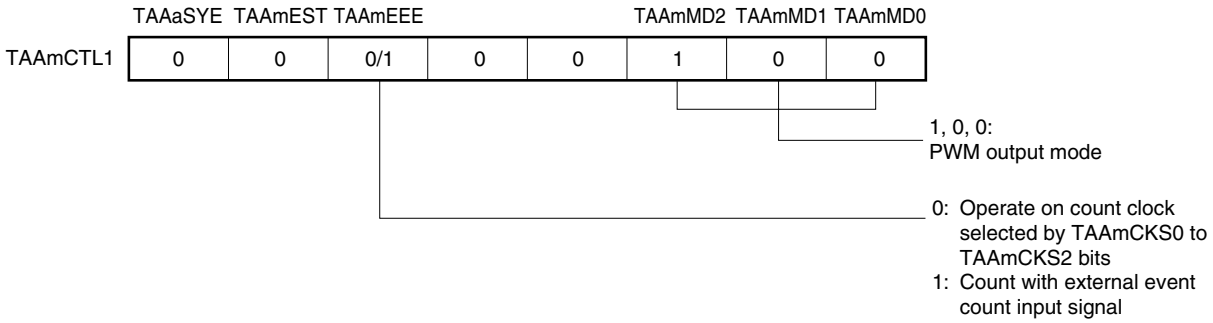
Figure 6-34. Setting of Registers in PWM Output Mode (1/2)

(a) TAAm control register 0 (TAAmCTL0)

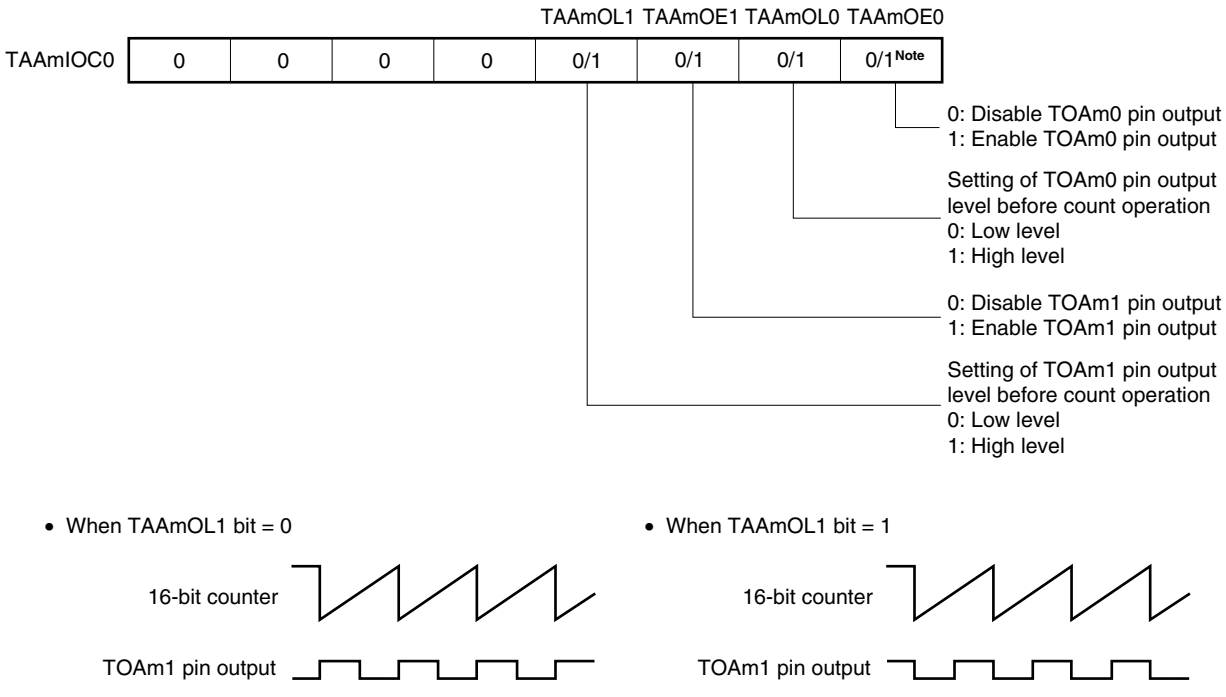


Note The setting is invalid when the TAAmCTL1.TAAmEEE bit = 1.

(b) TAAm control register 1 (TAAmCTL1)



(c) TAAm I/O control register 0 (TAAmIOC0)



Note Clear this bit to 0 when the TOAm0 pin is not used in the PWM output mode.

(a) Function as compare register

The TABnCCR0 register can be rewritten even when the TABnCTL0.TABnCE bit = 1.

The set value of the TABnCCR0 register is transferred to the CCR0 buffer register. When the value of the 16-bit counter matches the value of the CCR0 buffer register, a compare match interrupt request signal (INTTBnCC0) is generated. If TOBn0 pin output is enabled at this time, the output of the TOBn0 pin is inverted.

When the TABnCCR0 register is used as a cycle register in the interval timer mode, external event count mode, external trigger pulse output mode, one-shot pulse output mode, or PWM output mode, the value of the 16-bit counter is cleared (0000H) if its count value matches the value of the CCR0 buffer register.

The compare register is not cleared by setting the TABnCTL0.TABnCE bit to 0.

(b) Function as capture register

When the TABnCCR0 register is used as a capture register in the free-running timer mode, the count value of the 16-bit counter is stored in the TABnCCR0 register if the valid edge of the capture trigger input pin (TIBn0 pin) is detected. In the pulse-width measurement mode, the count value of the 16-bit counter is stored in the TABnCCR0 register and the 16-bit counter is cleared (0000H) if the valid edge of the capture trigger input pin (TIBn0 pin) is detected.

Even if the capture operation and reading the TABnCCR0 register conflict, the correct value of the TABnCCR0 register can be read.

The capture register is cleared by setting the TABnCTL0.TABnCE bit = 0.

The following table shows the functions of the capture/compare register in each mode, and how to write data to the compare register.

Table 7-2. Function of Capture/Compare Register in Each Mode and How to Write Compare Register

Operation Mode	Capture/Compare Register	How to Write Compare Register
Interval timer	Compare register	Anytime write
External event counter	Compare register	Anytime write
External trigger pulse output	Compare register	Batch write[Note]
One-shot pulse output	Compare register	Anytime write
PWM output	Compare register	Batch write[Note]
Free-running timer	Capture/compare register	Anytime write
Pulse width measurement	Capture register	None

Note Writing to the TABnCCR1 register is the trigger.

Remark For anytime write and batch write, see **7.6 (2) Anytime write and batch write**.

Figure 7-15. Register Setting for Operation in External Event Count Mode (2/2)

(f) TABn capture/compare registers 1 to 3 (TABnCCR1 to TABnCCR3)

The TABnCCR1 to TABnCCR3 registers are not used in the external event count mode. However, the set value of the TABnCCR1 to TABnCCR3 registers are transferred to the CCR1 to CCR3 buffer registers. When the count value of the 16-bit counter matches the value of the CCR1 to CCR3 buffer registers, compare match interrupt request signals (INTTBnCC1 to INTTBnCC3) are generated.

When the TABnCCR1 to TABnCCR3 registers are not used, it is recommended to set their values to FFFFH. Also mask the registers by the interrupt mask flags (TABnCCIC1.TABnCCMK1 to TABnCCIC3.TABnCCMK3).

Caution Set the TABnIOC0 register to 00H.

Remarks 1. TABn I/O control register 1 (TABnIOC1) and TABn option register 0 (TABnOPT0) are not used in the external event count mode.

2. n = 0, 1

Figure 8-9. Register Setting for Interval Timer Mode Operation (2/2)

(d) TMTn counter read buffer register (TTnCNT)

By reading the TTnCNT register, the count value of the 16-bit counter can be read.

(e) TMTn capture/compare register 0 (TTnCCR0)

If the TTnCCR0 register is set to D_0, the interval is as follows.

Interval = $(D_0 + 1) \times$ Count clock cycle

(f) TMTn capture/compare register 1 (TTnCCR1)

The TTnCCR1 register is not used in the interval timer mode. However, the set value of the TTnCCR1 register is transferred to the CCR1 buffer register. When the count value of the 16-bit counter matches the value of the CCR1 buffer register, the TOTm1 pin output is inverted and a compare match interrupt request signal (INTTTEQCn1) is generated.

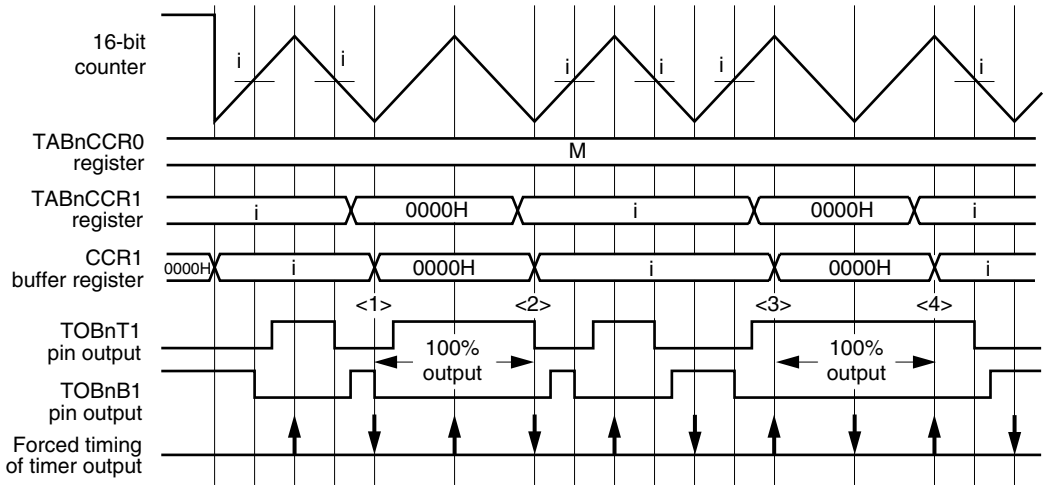
By setting this register to the same value as the value set in the TTnCCR0 register, a PWM waveform with a duty factor of 50% can be output from the TOTm1 pin.

When the TTnCCR1 register is not used, it is recommended to set its value to FFFFH. Also mask the register by the interrupt mask flag (TTnCCIC1.TTnCCMK1).

Remarks 1. TMTm control register 2 (TTmCTL2), TMTm I/O control register 1 (TTmIOC1), TMTm I/O control register 2 (TTmIOC2), TMTm I/O control register 3 (TTmIOC3), TMTn option register 0 (TTnOPT0), TMTm option register 1 (TTmOPT1), TMTm capture input select register (TTISLm), and TMTm counter write register (TTmTCW) are not used in the interval timer mode.

2. V850E/IF3: m = 1, n = 0, 1
V850E/IG3: m = 0, 1, n = 0, 1

Figure 10-10. 100% PWM Output Waveform (With Dead Time)



<1> 100% output is selected by the valley interrupt (with a match with the 16-bit counter).
The valley interrupt forcibly lowers the timer output, but raising the timer output takes precedence when the value of the TABnCCRm register matches the value of the 16-bit counter. As a result, the 100% output is produced.

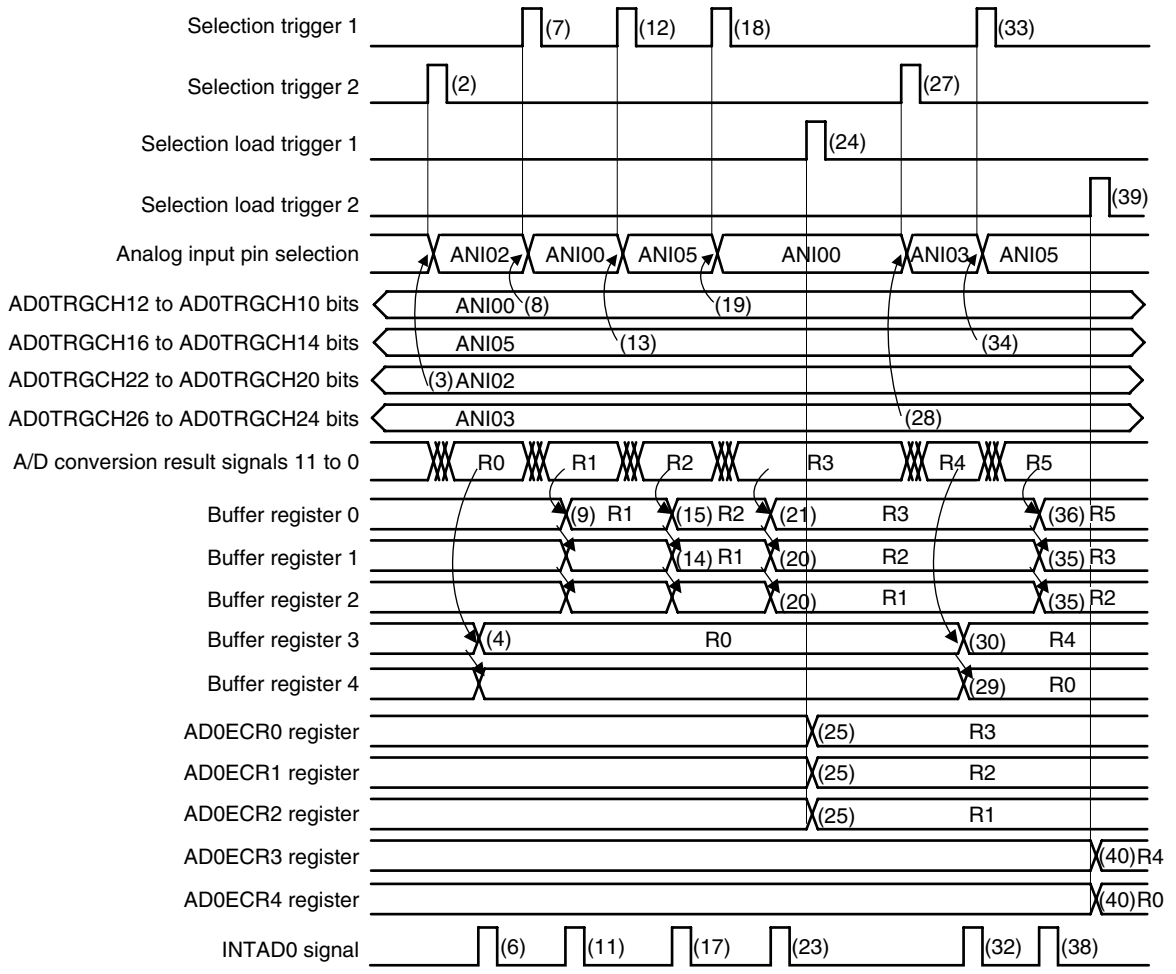
<2> 100% output is canceled by the valley interrupt (without a match with the 16-bit counter).
The valley interrupt forcibly lowers the timer output. This cancels the 100% output.

<3> 100% output is selected by the crest interrupt (without a match with the 16-bit counter).
The crest interrupt forcibly raises the timer output. This produces the 100% output.

<4> 100% output is canceled by the crest interrupt (without a match with the 16-bit counter).
The crest interrupt forcibly raises the timer output. This cancels the 100% output.

Remark ↑ means forced raising and ↓ means forced lowering.

Figure 12-22. Example of Operation in Extension Buffer Mode: A/D Converter 0 (1/2)

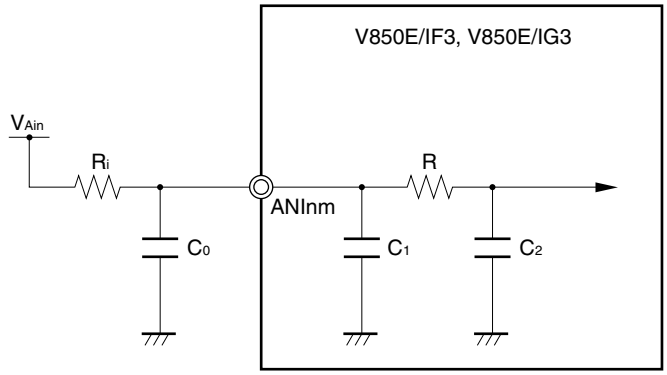


Remarks 1. Buffer registers 0 to 4: A/Dn conversion result extension buffer registers 0 to 4

2. R0 to R6: Conversion result

3. n = 0, 1

An example of calculating an overall error of A/D converters 0 and 1 is shown below.



<R>

fXX (MHz)	A/D conversion time (μs)	Sampling (μs)	R (kΩ)	C1 (pF)	C2 (pF)	C0 (pF)	Ri (kΩ)	Sampling error (LSB)[Note]
64	2.00 (32/fAD01)	0.78 (12.5/fAD01)	5.1	15	3.9	100	1.0	364.8
						100	0.5	30.4
						100	0.25	0.1 or lower
						100	0.125	0.1 or lower
						50	1.0	62.4
						50	0.5	0.8
						50	0.25	0.1 or lower
						50	0.125	0.1 or lower

Note The error when considering the signal source impedance is “sampling error + overall error”.

Remarks 1. These values are reference values calculated by simulating what happens to C_2 voltage by R_i and C_0 when V_{Ain} is applied from 0 V to 5 V at the same time as sampling start.

2. m = 0 to 5 when n = 0
m = 0 to 7 when n = 1

3. fXX: System clock frequency
fAD01: Basic clock frequency

13.5 Operation in Software Trigger Mode

When the AD2M0.AD2CE bit is set to 1, A/D conversion is started.

When A/D conversion is started, the AD2M0.AD2EF bit = 1 (conversion in progress).

If the AD2M0 and AD2S registers are written during A/D conversion, the conversion is stopped and executed again from the beginning.

(1) Operation in software trigger continuous select mode

In this mode, one analog input pin (ANI2n) specified by the AD2S register is A/D-converted once. The conversion results are stored in one AD2CRn register. The ANI2n pin and AD2CRn register correspond one to one.

Each time an A/D conversion is executed, an A/D2 conversion end interrupt request signal (INTAD2) is generated and A/D conversion ends. After A/D conversion ends, the conversion is repeated again unless the AD2M0.AD2CE bit is set to 0.

It is not necessary to set (1) the AD2M0.AD2CE bit to restart A/D conversion[Note].

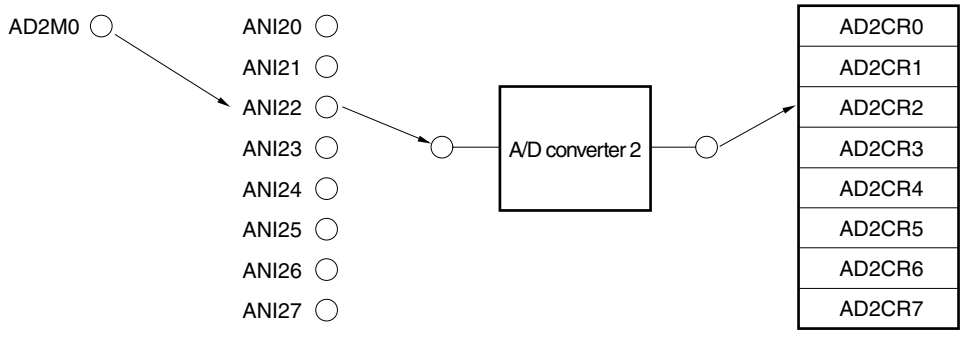
Note In the software trigger continuous select mode, the A/D conversion operation is not stopped unless the AD2M0.AD2CE bit is set to 0. If the AD2CRn register is not read before the next A/D conversion ends, it is overwritten.

This mode is suitable for applications in which the A/D conversion value of one analog input pin is read.

Analog Input Pin	A/D Conversion Result Register
ANI2n	AD2CRn

Remark V850E/IF3: n = 0 to 3
V850E/IG3: n = 0 to 7

Figure 13-8. Operation Example of Software Trigger Continuous Select Mode: V850E/IG3



(1) The AD2CE bit = 1 (enable)
(2) The ANI22 pin is A/D-converted
(3) The conversion result is stored in the AD2CR2 register
(4) The AD2M0.AD2EF bit = 0
(5) The INTAD2 interrupt request signal is generated
(6) Return to (2)
(7) To end the conversion, the AD2CE bit = 0 (stop)

Remark This is an operation example with the following setting.
AD2M0.AD2MD1 and AD2M0.AD2MD0 bits = 00, AD2S.AD2S2 to AD2S.AD2S0 bits = 010

(4) Baud rate

The baud rate is obtained by the following equation.

$$\text{Baud rate} = \frac{f_{UCLK}}{2 \times k} \text{ [bps]}$$

f_{UCLK}: Frequency of base clock selected by the UAnCTL1.UAnCKS3 to UAnCTL1.UAnCKS0 bits

k: Value set using the UAnCTL2.UAnBRS7 to UAnCTL2.UAnBRS0 bits (k = 4, 5, 6, ..., 255)

(5) Baud rate error

The baud rate error is obtained by the following equation.

$$\text{Error (\%)} = \left(\frac{\text{Actual baud rate (baud rate with error)}}{\text{Target baud rate (correct baud rate)}} - 1 \right) \times 100 \text{ [\%]}$$

Cautions 1. The baud rate error during transmission must be within the error tolerance on the receiving side.

2. The baud rate error during reception must satisfy the range indicated in section (7) Allowable baud rate range during reception.

Example Peripheral clock frequency = 32 MHz = 32,000,000 Hz

Set value of UAnCTL1.UAnCKS3 to UAnCTL1.UAnCKS0 bits = 0000B (f_{UCLK} = 16,000,000 Hz)

Set value of UAnCTL2.UAnBRS7 to UAnCTL2.UAnBRS0 bits = 00110100B (k = 52)

Target baud rate = 153,600

Baud rate = 16,000,000/ (2 × 52) = 153,846 [bps]

Error = (153,846/153,600 − 1) × 100

= 0.160 [%]

(2) UARTB status register (UBSTR)

The UBSTR register indicates the transfer status and reception error contents while UARTB is transmitting data.

The status flag that indicates the transfer status during transmission indicates the data retention status of the transmit shift register and transmit data register (the UBTX register in the single mode or transmit FIFO in the FIFO mode). The status flag that indicates a reception error holds its status until it is cleared to 0.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

Caution When the UBCTL0.UBPWR bit or UBCTL0.UBRXE bit is set to 0, or when 0 is written to the UBSTR register, the UBSTR.UBOVF, UBSTR.UBPE, UBSTR.UBFE, and UBSTR.UBOVE bits are cleared to 0.

(1/2)

After reset: 00H R/W Address: FFFFFA44H

	<7>	6	5	4	3	<2>	<1>	<0>
UBSTR	UBTSF	0	0	0	UBOVF	UBPE	UBFE	UBOVE

UBTSF	Transfer status flag
0	• In single mode (UBFIC0.UBMOD bit = 0) Data to be transferred to the transmit shift register and UBTX register does not exist (cleared (0) when UBCTL0.UBPWR bit = 0 or UBCTL0.UBTXE bit = 0). • In FIFO mode (UBFIC0.UBMOD bit = 1) Data to be transferred to the transmit shift register and transmit FIFO does not exist (cleared (0) when UBCTL0.UBPWR bit = 0 or UBCTL0.UBTXE bit = 0).
1	• In single mode (UBFIC0.UBMOD bit = 0) Data to be transferred to the transmit shift register or UBTX register exists (transmission in progress). • In FIFO mode (UBFIC0.UBMOD bit = 1) Data to be transferred to the transmit shift register and transmit FIFO exists (transmission in progress).
The value of the UBTSF bit is reflected after two periods of f_{XX} have elapsed, after the transmit data is written to the UBTX register. Therefore, exercise care when referencing the UBTSF bit after transmit data has been written to the UBTX register.	

UBOVF	Overflow flag
0	Overflow did not occur.
1	Overflow occurred (during reception).
• The UBOVF bit is valid only in the FIFO mode (when UBFIC0.UBMOD bit = 1), and invalid in the single mode (when UBFIC0.UBMOD bit = 0). • If an overflow occurs, the received data is not written to receive FIFO but discarded.	

(3/3)

ACKD0	Detection of $\overline{ACK}$
0	$\overline{ACK}$ was not detected.
1	$\overline{ACK}$ was detected.

Condition for clearing (ACKD0 bit = 0)	Condition for setting (ACKD0 bit = 1)
• When a stop condition is detected • At the rising edge of the next byte's first clock • Cleared by the LREL0 bit = 1 (exit from communications) • When the IICE0 bit changes from 1 to 0 (operation stop) • Reset	• After the SDA pin is set to low level at the rising edge of the SCL pin's ninth clock

STD0	Detection of start condition
0	Start condition was not detected.
1	Start condition was detected. This indicates that the address transfer period is in effect

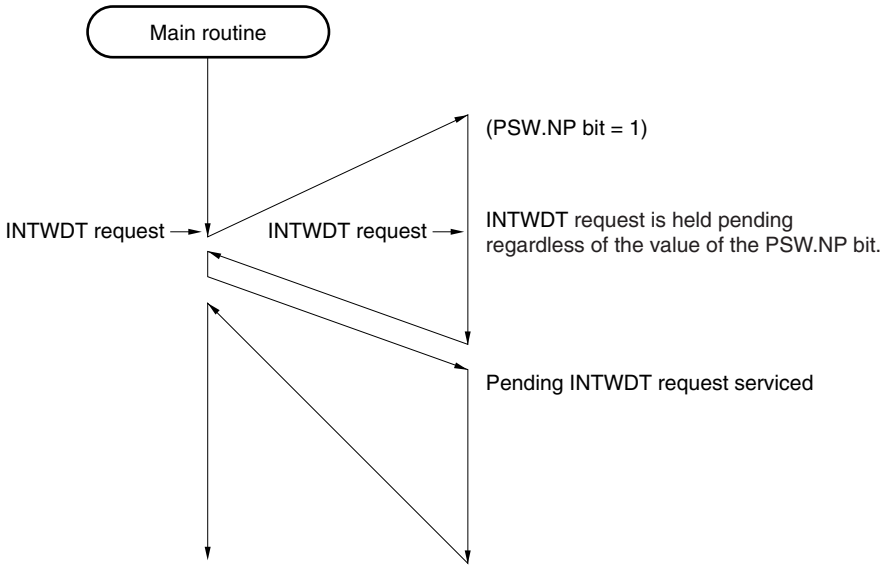
Condition for clearing (STD0 bit = 0)	Condition for setting (STD0 bit = 1)
• When a stop condition is detected • At the rising edge of the next byte's first clock following address transfer • Cleared by the LREL0 bit = 1 (exit from communications) • When the IICE0 bit changes from 1 to 0 (operation stop) • Reset	• When a start condition is detected

SPD0	Detection of stop condition
0	Stop condition was not detected.
1	Stop condition was detected. The master device's communication is terminated and the bus is released.

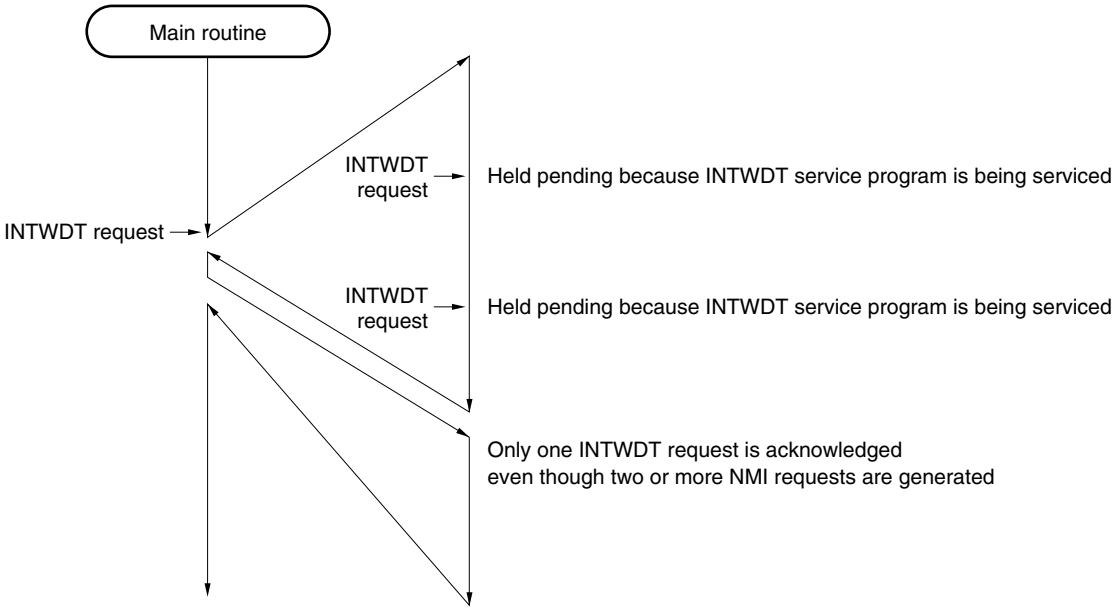
Condition for clearing (SPD0 bit = 0)	Condition for setting (SPD0 bit = 1)
• At the rising edge of the address transfer byte's first clock following setting of this bit and detection of a start condition • When the IICE0 bit changes from 1 to 0 (operation stop) • Reset	• When a stop condition is detected

Figure 20-2. Acknowledging Non-Maskable Interrupt Request

(a) If a new INTWDT request is generated while an INTWDT service program is being executed



(b) If a new INTWDT request is generated twice while an INTWDT service program is being executed



20.5 Software Exception

A software exception is generated when the CPU executes the TRAP instruction, and can always be acknowledged.

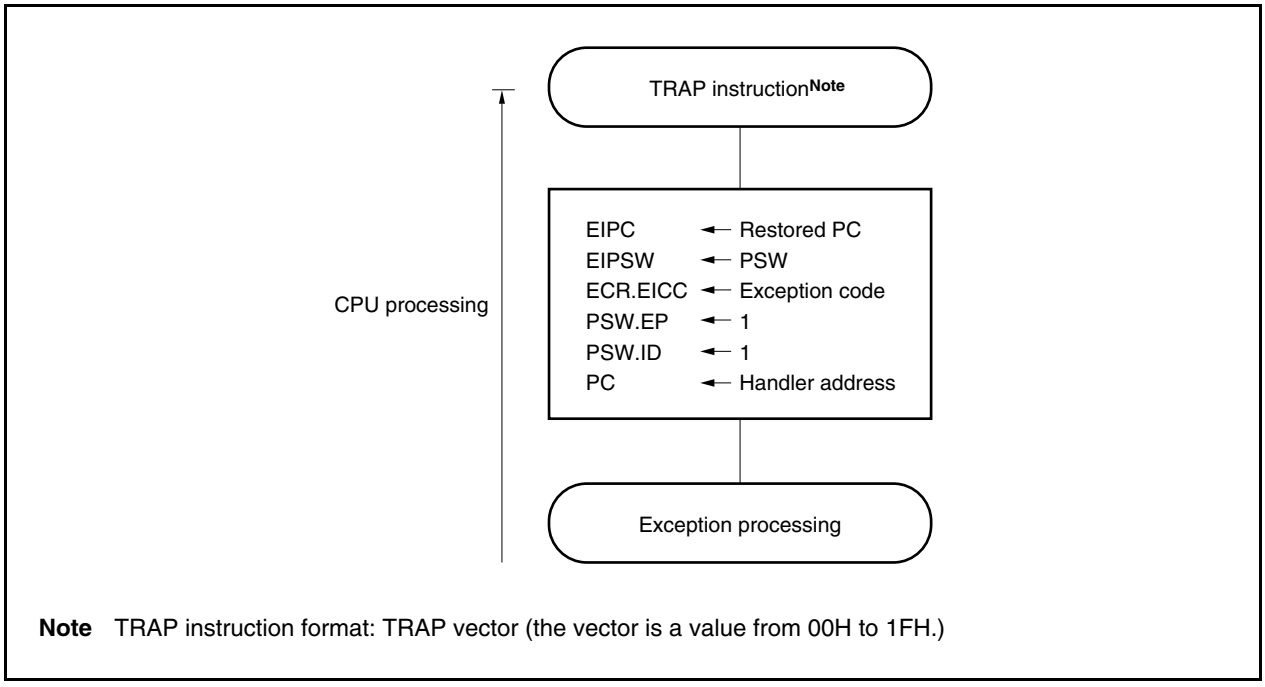
20.5.1 Operation

If a software exception occurs, the CPU performs the following processing, and transfers control to the handler routine.

<1> Saves the restored PC to EIPC.
<2> Saves the current PSW to EIPSW.
<3> Writes an exception code to the lower 16 bits (EICC) of ECR (interrupt source).
<4> Sets the PSW.EP and PSW.ID bits (1).
<5> Sets the handler address (00000040H or 00000050H) corresponding to the software exception to the PC, and transfers control.

The processing of a software exception is shown below.

Figure 20-8. Software Exception Processing



Note TRAP instruction format: TRAP vector (the vector is a value from 00H to 1FH.)

The handler address is determined by the TRAP instruction's operand (vector). If the vector is 00H to 0FH, it becomes 00000040H, and if the vector is 10H to 1FH, it becomes 00000050H.

21.2 Control Registers

(1) Power save control register (PSC)

The PSC register is an 8-bit register that controls the standby function. The STB bit of this register is used to specify the standby mode. This register is a special register (see **3.4.8 Special registers**). This register can be written only by a combination of specific sequences.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

After reset: 00H R/W Address: FFFFF1FEH

	7	6	5	<4>	3	2	<1>	0
PSC	0	0	0	INTM	0	0	STB	0

INTM	Standby mode control[Note 2] by maskable interrupt request (INTxx[Note 1])
0	Standby mode release by INTxx request enabled
1	Standby mode release by INTxx request disabled

STB	Sets operation mode
0	Normal mode
1	Standby mode

Notes 1. For details, see **Table 20-1 Interrupt Source List**.

2. The setting is valid only in the IDLE mode and STOP mode.

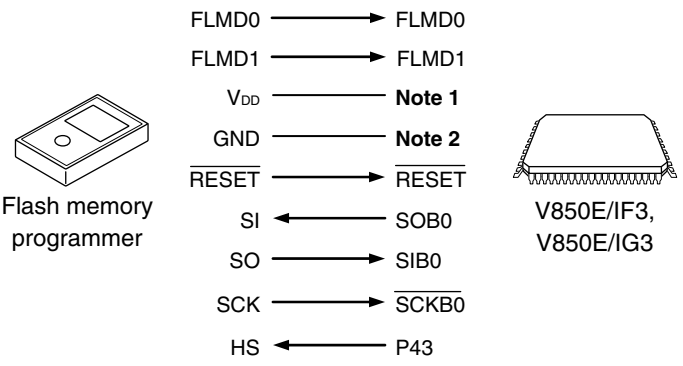
Cautions 1. Be sure to set bits 0, 2, 3, and 5 to 7 to "0".

2. Before setting a standby mode by setting the STB bit to 1, be sure to set the PCC register to 03H and then set the STB bit to 1. Otherwise, the standby mode may not be set or released. After releasing the standby mode, change the value of the PCC register to the desired value.

3. To set the IDLE mode or STOP mode, set the PCC register to 03H, and the PSMR.PSM0 bit in that order and then set the STB bit to 1.

(3) CSIB0 communication method supporting handshake

Transfer rate: Up to 2.5 Mbps (MSB first)



Notes 1. V_{DD0}, V_{DD1}, EV_{DD0}, EV_{DD1}, EV_{DD2} (V850E/IG3 only), AV_{DD0}, AV_{DD1}, AV_{DD2}, AV_{REFP0}, AV_{REFP1}

2. V_{SS0}, V_{SS1}, EV_{SS0}, EV_{SS1}, EV_{SS2} (V850E/IG3 only), AV_{SS0}, AV_{SS1}, AV_{SS2}

Cautions 1. Supply the operating clock of the V850E/IF3 or V850E/IG3 via the oscillator configured on the V850E/IF3 or V850E/IG3 board using a resonator and a capacitor.

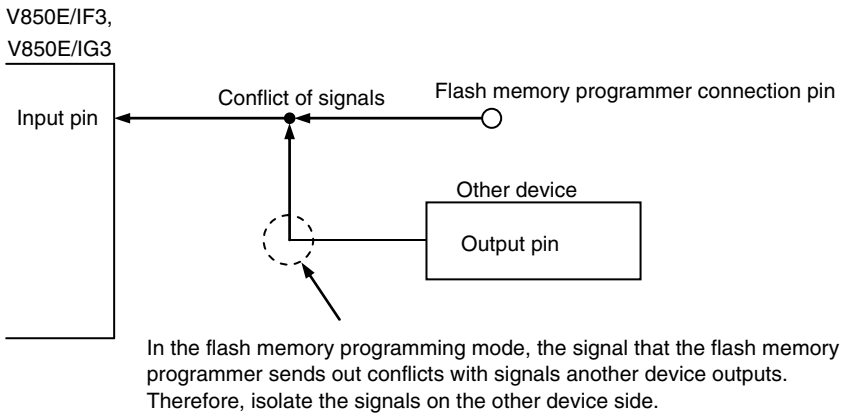
2. For details, refer to the user's manual of each programmer.

The flash memory programmer outputs the transfer clock, and the V850E/IF3 or V850E/IG3 operates as a slave.

When the PG-FP4 or PG-FP5 is used, it sends the following signals to the V850E/IF3 or V850E/IG3. For details, refer to the **PG-FP4 User's Manual (U15260E)** or **PG-FP5 User's Manual (U18865E)**.

(1) Conflict of signals

When the flash memory programmer (output) is connected to an interface pin (input) that is connected to another device (output), a conflict of signals occurs. To avoid the conflict of signals, isolate the connection to the other device or set the other device to the output high-impedance status.



In the flash memory programming mode, the signal that the flash memory programmer sends out conflicts with signals another device outputs. Therefore, isolate the signals on the other device side.

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