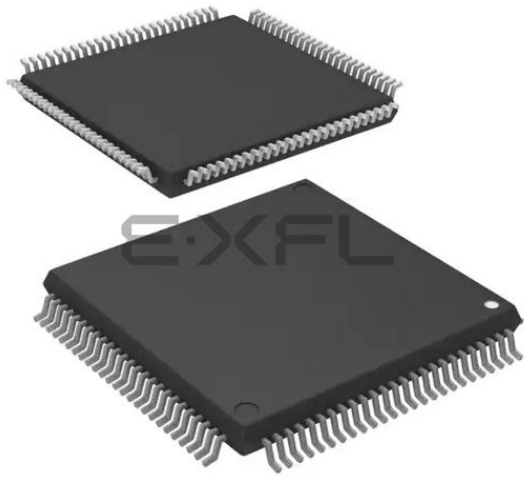
Renesas Electronics America Inc - UPD70F3454GC(R)-8EA-A Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CSI, EBI/EMI, I²C, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	56
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 10x12b, 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3454gc-r-8ea-a

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Pin	Alternate-Function Pin Name	Pin No.				I/O Circuit Type	Recommended Connection
		IF3	IG3				
		GC	GC	GF	F1		
PDL4	AD4[Note 1]	61	77	5	C11	5-AG	Input: Independently connect to EV_{DD0}, EV_{DD1}, EV_{DD2}[Note 2] or EV_{SS0}, EV_{SS1}, EV_{SS2}[Note 2] via a resistor. Output: Leave open.
PDL5	AD5[Note 1]/FLMD1	60	76	4	A12		
PDL6	AD6[Note 1]	59	75	3	B12		
PDL7	AD7[Note 1]	58	74	2	C14		
PDL8	AD8[Note 1]	57	73	1	C13		
PDL9	AD9[Note 1]	56	72	100	D14		
PDL10[Note 2]	AD10[Note 1]	–	71	99	D13		
PDL11[Note 2]	AD11[Note 1]	–	70	98	D12		
PDL12[Note 2]	AD12[Note 1]	–	69	97	E14		
PDL13[Note 2]	AD13[Note 1]	–	68	96	E13		
PDL14[Note 2]	AD14[Note 1]	–	67	95	E12		
PDL15[Note 2]	AD15[Note 1]	–	66	94	F12		
ANI00	ANI05	1	2	30	D1	7-C	Connect to AV_{SS0} or AV_{SS1}.
ANI01	–	2	3	31	D2		
ANI02	–	3	4	32	E3		
ANI03	CREF0L	4	5	33	F3		
ANI04	CREF0F	5	6	34	F4		
ANI10	ANI15	16	17	45	J1		
ANI11	ANI16	15	16	44	J2		
ANI12	ANI17	14	15	43	H3		
ANI13	CREF1L	13	14	42	G3		
ANI14	CREF1F	12	13	41	G4		

Notes 1. μPD70F3454GC-8EA-A and 70F3454F1-DA9-A only

2. V850E/IG3 only

Remark IF3: V850E/IF3
IG3: V850E/IG3
GC (V850E/IF3): 80-pin plastic LQFP (14 × 14)
GC (V850E/IG3): 100-pin plastic LQFP (fine pitch) (14 × 14)
GF (V850E/IG3): 100-pin plastic LQFP (14 × 20)
F1 (V850E/IG3): 161-pin plastic FBGA (10 × 10)

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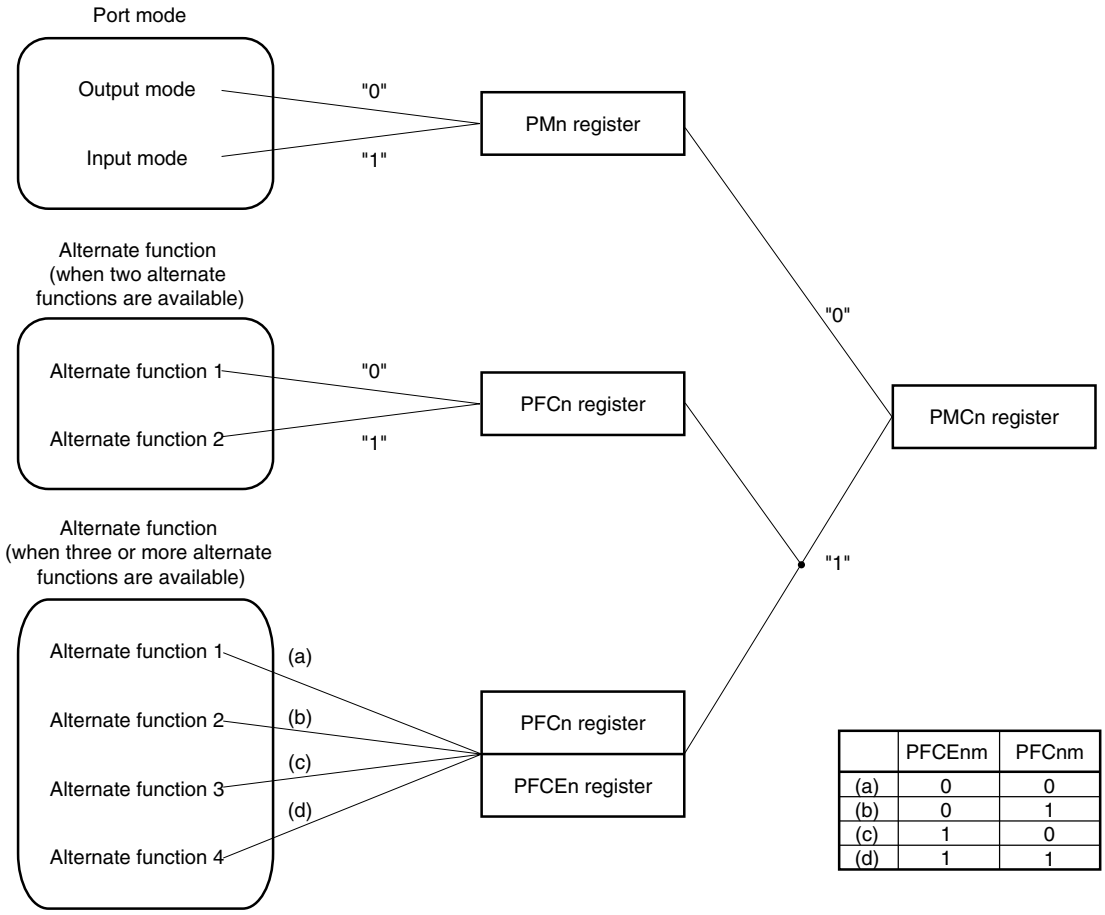
Address	Function Register Name	Symbol	R/W	Bit Units for Manipulation			After Reset
				1	8	16	
FFFFF100H	Interrupt mask register 0	IMR0	R/W			√	FFFFH
FFFFF100H	Interrupt mask register 0L	IMR0L		√	√		FFH
FFFFF101H	Interrupt mask register 0H	IMR0H		√	√		FFH
FFFFF102H	Interrupt mask register 1	IMR1				√	FFFFH
FFFFF102H	Interrupt mask register 1L	IMR1L		√	√		FFH
FFFFF103H	Interrupt mask register 1H	IMR1H		√	√		FFH
FFFFF104H	Interrupt mask register 2	IMR2				√	FFFFH
FFFFF104H	Interrupt mask register 2L	IMR2L		√	√		FFH
FFFFF105H	Interrupt mask register 2H	IMR2H		√	√		FFH
FFFFF106H	Interrupt mask register 3	IMR3				√	FFFFH
FFFFF106H	Interrupt mask register 3L	IMR3L		√	√		FFH
FFFFF107H	Interrupt mask register 3H	IMR3H		√	√		FFH
FFFFF108H	Interrupt mask register 4	IMR4				√	FFFFH
FFFFF108H	Interrupt mask register 4L	IMR4L		√	√		FFH
FFFFF109H	Interrupt mask register 4H	IMR4H		√	√		FFH
FFFFF10AH	Interrupt mask register 5	IMR5				√	FFFFH
FFFFF10AH	Interrupt mask register 5L	IMR5L		√	√		FFH
FFFFF10BH	Interrupt mask register 5H	IMR5H		√	√		FFH
FFFFF110H	Interrupt control register	LVILIC		√	√		47H
FFFFF112H	Interrupt control register	LVIHIC		√	√		47H
FFFFF114H	Interrupt control register	PIC00		√	√		47H
FFFFF116H	Interrupt control register	PIC01		√	√		47H
FFFFF118H	Interrupt control register	PIC02[Note]		√	√		47H
FFFFF11AH	Interrupt control register	PIC03[Note]		√	√		47H
FFFFF11CH	Interrupt control register	PIC04[Note]		√	√		47H
FFFFF11EH	Interrupt control register	PIC05[Note]		√	√		47H
FFFFF120H	Interrupt control register	PIC06[Note]		√	√		47H
FFFFF122H	Interrupt control register	PIC07[Note]		√	√		47H
FFFFF124H	Interrupt control register	PIC08		√	√		47H
FFFFF126H	Interrupt control register	PIC09		√	√		47H
FFFFF128H	Interrupt control register	PIC10		√	√		47H
FFFFF12AH	Interrupt control register	PIC11		√	√		47H
FFFFF12CH	Interrupt control register	PIC12		√	√		47H
FFFFF12EH	Interrupt control register	PIC13		√	√		47H
FFFFF130H	Interrupt control register	PIC14		√	√		47H
FFFFF132H	Interrupt control register	PIC15		√	√		47H
FFFFF134H	Interrupt control register	PIC16		√	√		47H
FFFFF136H	Interrupt control register	PIC17		√	√		47H
FFFFF138H	Interrupt control register	PIC18		√	√		47H
FFFFF13AH	Interrupt control register	CMPIC0L		√	√		47H

Note V850E/IG3 only

(7) Port settings

Set the ports as follows.

Figure 4-3. Register Settings and Pin Functions



	PFCEnm	PFCnm
(a)	0	0
(b)	0	1
(c)	1	0
(d)	1	1

Caution To switch to external interrupt input (INTPn) from the port mode (by changing the PMCa.PMCam bit from 0 to 1), an external interrupt may be input if a wrong valid edge is detected. Therefore, be sure to set "no edge detection" by INTRk, INTFk, ADTR, or ADTF register, select external interrupt input (INTPn), and then specify the valid edge (V850E/IF3: n = 00, 01, 08 to 18, ADT0, ADT1, a = 0 to 4, m = 0 to 7, k = 0 to 2, V850E/IG3: n = 00 to 18, ADT0, ADT1, a = 0 to 4, m = 0 to 7, k = 0 to 2)).

When switching to the port mode from external interrupt input (INTPn) (by changing the PMCam bit = from 1 to 0), an edge may be detected. Therefore, be sure to set "no edge detection" by INTRk, INTFk, ADTR, or ADTF register, and then select the port mode.

Remark Switch to the alternate function using the following procedure (for n, see **Tables 4-3** and **4-4**).

<1> Set the PFCn and PFCEn registers.

<2> Set the PMCn register.

<3> Set the INTRk, INTFk, ADTR, and ADTF registers (when external interrupt pin is set).

If the PMCn register is set before setting the PFCn and PFCEn registers, an unexpected peripheral function may be selected while the PFCn and PFCEn registers are being set.

4.3.6 Port 7

Port 7 is an input port with all its pins fixed to the input mode.

The number of input port pins differs depending on the product.

Generic Name	Number of I/O Ports
V850E/IF3	4-bit input-only port
V850E/IG3	8-bit input-only port

Port 7 has an alternate function as the following pins.

Table 4-11. Alternate-Function Pins of Port 7

Pin Name	Pin No.				Alternate-Function Pin Name	I/O	Pull-Up[Note 1]
	IF3	IG3					
	GC	GC	GF	F1			
P70	20	25	53	L1	ANI20	Input	None
P71	19	24	52	L2	ANI21	Input	
P72	18	23	51	L3	ANI22	Input	
P73	17	22	50	K1	ANI23	Input	
P74[Note 2]	–	21	49	K2	ANI24[Note 2]	Input	
P75[Note 2]	–	20	48	K3	ANI25[Note 2]	Input	
P76[Note 2]	–	19	47	K4	ANI26[Note 2]	Input	
P77[Note 2]	–	18	46	J4	ANI27[Note 2]	Input	

Notes 1. Software pull-up function

2. V850E/IG3 only

Remark IF3: V850E/IF3

IG3: V850E/IG3

GC (V850E/IF3): 80-pin plastic LQFP (14 × 14)

GC (V850E/IG3): 100-pin plastic LQFP (fine pitch) (14 × 14)

GF (V850E/IG3): 100-pin plastic LQFP (14 × 20)

F1 (V850E/IG3): 161-pin plastic FBGA (10 × 10)

Table 4-13. Output Data and Port Read Value for Each Setting (7/12)

Port Name	Function	PMCmn	PFCEmn	PFCmn	PMmn	Output Data	Pmn Read Value	Remark
P33	Output port	0	None	×	0	Port latch	Port latch	
	Input port				1	–	Pin level	
	SOB1	1	None	0	0	Alternate output 1 (serial output)	Port latch	
					1		Pin level	
	TXDA2	1	None	1	0	Alternate output 2 (serial output)	Port latch	
					1		Pin level	
P34	Output port	0	×	×	0	Port latch	Port latch	
	Input port				1	–	Pin level	
	$\overline{\text{SCKB1}}$	1	0	0	0	Alternate I/O (serial I/O)	Port latch	Output in master mode Input in slave mode
					1		Pin level	
	INTP11	1	0	1	0	–	Port latch	Alternate input (external interrupt input (necessary to specify valid edge))
					1		Pin level	
	$\overline{\text{CS0}}$[Note]	1	1	0	0	Alternate output (bus output)	Port latch	
					1		Pin level	
P35	Output port	0	×	×	0	Port latch	Port latch	
	Input port				1	–	Pin level	
	SIB2	1	0	0	0	–	Port latch	Alternate input (serial input)
					1		Pin level	
	RXDB	1	0	1	0	–	Port latch	Alternate input (serial input)
					1		Pin level	

Note μPD70F3454GC-8EA-A and 70F3454F1-DA9-A only

Remark ×: don't care

(6) TAAn option register 0 (TAAnOPT0)

The TAAnOPT0 register is an 8-bit register that sets the capture/compare operation and detects overflow.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

After reset: 00H R/W Address: TAA0OPT0 FFFFF665H, TAA1OPT0 FFFFF685H, TAA2OPT0 FFFFF6A5H, TAA3OPT0 FFFFFB05H, TAA4OPT0 FFFFFB25H

	7	6	5	4	3	2	1	<0>
TAAnOPT0	0	0	TAAmCCS1Note	TAAmCCS0Note	0	0	0	TAAnOVF

V850E/IF3
n = 0 to 4
m = 2, 4

V850E/IG3
n = 0 to 4
m = 2 to 4

TAAmCCS1Note	TAAmCCR1 register capture/compare selection
0	Compare register selected
1	Capture register selected (cleared by TAAmCTL0.TAAmCE bit = 0)
The TAAmCCS1 bit setting is valid only in the free-running timer mode.	

TAAmCCS0Note	TAAmCCR0 register capture/compare selection
0	Compare register selected
1	Capture register selected (cleared by TAAmCTL0.TAAmCE bit = 0)
The TAAmCCS0 bit setting is valid only in the free-running timer mode.	

TAAnOVF	TAAn overflow detection flag
Set (1)	Overflow occurred
Reset (0)	0 is written to TAAnOVF bit or TAAnCTL0.TAAnCE bit = 0

- The TAAnOVF bit is set to 1 when the 16-bit counter value overflows from FFFFH to 0000H in the free-running timer mode or the pulse width measurement mode.
- An overflow interrupt request signal (INTTAnOV) is generated at the same time that the TAAnOVF bit is set to 1. The INTTAnOV signal is not generated in modes other than the free-running timer mode and the pulse width measurement mode.
- The TAAnOVF bit is not cleared to 0 even when the TAAnOVF bit or the TAAnOPT0 register are read when the TAAnOVF bit = 1.
- Before clearing the TAAnOVF bit to 0 after generation of the INTTAnOV signal, be sure to confirm (by reading) that the TAAnOVF bit is set to 1.
- The TAAnOVF bit can be both read and written, but the TAAnOVF bit cannot be set to 1 by software. Writing 1 has no effect on the operation of TAAn.

Note With the V850E/IF3, this bit can be set only in TAA2 and TAA4. Be sure to set bits 4 and 5 of TAA0, TAA1, and TAA3 to “0”.

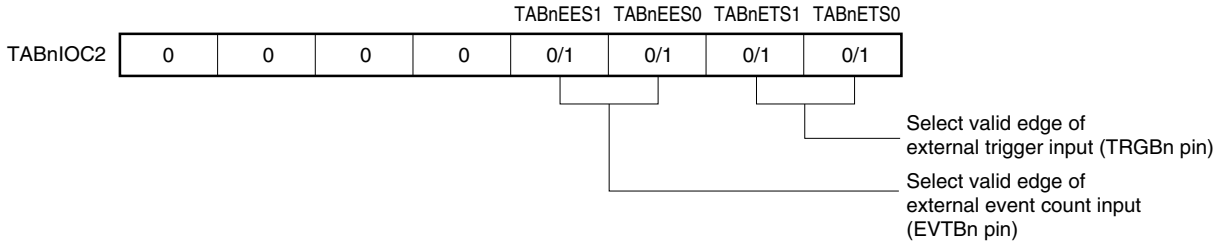
With the V850E/IG3, this bit can be set only in TAA2 to TAA4. Be sure to set bits 4 and 5 of TAA0 and TAA1 to “0”.

Cautions 1. Rewrite the TAAmCCS1 and TAAmCCS0 bits when the TAAmCE bit = 0. (The same value can be written when the TAAmCE bit = 1.) If rewriting was mistakenly performed, clear the TAAmCE bit to 0 and then set the bits again.

2. Be sure to set bits 1 to 3, 6, and 7 to “0”.

Figure 7-22. Setting of Registers in External Trigger Pulse Output Mode (3/3)

(d) TABn I/O control register 2 (TABnIOC2)



(e) TABn counter read buffer register (TABnCNT)

The value of the 16-bit counter can be read by reading the TABnCNT register.

(f) TABn capture/compare registers 0 to 3 (TABnCCR0 to TABnCCR3)

If D_0 is set to the TABnCCR0 register, D_1 to the TABnCCR1 register, D_2 to the TABnCCR2 register, and D_3, to the TABnCCR3 register, the cycle and active level of the PWM waveform are as follows.

Cycle = $(D_0 + 1) \times$ Count clock cycle
TOBn1 pin PWM waveform active level width = $D_1 \times$ Count clock cycle
TOBn2 pin PWM waveform active level width = $D_2 \times$ Count clock cycle
TOBn3 pin PWM waveform active level width = $D_3 \times$ Count clock cycle

Remarks 1. TABn I/O control register 1 (TABnIOC1) and TABn option register 0 (TABnOPT0) are not used in the external trigger pulse output mode.

2. n = 0, 1
b = 1 to 3

8.6.7 Pulse width measurement mode (TTmMD3 to TTmMD0 bits = 0110)

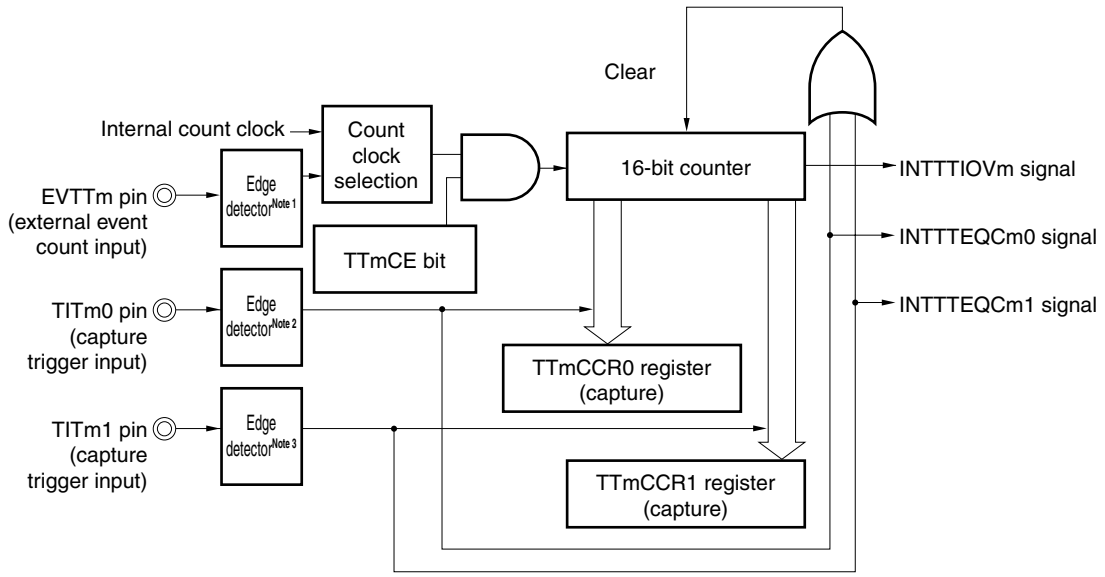
This mode is valid only in TMT0 (V850E/IG3 only) and TMT1.

In the pulse width measurement mode, 16-bit timer/event counter T starts counting when the TTmCTL0.TTmCE bit is set to 1. Each time the valid edge input to the TITma pin has been detected, the count value of the 16-bit counter is stored in the TTmCCRa register, and the 16-bit counter is cleared to 0000H.

The interval of the valid edge can be measured by reading the TTmCCRa register after a capture interrupt request signal (INTTTEQCma) occurs.

As shown in Figure 8-40, select either the TITm0 or TITm1 pin as the capture trigger input pin and set the unused pins to “No edge detection” by using the TTmIOC1 register.

Figure 8-39. Configuration in Pulse Width Measurement Mode



Notes 1. Set by the TTmIOC2.TTmEES1 and TTmIOC2.TTmEES0 bits.

2. Set by the TTmIOC1.TTmIS1 and TTmIOC1.TTmIS0 bits.

3. Set by the TTmIOC1.TTmIS3 and TTmIOC1.TTmIS2 bits.

Remark V850E/IF3: m = 1, a = 0, 1
V850E/IG3: m = 0, 1, a = 0, 1

Figure 8-41. Register Setting in Pulse Width Measurement Mode (2/2)

(e) TMTm option register 0 (TTmOPT0)

	TTmCCS1	TTmCCS0					TTmOVF
TTmOPT0	0	0	0	0	0	0	0	0/1

Overflow flag

(f) TMTm counter read buffer register (TTmCNT)

The value of the 16-bit counter can be read by reading the TTmCNT register.

(g) TMTm capture/compare registers 0 and 1 (TTmCCR0 and TTmCCR1)

These registers store the count value of the 16-bit counter when the valid edge input to the TITm0 and TITm1 pins is detected.

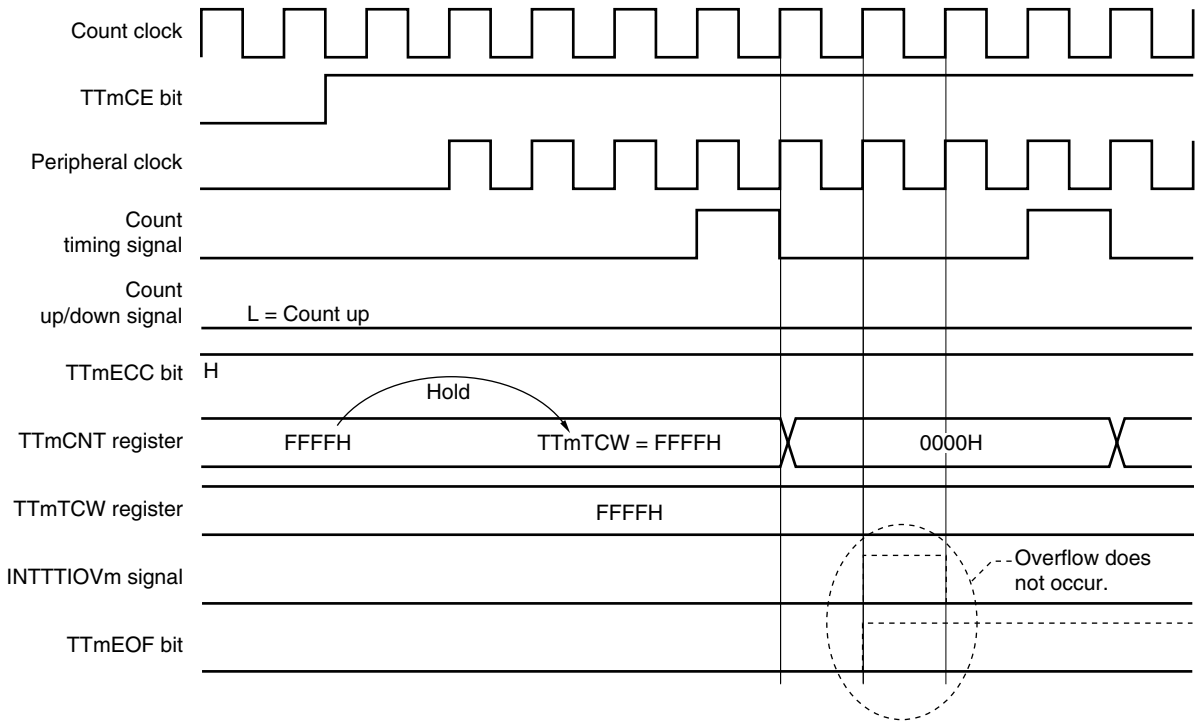
Remarks 1. TMTm control register 2 (TTmCTL2), TMTm I/O control register 0 (TTmIOC0), TMTm I/O control register 3 (TTmIOC3), TMTm option register 1 (TTmOPT1), TMTm capture input select register (TTISLm), and TMTm counter write register (TTmTCW) are not used in the pulse width measurement mode.

2. V850E/IF3: m = 1
V850E/IG3: m = 0, 1

(b) If overflow does not occur immediately after start of operation

If the count operation is resumed when the TTmCTL2.TTmECC bit = 1, the 16-bit counter does not overflow if its count value that has been held is FFFFH and if the next count operation is counting up.

After the counter starts operating and counts up from a count value (value of TTmTCW register = FFFFH), the counter overflows from FFFFH to 0000H. However, detection of the overflow is masked, the overflow flag (TTmEOF) is not set, and the overflow interrupt request signal (INTTTIOVm) is not generated.



Remark V850E/IF3: m = 1
V850E/IG3: m = 0, 1

10.4.4 Operation to rewrite register with transfer function

The following seven registers are provided with a transfer function and used to control a motor. Each of registers has a buffer register.

- TABnCCR0: Register that specifies the cycle of the 16-bit counter (TAB)
- TABnCCR1: Register that specifies the duty factor of TOBnT1 (U) and TOBnB1 ($\overline{U}$)
- TABnCCR2: Register that specifies the duty factor of TOBnT2 (V) and TOBnB2 ($\overline{V}$)
- TABnCCR3: Register that specifies the duty factor of TOBnT3 (W) and TOBnB3 ($\overline{W}$)
- TABnOPT1: Register that specifies the culling of interrupts
- TAAnCCR0: Register that specifies the A/D conversion start trigger generation timing (TAAn during tuning operation)
- TAAnCCR1: Register that specifies the A/D conversion start trigger generation timing (TAAn during tuning operation)

The following three rewrite modes are provided in the registers with a transfer function.

- Anytime rewriting mode

  This mode is specified by setting the TABnOPT0.TABnCMS bit to 1. The setting of the TABnOPT2.TABnRDE bit is ignored.

  In this mode, each compare register is updated independently, and the value of the compare register is updated as soon as a new value is written to it.

- Batch rewrite mode (transfer mode)

  This mode is specified by setting the TABnOPT0.TABnCMS bit to 0, the TABnOPT1.TABnID4 to TABnOPT1.TABnID0 bits to 00000, and the TABnOPT2.TABnRDE bit to 0.

  When data is written to the TABnCCR1 register, the seven registers are transferred to the buffer register all at once at the next transfer timing. Unless the TABnCCR1 register is rewritten, the transfer operation is not performed even if the other six registers are rewritten.

  The transfer timing is the timing of each crest (match between the 16-bit counter value and TABnCCR0 register value) and valley (match between the 16-bit counter value and 0001H) regardless of the interrupt.

- Intermittent batch rewrite mode (transfer culling mode)

  This mode is specified by setting the TABnOPT0.TABnCMS bit to 0 and the TABnOPT2.TABnRDE bit to 1.

  When data is written to the TABnCCR1 register, the seven registers are transferred to the buffer register all at once at the next transfer timing. Unless the TABnCCR1 register is rewritten, the transfer operation is not performed even if the other six registers are rewritten.

  If interrupt culling is specified by the TABnOPT1 register, the transfer timing is also culled as the interrupts are culled, and the seven registers are transferred all at once at the culled timing of crest interrupt (match between the 16-bit counter value and TABnCCR0 register value) or valley interrupt (match between the 16-bit counter value and 0001H).

  For details of the interrupt culling function, see **10.4.3 Interrupt culling function**.

10.4.6 A/D conversion start trigger output function

The V850E/IF3 and V850E/IG3 have a function to select four trigger sources (INTTBnOV, INTTBnCC0, INTTAnCC0, INTTAnCC1) to generate the A/D conversion start trigger signal (TABTADTn0, TABTADTn1) of A/D converters 0 and 1.

The trigger sources are specified by the TABnOPT2.TABnAT0 to TABnOPT2.TABnAT3 and TABnOPT3.TABnAT4 to TABnOPT3.TABnAT7 bits.

- TABnAT0, TABnAT4 bits = 1:
  A/D conversion start trigger signal generated when INTTBnOV (counter underflow) occurs.
- TABnAT1, TABnAT5 bits = 1:
  A/D conversion start trigger signal generated when INTTBnCC0 (cycle match) occurs.
- TABnAT2, TABnAT6 bits = 1:
  A/D conversion start trigger signal generated when INTTAnCC0 (match of TAAnCCR0 register of TAAn during tuning operation) occurs.
- TABnAT3, TABnAT7 bits = 1:
  A/D conversion start trigger signal generated when INTTAnCC1 (match of TAAnCCR1 register of TAAn during tuning operation) occurs.

The A/D conversion start trigger signals selected by the TABnAT0 to TABnAT3 and TABnAT4 to TABnAT7 bits are ORed and output. Therefore, two or more trigger sources can be specified at the same time.

The INTTBnOV and INTTBnCC0 signals selected by the TABnAT0, TABnAT1, TABnAT4, and TABnAT5 bits are culled interrupt signals.

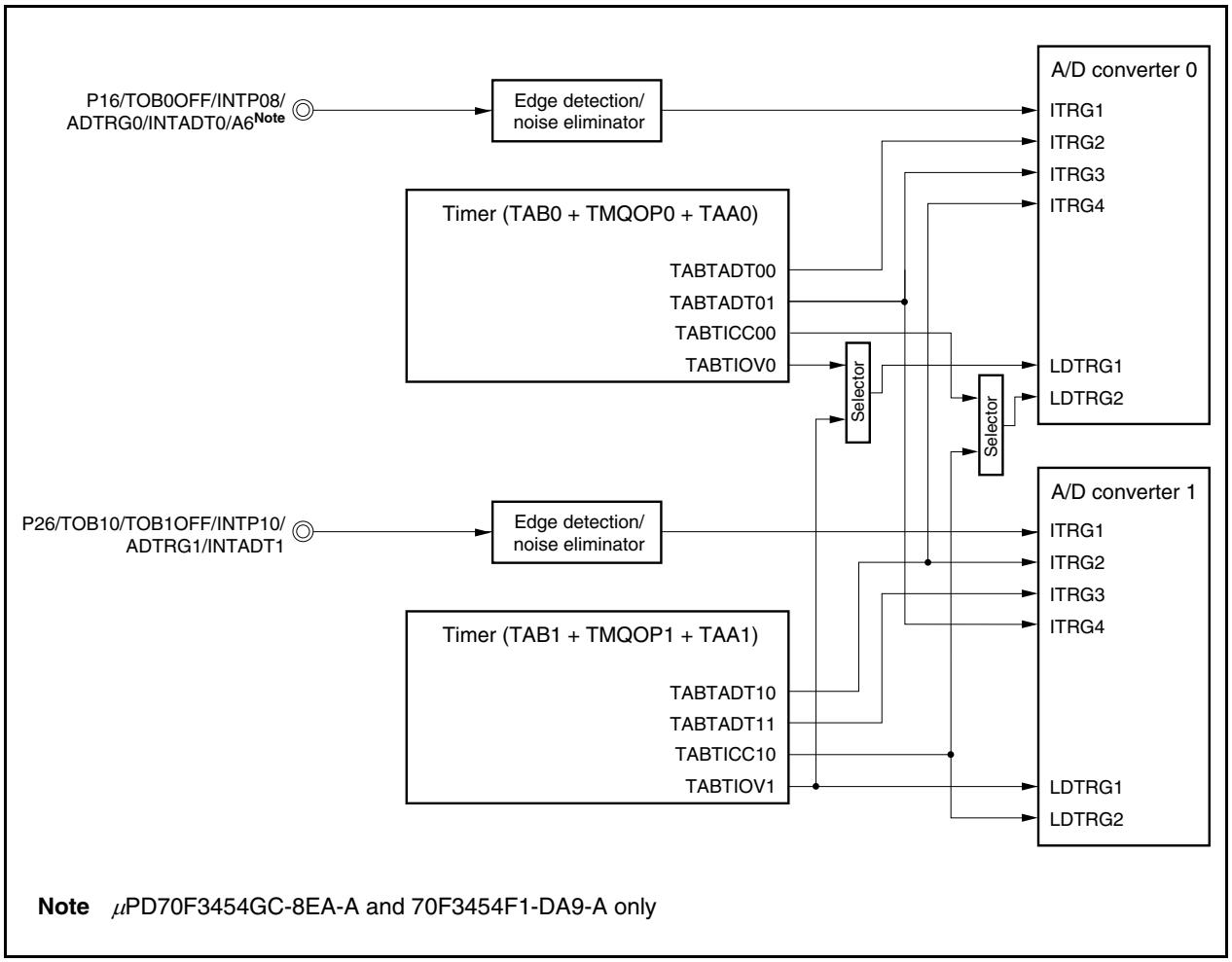
Therefore, these signals are output after the interrupts have been culled and, unless interrupt output is enabled (TABnOPT1.TABnICE, TABnOPT1.TABnIOE bits), the A/D conversion start trigger is not output.

The trigger sources (INTTAnCC0 and INTTAnCC1) from TAAn have a function to mask the A/D conversion start trigger signal depending on the status of the up-count/down-count of the 16-bit counter, if so set by the TABnAT2, TABnAT3, TABnAT6, and TABnAT7 bits.

- TABnATM2, TABnATM6 bits:
  Correspond to the TABnAT2 and TABnAT6 bits and control INTTAnCC0 (match interrupt signal) of TAAn.
  - TABnATM2, TABnATM6 bits = 0
    The A/D conversion start trigger signal is output when the 16-bit counter counts up (TABnOPT0.TABnCUF bit = 0), and the A/D conversion start trigger signal is not output when the 16-bit counter counts down (TABnOPT0.TABnCUF bit = 1).
  - TABnATM2, TABnATM6 bits = 1
    The A/D conversion start trigger signal is output when the 16-bit counter counts down (TABnOPT0.TABnCUF bit = 1), and the A/D conversion start trigger signal is not output when the 16-bit counter counts up (TABnOPT0.TABnCUF bit = 0).

- TABnATM3, TABnATM7 bits:
  Correspond to the TABnAT3 and TABnAT7 bits and control INTTAnCC1 (match interrupt signal) of TAAn.
  - TABnATM3, TABnATM7 bits = 0
    The A/D conversion start trigger signal is output when the 16-bit counter counts up (TABnCUF bit = 0), and the A/D conversion start trigger signal is not output when the 16-bit counter counts down (TABnCUF bit = 1).
  - TABnATM3, TABnATM7 bits = 1
    The A/D conversion start trigger signal is output when the 16-bit counter counts down (TABnCUF bit = 1), and the A/D conversion start trigger signal is not output when the 16-bit counter counts up (TABnCUF bit = 0).

Figure 12-6. Block Diagram of Trigger Source Selector in Hardware Trigger Mode



Note μPD70F3454GC-8EA-A and 70F3454F1-DA9-A only

After reset: 0000H R Address: AD0CR0 FFFFF200H, AD0CR1 FFFFF202H,
AD0CR2 FFFFF204H, AD0CR3 FFFFF206H,
AD0CR4 FFFFF208H, AD0CR5 FFFFF20AH,
AD0CR6 FFFFF20CH, AD0CR7 FFFFF20EH,
AD0CR8 FFFFF210H, AD0CR9 FFFFF212H,
AD0CR10 FFFFF214H, AD0CR11 FFFFF216H,
AD0CR12 FFFFF218H, AD0CR13 FFFFF21AH,
AD0CR14 FFFFF21CH, AD0CR15 FFFFF21EH,
AD1CR0 FFFFF280H, AD1CR1 FFFFF282H,
AD1CR2 FFFFF284H, AD1CR3 FFFFF286H,
AD1CR4 FFFFF288H, AD1CR5 FFFFF28AH,
AD1CR6 FFFFF28CH, AD1CR7 FFFFF28EH,
AD1CR8 FFFFF290H, AD1CR9 FFFFF292H,
AD1CR10 FFFFF294H, AD1CR11 FFFFF296H,
AD1CR12 FFFFF298H, AD1CR13 FFFFF29AH,
AD1CR14 FFFFF29CH, AD1CR15 FFFFF29EH

ADnCRm
(n = 0, 1)
(m = 0 to 15)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADnCRm11	ADnCRm10	ADnCRm9	ADnCRm8	ADnCRm7	ADnCRm6	ADnCRm5	ADnCRm4	ADnCRm3	ADnCRm2	ADnCRm1	ADnCRm0	0	0	0	0

After reset: 0000H R Address: AD0CR0H FFFFF201H, AD0CR1H FFFFF203H,
AD0CR2H FFFFF205H, AD0CR3H FFFFF207H,
AD0CR4H FFFFF209H, AD0CR5H FFFFF20BH,
AD0CR6H FFFFF20DH, AD0CR7H FFFFF20FH,
AD0CR8H FFFFF211H, AD0CR9H FFFFF213H,
AD0CR10H FFFFF215H, AD0CR11H FFFFF217H,
AD0CR12H FFFFF219H, AD0CR13H FFFFF21BH,
AD0CR14H FFFFF21DH, AD0CR15H FFFFF21FH,
AD1CR0H FFFFF281H, AD1CR1H FFFFF283H,
AD1CR2H FFFFF285H, AD1CR3H FFFFF287H,
AD1CR4H FFFFF289H, AD1CR5H FFFFF28BH,
AD1CR6H FFFFF28DH, AD1CR7H FFFFF28FH,
AD1CR8H FFFFF291H, AD1CR9H FFFFF293H,
AD1CR10H FFFFF295H, AD1CR11H FFFFF297H,
AD1CR12H FFFFF299H, AD1CR13H FFFFF29BH,
AD1CR14H FFFFF29DH, AD1CR15H FFFFF29FH

ADnCRmH
(n = 0, 1)
(m = 0 to 15)

7	6	5	4	3	2	1	0
ADnCRm11	ADnCRm10	ADnCRm9	ADnCRm8	ADnCRm7	ADnCRm6	ADnCRm5	ADnCRm4

(8) A/D converter n channel specification register 2 (ADnCH2)

The ADnCH2 register is a register that specifies the analog input pin for selection trigger 2 in the extension buffer mode.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

After reset: 00H R/W Address: AD0CH2 FFFFF233H, AD1CH2 FFFFF2B3H

	7	6	5	4	3	2	1	0
ADnCH2 (n = 0, 1)	0	ADn TRGCH26	ADn TRGCH25	ADn TRGCH24	0	ADn TRGCH22	ADn TRGCH21	ADn TRGCH20

ADnTRGCH26	ADnTRGCH25	ADnTRGCH24	Specification of analog input pin for selection trigger 2
0	0	0	ANIn0
0	0	1	ANIn1
0	1	0	ANIn2
0	1	1	ANIn3
1	0	0	ANIn4
1	0	1	ANIn5
1	1	0	ANI16
1	1	1	ANI17

ADnTRGCH22	ADnTRGCH21	ADnTRGCH20	Specification of analog input pin for selection trigger 2
0	0	0	ANIn0
0	0	1	ANIn1
0	1	0	ANIn2
0	1	1	ANIn3
1	0	0	ANIn4
1	0	1	ANIn5
1	1	0	ANI16
1	1	1	ANI17

Cautions 1. Set the ADnCH2 register when the ADnSCM.ADnCE bit = 0 (conversion operation is stopped) (the same value can be written to the register when the ADnCE bit = 1 (conversion operation is enabled)).

2. The ADnCH2 register is valid only in the extension buffer mode; it is invalid in any other mode.

3. Be sure to set bits 3 and 7 to "0".

(2) Operation of multiple channel conversion

The signals of two or more analog input pins specified by the ADnCHEN register are converted sequentially starting from the pin with the lowest number. The result of conversion is stored in the ADnCRk register corresponding to the analog input pin.

When conversion of the signals of all the specified analog input pins is completed, an A/Dn conversion end interrupt request signal (INTADn) is generated. After A/D conversion is completed, the A/D converter stops conversion operation with the ADnSCM.ADnCE bit remaining set to 1. The A/D conversion can be restarted by setting the ADnCE bit to 1.

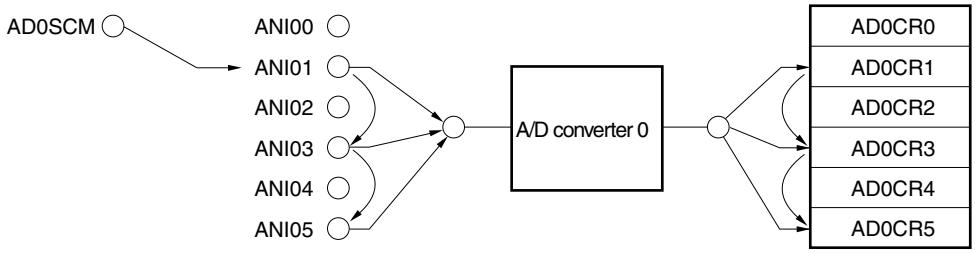
This operation is suitable for an application where two or more analog input signals should be monitored.

Analog Input Pin	A/D Conversion Result Register
ANInk[Note]	ADnCRk
ANInk[Note]	ADnCRk

Note Two or more can be specified by the ADnCHEN register.
However, A/D conversion is sequentially executed starting from the pin with the lowest number.

Remark A/D converter 0: n = 0, k = 0 to 5
A/D converter 1: n = 1, k = 0 to 7

Figure 12-15. Example of Multiple Channel Conversion Operation (A/D Trigger Mode): A/D Converter 0



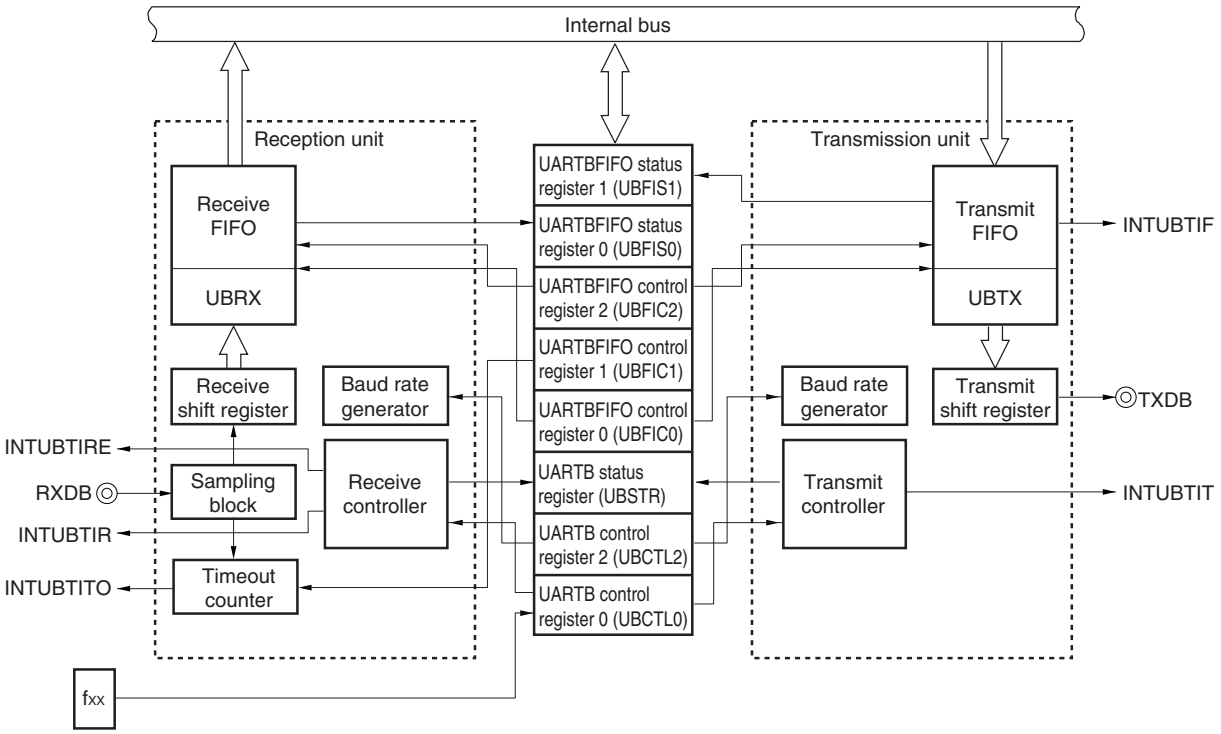
(1) AD0CE bit = 1 (enable)
(2) Signal of ANI01 pin is A/D-converted
(3) Conversion result is stored in AD0CR1 register
(4) Signal of ANI03 pin is A/D-converted
(5) Conversion result is stored in AD0CR3 register
(6) Signal of ANI05 pin is A/D-converted
(7) Conversion result is stored in AD0CR5 register
(8) AD0SCM.AD0CS bit = 0
(9) INTAD0 interrupt request signal is generated

Remark This is an operation example when the AD0SCM.AD0PLM, AD0TRG1, and AD0TRG0 bits = 000, AD0CTL0.AD0MD1 and AD0CTL0.AD0MD0 bits = 00, and AD0CHEN register = 002AH.

15.3 Configuration

The block diagram of the UARTB is shown below.

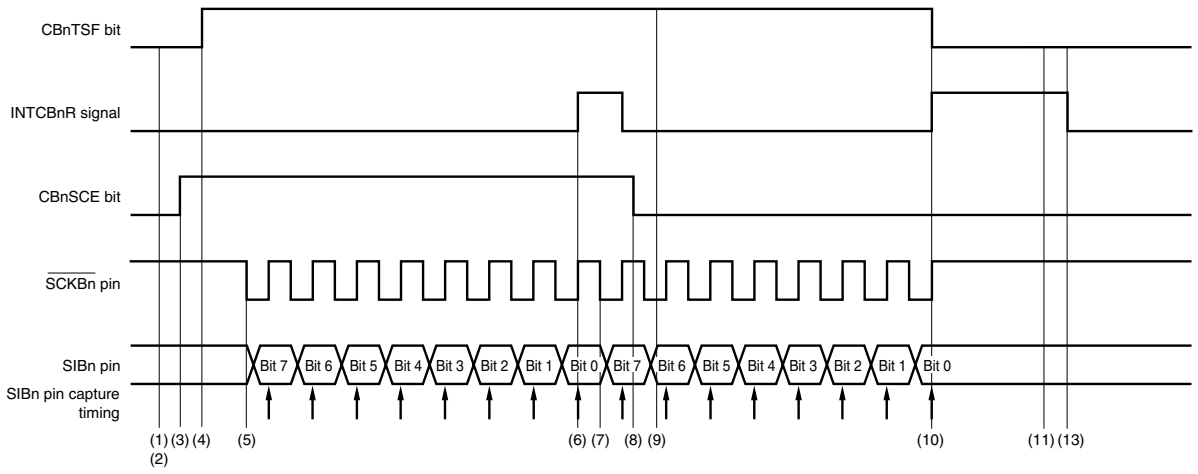
Figure 15-2. Block Diagram of UARTB



Remarks 1. fxx: Peripheral clock

2. For the configuration of the baud rate generator, see **Figure 15-9**.

(2) Operation timing



(1) Write 07H to the CBnCTL1 register, and select communication type 1, communication clock (f_{CCLK}) = external clock ($\overline{SCKBn}$), and slave mode.
(2) Write 00H to the CBnCTL2 register, and set the transfer data length to 8 bits.
(3) Write A3H to the CBnCTL0 register, and select the reception mode, MSB first, and continuous transfer mode at the same time as enabling the operation of the communication clock (f_{CCLK}).
(4) The CBnSTR.CBnTSF bit is set to 1 by performing a dummy read of the CBnRX register, and the device waits for a serial clock input.
(5) When a serial clock is input, capture the receive data of the SIBn pin in synchronization with the serial clock.
(6) When reception is ended, the reception end interrupt request signal (INTCBnR) is generated, and reading of the CBnRX register is enabled.
(7) When a serial clock is input in the CBnCTL0.CBnSCE bit = 1 status, continuous reception is started.
(8) To end continuous reception at the current reception, write the CBnSCE bit = 0.
(9) Read the CBnRX register.
(10) When reception is ended, the INTCBnR signal is generated, and reading of the CBnRX register is enabled. When the CBnSCE bit = 0 is set before communication end, clear the CBnTSF bit to 0 to end the receive operation.
(11) Read the CBnRX register.
(12) If an overrun error occurs, write the CBnSTR.CBnOVE bit = 0, and clear the error flag.
(13) To release the reception enable status, write the CBnCTL0.CBnPWR bit = 0 and the CBnCTL0.CBnRXE bit = 0 after checking that the CBnTSF bit = 0.

Remark n = 0 to 2

CHAPTER 20 INTERRUPT/EXCEPTION PROCESSING FUNCTION

The V850E/IF3 and V850E/IG3 are provided with a dedicated interrupt controller (INTC) for interrupt servicing and can process a total of 89 to 96 interrupt requests.

An interrupt is an event that occurs independently of program execution, and an exception is an event whose occurrence is dependent on program execution.

The V850E/IF3 and V850E/IG3 can process interrupt requests from the on-chip peripheral hardware and external sources. Moreover, exception processing can be started by the TRAP instruction (software exception) or by generation of an exception event (i.e. fetching of an illegal opcode) (exception trap).

20.1 Features

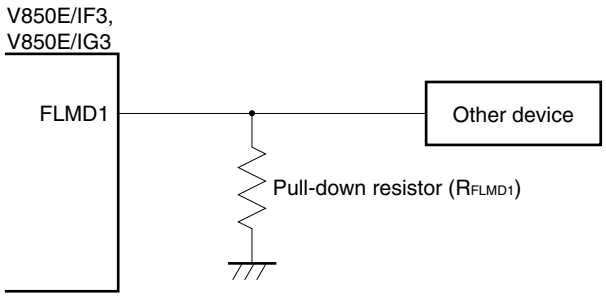
○ Interrupts
- Non-maskable interrupts: 1 source (external: none, internal: 1 source)
- Maskable interrupts (the number of maskable interrupt sources differs depending on the product)
  V850E/IF3: 88 sources (external: 15 sources, internal: 73 sources)
  V850E/IG3: 95 sources (external: 21 sources, internal: 74 sources)
- 8 levels of programmable priorities (maskable interrupts)
- Multiple interrupt control according to priority
- Masks can be specified for each maskable interrupt request.
- Noise elimination, edge detection, and valid edge specification for external interrupt request signals.

○ Exceptions
- Software exceptions: 32 sources
- Exception traps: 2 sources (illegal opcode exception and debug trap)

Interrupt sources are listed in Table 20-1.

(2) FLMD1 pin

When 0 V is input to the FLMD0 pin, the FLMD1 pin does not function. When EV_{DD0}, EV_{DD1}, or EV_{DD2} (V850E/IG3 only) is supplied to the FLMD0 pin, the flash memory programming mode is entered, so 0 V must be input to the FLMD1 pin. The following shows an example of the connection of the FLMD1 pin.



Caution If the EV_{DD0}, EV_{DD1}, or EV_{DD2} (V850E/IG3 only) signal is input to the FLMD1 pin from another device during on-board programming and immediately after reset, isolate this signal.

Table 27-8. Relationship Between FLMD0 and FLMD1 Pins and Operation Mode When Reset Is Released

FLMD0	FLMD1	Operation Mode
0	Don't care	Normal operation mode
EV_{DD}	0	Flash memory programming mode
EV_{DD}	EV_{DD}	Setting prohibited

Remark EV_{DD}: EV_{DD0}, EV_{DD1}, EV_{DD2} (V850E/IG3 only)

27.7.5 Port pins

When the flash memory programming mode is set, all the port pins except the pin that communicates with the flash memory programmer change to the high-impedance status. These port pins need not be processed. If problems such as disabling of the high-impedance status should occur to the external devices connected to the ports, connect them to EV_{DD0}, EV_{DD1}, EV_{DD2} (V850E/IG3 only), or EV_{SS0}, EV_{SS1}, EV_{SS2} (V850E/IG3 only) via resistors.

27.7.6 Other signal pins

Connect X1 and X2 in the same status as in the normal operation mode.