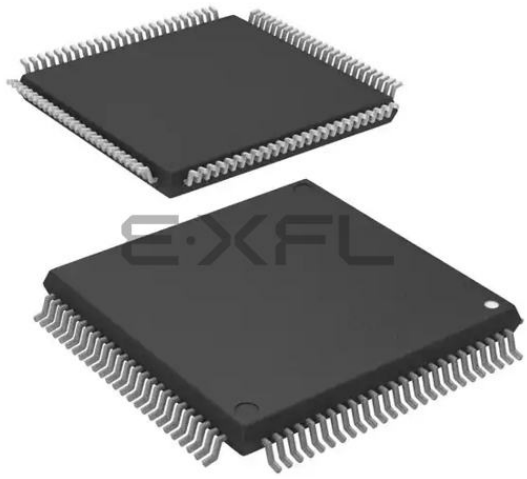
Renesas Electronics America Inc - UPD70F3454GF(R)-GAS-AX Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CSI, EBI/EMI, I²C, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	56
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 10x12b, 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3454gf-r-gas-ax

1.3 V850E/IG3

1.3.1 Features (V850E/IG3)

○ Minimum instruction execution time:
15.6 ns (at internal 64 MHz operation)

○ General-purpose registers: 32 bits × 32

○ CPU features: Signed multiplication (16 bits × 16 bits → 32 bits or 32 bits × 32 bits → 64 bits): 1 to 2 clocks
Saturated operation instructions (with overflow/underflow detection function)
32-bit shift instructions: 1 clock
Bit manipulation instructions
Load/store instructions with long/short format
Signed load instructions

○ Memory space (μPD70F3454GC-8EA-A and 70F3454F1-DA9-A only):
256 MB of linear address space (program/data sharing)
Chip select output function: 2 spaces
Memory block division function: 2 MB/block

- External bus interface: Multiplexed bus mode: 16-bit address bus
  8-bit/16-bit data bus
  Separate bus mode: 8-bit address bus
  8-bit/16-bit data bus
  8-bit/16-bit data bus sizing function
  External bus frequency switch function: 32/16 MHz
  Wait function
  • Programmable wait function
  • External wait function
  Idle state function
  Address setup wait function

○ Internal memory:

Part Number	Internal ROM	Internal RAM
μPD70F3453	128 KB (flash memory)	8 KB
μPD70F3454	256 KB (flash memory)	12 KB

○ On-chip debug function: Supports MINICUBE and MINICUBE2.

○ Interrupts/exceptions: Non-maskable interrupts: 1 source (external: none, internal: 1)
Maskable interrupts: 95 sources (external: 21, internal: 74)
Software exceptions: 32 sources
Exception traps: 2 sources

(14/14)

Address	Function Register Name	Symbol	R/W	Bit Units for Manipulation			After Reset
				1	8	16	
FFFFFC66H	Port 3 function register	PF3	R/W	√	√		00H
FFFFFD00H	CSIB0 control register 0	CB0CTL0		√	√		01H
FFFFFD01H	CSIB0 control register 1	CB0CTL1		√	√		00H
FFFFFD02H	CSIB0 control register 2	CB0CTL2			√		00H
FFFFFD03H	CSIB0 status register	CB0STR		√	√		00H
FFFFFD04H	CSIB0 receive data register	CB0RX	R			√	0000H
FFFFFD04H	CSIB0 receive data register L	CB0RXL			√		00H
FFFFFD06H	CSIB0 transmit data register	CB0TX	R/W			√	0000H
FFFFFD06H	CSIB0 transmit data register L	CB0TXL			√		00H
FFFFFD10H	CSIB1 control register 0	CB1CTL0		√	√		01H
FFFFFD11H	CSIB1 control register 1	CB1CTL1		√	√		00H
FFFFFD12H	CSIB1 control register 2	CB1CTL2			√		00H
FFFFFD13H	CSIB1 status register	CB1STR		√	√		00H
FFFFFD14H	CSIB1 receive data register	CB1RX	R			√	0000H
FFFFFD14H	CSIB1 receive data register L	CB1RXL			√		00H
FFFFFD16H	CSIB1 transmit data register	CB1TX	R/W			√	0000H
FFFFFD16H	CSIB1 transmit data register L	CB1TXL			√		00H
FFFFFD20H	CSIB2 control register 0	CB2CTL0		√	√		01H
FFFFFD21H	CSIB2 control register 1	CB2CTL1		√	√		00H
FFFFFD22H	CSIB2 control register 2	CB2CTL2			√		00H
FFFFFD23H	CSIB2 status register	CB2STR		√	√		00H
FFFFFD24H	CSIB2 receive data register	CB2RX	R			√	0000H
FFFFFD24H	CSIB2 receive data register L	CB2RXL			√		00H
FFFFFD26H	CSIB2 transmit data register	CB2TX	R/W			√	0000H
FFFFFD26H	CSIB2 transmit data register L	CB2TXL			√		00H
FFFFFD80H	IIC shift register 0	IIC0			√		00H
FFFFFD82H	IIC control register 0	IICC0		√	√		00H
FFFFFD83H	Slave address register 0	SVA0			√		00H
FFFFFD84H	IIC clock select register 0	IICCL0		√	√		00H
FFFFFD85H	IIC function expansion register 0	IICX0		√	√		00H
FFFFFD86H	IIC status register 0	IICS0	R	√	√		00H
FFFFFD8AH	IIC flag register 0	IICF0	R/W	√	√		00H
FFFFFD90H	IIC OPS clock select register	IICOCKS			√		00H
FFFFFF44H	Pull-up resistor option register DL	PUDL				√	0000H
FFFFFF44H	Pull-up resistor option register DLL	PUDLL		√	√		00H
FFFFFF45H	Pull-up resistor option register DLH	PUDLH		√	√		00H

Table 4-14. Using Port Pin as Alternate-Function Pin (4/8)

Pin Name	Alternate Pin		Pnx Bit of Pn Register	PMnx Bit of PMn Register	PMCnx Bit of PMCn Register	PFCEnx Bit of PFCEn Register	PFCnx Bit of PFCn Register	Other Bit (Register)
	Name	I/O						
P23	TOB1B2	Output	P23 = Setting not required	PM23 = Setting not required	PMC23 = 1	–	PFC23 = 0	
	TIB10	Input	P23 = Setting not required	PM23 = Setting not required	PMC23 = 1	–	PFC23 = 1	
P24	TOB1T3	Output	P24 = Setting not required	PM24 = Setting not required	PMC24 = 1	–	PFC24 = 0	
	EVTB1	Input	P24 = Setting not required	PM24 = Setting not required	PMC24 = 1	–	PFC24 = 1	
P25	TOB1B3	Output	P25 = Setting not required	PM25 = Setting not required	PMC25 = 1	–	PFC25 = 0	
	TRGB1	Input	P25 = Setting not required	PM25 = Setting not required	PMC25 = 1	–	PFC25 = 1	
P26	TOB10	Output	P26 = Setting not required	PM26 = Setting not required	PMC26 = 1	PFCE26 = 0	PFC26 = 0	
	TOB1OFF	Input	P26 = Setting not required	PM26 = Setting not required	PMC26 = 1	PFCE26 = 0	PFC26 = 1	
	INTP10	Input	P26 = Setting not required	PM26 = Setting not required	PMC26 = 1	PFCE26 = 0	PFC26 = 1	INTF10 (INTF1), INTR10 (INTR1)
	ADTRG1	Input	P26 = Setting not required	PM26 = Setting not required	PMC26 = 1	PFCE26 = 1	PFC26 = 0	
	INTADT1	Input	P26 = Setting not required	PM26 = Setting not required	PMC26 = 1	PFCE26 = 1	PFC26 = 0	ADTF1 (ADTF), ADTR1 (ADTR)
P27	DMS[Notes 1, 2]	Input	P27 = Setting not required	PM27 = Setting not required	–	–	–	
P30	RXDA1	Input	P30 = Setting not required	PM30 = Setting not required	PMC30 = 1	PFCE30 = 0	PFC30 = 0	
	SCL	I/O	P30 = Setting not required	PM30 = Setting not required	PMC30 = 1	PFCE30 = 0	PFC30 = 1	PF30 (PF3) = 1
P31	TXDA1	Output	P31 = Setting not required	PM31 = Setting not required	PMC31 = 1	PFCE31 = 0	PFC31 = 0	
	SDA	I/O	P31 = Setting not required	PM31 = Setting not required	PMC31 = 1	PFCE31 = 0	PFC31 = 1	PF31 (PF3) = 1

Notes 1. V850E/IG3 only

2. The P27 pin is also used for on-chip debugging. Switching between on-chip debug function and port function can be set by using the $\overline{\text{DRST}}$ pin level. The following shows the setting method.

Port 2 Functions	
Low-Level Input to $\overline{\text{DRST}}$ Pin	High-Level Input to $\overline{\text{DRST}}$ Pin
P27	DMS

(3) Power save control register (PSC)

The PSC register is an 8-bit register that controls the standby function and specifies the standby mode by setting the STB bit. The PSC register is a special register (see **3.4.8 Special registers**). Data can be written to this register only in a combination of specific sequences.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

After reset: 00H R/W Address: FFFFF1FEH

	7	6	5	<4>	3	2	<1>	0
PSC	0	0	0	INTM	0	0	STB	0

INTM	Standby mode control[Note 2] by maskable interrupt request (INTxx[Note 1])
0	Standby mode release by INTxx request enabled
1	Standby mode release by INTxx request disabled

STB	Sets operation mode
0	Normal mode
1	Standby mode

Notes 1. For details, see **Table 20-1 Interrupt Source List**.

2. Setting is valid only in the IDLE mode and STOP mode.

Cautions 1. Be sure to set bits 0, 2, 3, and 5 to 7 to "0".

2. Before setting a standby mode by setting the STB bit to 1, be sure to set the PCC register to 03H and then set the STB bit to 1. Otherwise, the standby mode may not be set or released. After releasing the standby mode, change the value of the PCC register to the desired value.

3. To set the IDLE mode or STOP mode, set the PCC register to 03H, and the PSMR.PSM0 bit in that order and then set the STB bit to 1.

(5) TAAm I/O control register 2 (TAAmIOC2)

The TAAmIOC2 register is an 8-bit register that controls the valid edge for the external event count input signal (TIAm0 pin) and external trigger input signal (TIAm0 pin).

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

After reset: 00H R/W Address: TAA2IOC2 FFFFF6A4H, TAA3IOC2 FFFFFB04H[Note], TAA4IOC2 FFFFFB24H

	7	6	5	4	3	2	1	0
TAAmIOC2	0	0	0	0	TAAmEES1	TAAmEES0	TAAmETS1	TAAmETS0

(V850E/IF3 m = 2, 4)

(V850E/IG3 m = 2 to 4)

TAAmEES1	TAAmEES0	External event count input signal (TIAm0 pin) valid edge setting
0	0	No edge detection (external event count invalid)
0	1	Detection of rising edge
1	0	Detection of falling edge
1	1	Detection of both edges

TAAmETS1	TAAmETS0	External trigger input signal (TIAm0 pin) valid edge setting
0	0	No edge detection (external trigger invalid)
0	1	Detection of rising edge
1	0	Detection of falling edge
1	1	Detection of both edges

Note V850E/IG3 only

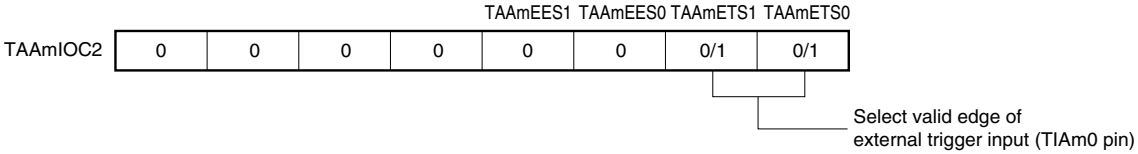
Cautions 1. Rewrite the TAAmEES1, TAAmEES0, TAAmETS1, and TAAmETS0 bits when the TAAmCTL0.TAAmCE bit = 0. (The same value can be written when the TAAmCE bit = 1.) If rewriting was mistakenly performed, clear the TAAmCE bit to 0 and then set the bits again.

2. The TAAmEES1 and TAAmEES0 bits are valid only when the TAAmCTL1.TAAmEEE bit = 1 or when the external event count mode (the TAAmCTL1.TAAmMD2 to TAAmCTL1.TAAmMD0 bits = 001) has been set.

3. The TAAmETS1 and TAAmETS0 bits are valid only in the external trigger pulse mode or one-shot pulse output mode.

Figure 6-30. Setting of Registers in One-Shot Pulse Output Mode (2/2)

(d) TAAm I/O control register 2 (TAAmIOC2)



(e) TAAm counter read buffer register (TAAmCNT)

The value of the 16-bit counter can be read by reading the TAAmCNT register.

(f) TAAm capture/compare registers 0 and 1 (TAAmCCR0 and TAAmCCR1)

If D_0 is set to the TAAmCCR0 register and D_1 to the TAAmCCR1 register, the active level width and output delay period of the one-shot pulse are as follows.

Active level width = $(D_0 - D_1 + 1) \times$ Count clock cycle
Output delay period = $D_1 \times$ Count clock cycle

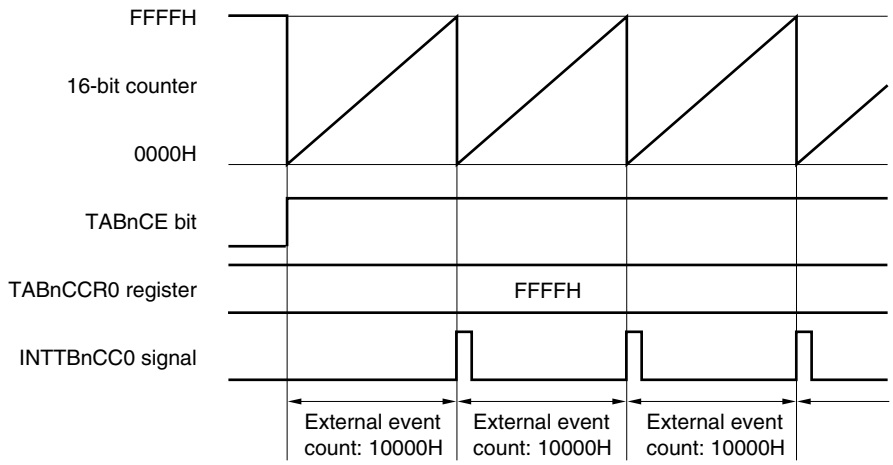
Caution One-shot pulses are not output even in the one-shot pulse output mode, if the value set in the TAAmCCR1 register is greater than that set in the TAAmCCR0 register.

Remarks 1. TAAm I/O control register 1 (TAAmIOC1) and TAAm option register 0 (TAAmOPT0) are not used in the one-shot pulse output mode.

2. V850E/IF3: m = 2, 4, a = 0, 1
V850E/IG3: m = 2 to 4, a = 0, 1

(b) Operation if TABnCCR0 register is set to FFFFH

If the TABnCCR0 register is set to FFFFH, the 16-bit counter counts to FFFFH each time the valid edge of the external event count signal has been detected. The 16-bit counter is cleared to 0000H in synchronization with the next count-up timing, and the INTTBnCC0 signal is generated. At this time, the TABnOPT0.TABnOVF bit is not set.



Remark n = 0, 1

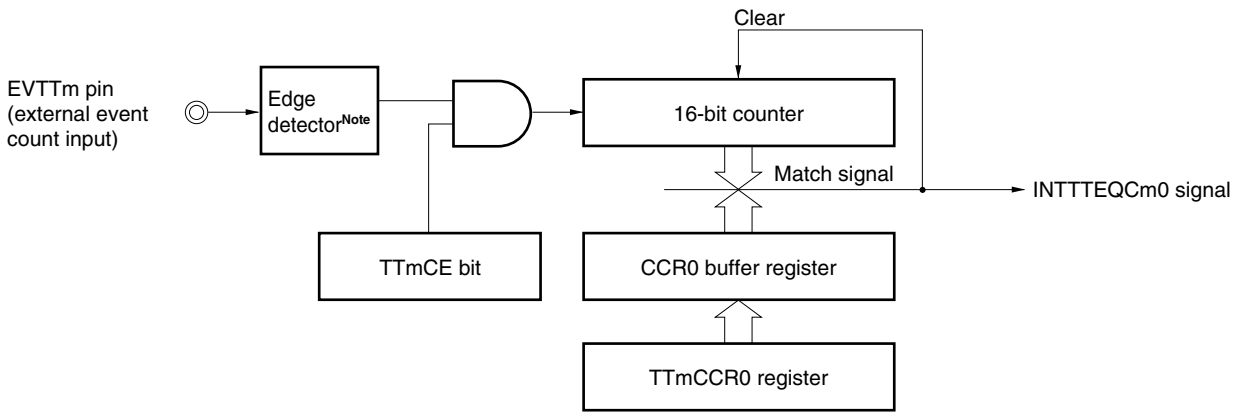
8.6.2 External event count mode (TTmMD3 to TTmMD0 bits = 0001)

This mode is valid only in TMT0 (V850E/IG3 only) and TMT1.

In the external event count mode, the valid edge of the external event count input (EVTTm) is counted when the TTmCTL0.TTmCE bit is set to 1, and an interrupt request signal (INTTTEQCm0) is generated each time the number of edges set by the TTmCCR0 register have been counted. The TOTm0 and TOTm1 pins cannot be used.

The TTmCCR1 register is not used in the external event count mode.

Figure 8-14. Configuration in External Event Count Mode

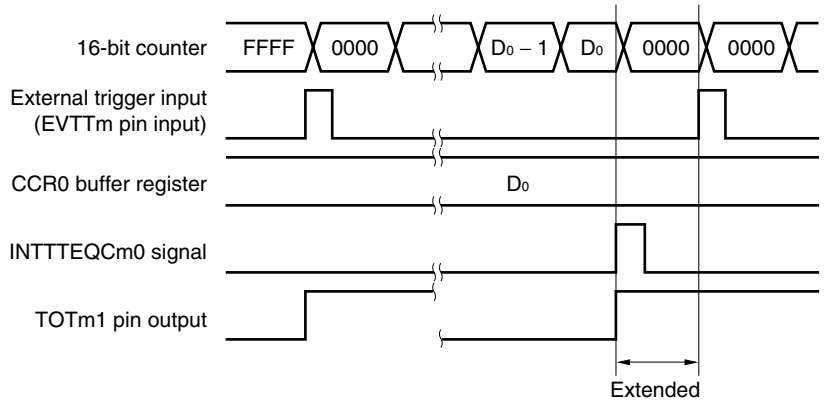


Note Set by the TTmIOC2.TTmEES1 and TTmIOC2.TTmEES0 bits.

Remark V850E/IF3: m = 1
V850E/IG3: m = 0, 1

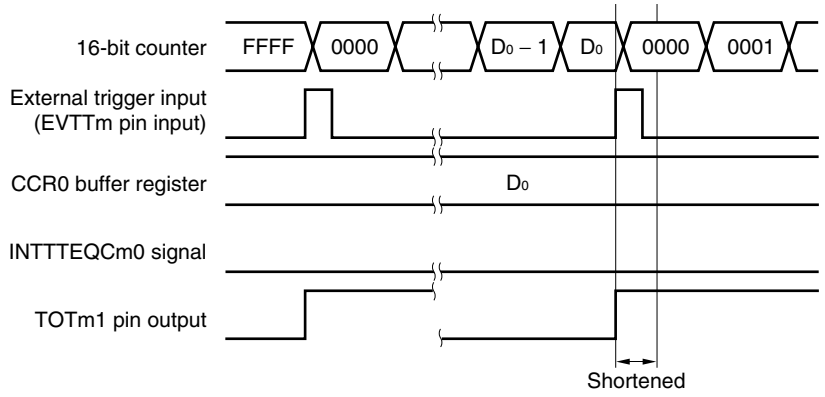
(d) Conflict between trigger detection and match with CCR0 buffer register

If the trigger is detected immediately after the INTTTEQCm0 signal is generated, the 16-bit counter is cleared to 0000H and continues counting up. Therefore, the active period of the TOTm1 pin is extended by time from generation of the INTTTEQCm0 signal to trigger detection.



Remark V850E/IF3: m = 1
V850E/IG3: m = 0, 1

If the trigger is detected immediately before the INTTTEQCm0 signal is generated, the INTTTEQCm0 signal is not generated. The 16-bit counter is cleared to 0000H, the TOTm1 pin is asserted, and the counter continues counting. Consequently, the inactive period of the PWM waveform is shortened.



Remark V850E/IF3: m = 1
V850E/IG3: m = 0, 1

(2) Interrupt requests

Two types of interrupt requests are available: the INTTBnCC0 (crest interrupt) signal and INTTBnOV (valley interrupt) signal.

The INTTBnCC0 and INTTBnOV signals can be culled by using the TABnOPT1 register.

For details of culling interrupts, see **10.4.3 Interrupt culling function**.

- INTTBnCC0 (crest interrupt) signal: Interrupt signal indicating matching between the value of the 16-bit counter that counts up and the value of the TABnCCR0 register
- INTTBnOV (valley interrupt) signal: Interrupt signal indicating matching between the value of the 16-bit counter that counts down and the value 0001H

(3) Rewriting registers during timer operation

The following registers have a buffer register and can be rewritten in the anytime rewriting mode, batch rewrite mode, or intermittent batch rewrite mode.

Related Unit	Register
Timer AAn	TAAn capture/compare register 0 (TAAnCCR0) TAAn capture/compare register 1 (TAAnCCR1)
Timer ABn	TABn capture/compare register 0 (TABnCCR0) TABn capture/compare register 1 (TABnCCR1) TABn capture/compare register 2 (TABnCCR2) TABn capture/compare register 3 (TABnCCR3)
Timer Qn option	TABn option register 1 (TABnOPT1)

Remark n = 0, 1

For details of the transfer function of the compare register, see **10.4.4 Operation to rewrite register with transfer function**.

(4) Counting-up/-down operation of 16-bit counter

The operation status of the 16-bit counter can be checked by using the TABnCUF bit of TABn option register 0 (TABnOPT0).

Status of TABnCUF Bit	Status of 16-Bit Counter	Range of 16-Bit Counter Value
TABnCUF bit = 0	Counting up	0000H – m
TABnCUF bit = 1	Counting down	(m+1) – 0001H

Remarks 1. m = Set value of TABnCCR0 register

2. n = 0, 1

14.1.3 Mode switching between UARTA2 and CSIB1

In the V850E/IF3 and V850E/IG3, UARTA2 and CSIB1 function alternately, and their pins cannot be used at the same time. To switch between UARTA2 and CSIB1, the PMC3, PFC3, and PFCE3 registers must be set in advance.

Caution The operations related to transmission and reception of UARTA2 or CSIB1 are not guaranteed if the mode is switched during transmission or reception. Be sure to disable the unit that is not used.

Figure 14-3. Mode Switch Settings of UARTA2 and CSIB1

After reset: 00H R/W Address: FFFFF446H

	7	6	5	4	3	2	1	0
PMC3	PMC37	PMC36	PMC35	PMC34	PMC33	PMC32	PMC31	PMC30

After reset: 00H R/W Address: FFFFF466H

	7	6	5	4	3	2	1	0
PFC3	PFC37	PFC36	PFC35	PFC34	PFC33	PFC32	PFC31	PFC30

After reset: 00H R/W Address: FFFFF706H

	7	6	5	4	3	2	1	0
PFCE3	PFCE37	PFCE36	PFCE35	PFCE34	0	PFCE32	PFCE31	PFCE30

PMC34	PFCE34	PFC34	Specification of alternate function of P34 pin
0	×	×	I/O port
1	0	0	$\overline{\text{SCKB1}}$ I/O
1	0	1	INTP11 input
1	1	0	$\overline{\text{CS0}}$[Note] output
1	1	1	Setting prohibited

PMC33	PFC33	Specification of alternate function of P33 pin
0	×	I/O port
1	0	SOB1 output
1	1	TXDA2 output

PMC32	PFCE32	PFC32	Specification of alternate function of P32 pin
0	×	×	I/O port
1	0	0	SIB1 input
1	0	1	RXDA2 input
1	1	0	$\overline{\text{CS1}}$[Note] output
1	1	1	Setting prohibited

Note μPD70F3454GC-8EA-A and 70F3454F1-DA9-A only

Remark x = don't care

(5) IIC function expansion register 0 (IICX0)

This register sets the function expansion of I²C (valid only in high-speed mode).

This register can be read or written in 8-bit or 1-bit units. The CLX0 bit is set in combination with the IICCL0.SMC0, IICCL0.CL00, IICOCKS.IICOCKS1, and IICOCKS.IICOCKS0 bits (see **17.4 (7) I²C transfer clock setting method**).

Set the IICX0 register when the IICC0.IICE0 bit = 0.

Reset sets this register to 00H.

After reset: 00H R/W Address: FFFFFD85H

	7	6	5	4	3	2	1	<0>
IICX0	0	0	0	0	0	0	0	CLX0

CLX0	Clock select expansion bit
0	Communicate at transfer rate set by the IICCL0.CL00 bit.
1	Communicate at double transfer rate set by the IICCL0.CL00 bit in high-speed mode .

(6) IICOPS clock select register (IICOCKS)

This register controls the division clock of I²C.

This register can be read or written in 8-bit or 1-bit units. The IICOCKS1 and IICOCKS0 bits are set in combination with the IICCL0.SMC0, IICCL0.CL00, and IICX0.CLX0 bits (see **17.4 (7) I²C transfer clock setting method**).

Reset sets this register to 00H.

After reset: 00H R/W Address: FFFFFD90H

	7	6	5	4	3	2	1	0
IICOCKS	0	0	0	IICOCKSEN	0	0	IICOCKS1	IICOCKS0

IICOCKSEN	Specification of I²C division clock operation
0	I²C division clock operation stop
1	I²C division clock operation enable

IICOCKS1	IICOCKS0	I²C division clock selection
0	0	$f_{XX}/4$
0	1	$f_{XX}/6$
1	0	$f_{XX}/8$
1	1	$f_{XX}/10$

(3) Start ~ Code ~ Data ~ Start ~ Code ~ Data ~ Stop

<1> When WTIM0 bit = 0 (after restart, extension code reception)

ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	SP

▲1 ▲2 ▲3 ▲4 Δ5

▲1: IICS0 register = 0010X010B

▲2: IICS0 register = 0010X000B

▲3: IICS0 register = 0010X010B

▲4: IICS0 register = 0010X000B

Δ 5: IICS0 register = 00000001B

Remark ▲: Always generated
Δ: Generated only when SPIE0 bit = 1
X: don't care

<2> When WTIM0 bit = 1 (after restart, extension code reception)

ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	SP

▲1 ▲2 ▲3 ▲4 ▲5 ▲6 Δ7

▲1: IICS0 register = 0010X010B

▲2: IICS0 register = 0010X110B

▲3: IICS0 register = 0010XX00B

▲4: IICS0 register = 0010X010B

▲5: IICS0 register = 0010X110B

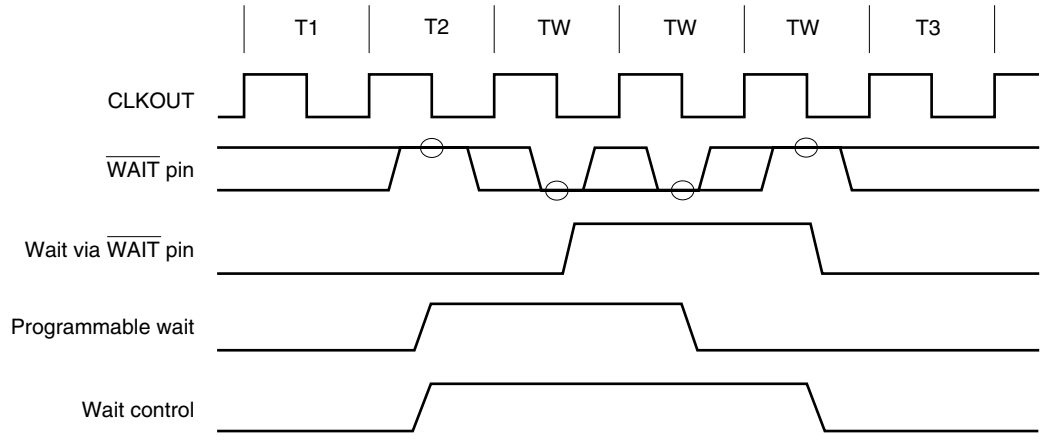
▲6: IICS0 register = 0010XX00B

Δ 7: IICS0 register = 00000001B

Remark ▲: Always generated
Δ: Generated only when SPIE0 bit = 1
X: don't care

<R> **Figure 18-1. Example of Inserting Wait States (2/2)**

(b) In multiplexed bus mode



Remark The circle ○ indicates the sampling timing.

18.6.4 Bus cycles in which wait function is valid

In the μPD70F3454GC-8EA-A and 70F3454F1-DA9-A, the number of waits can be specified for each memory block. The following shows the bus cycles in which the wait function is valid and the registers used for wait setting.

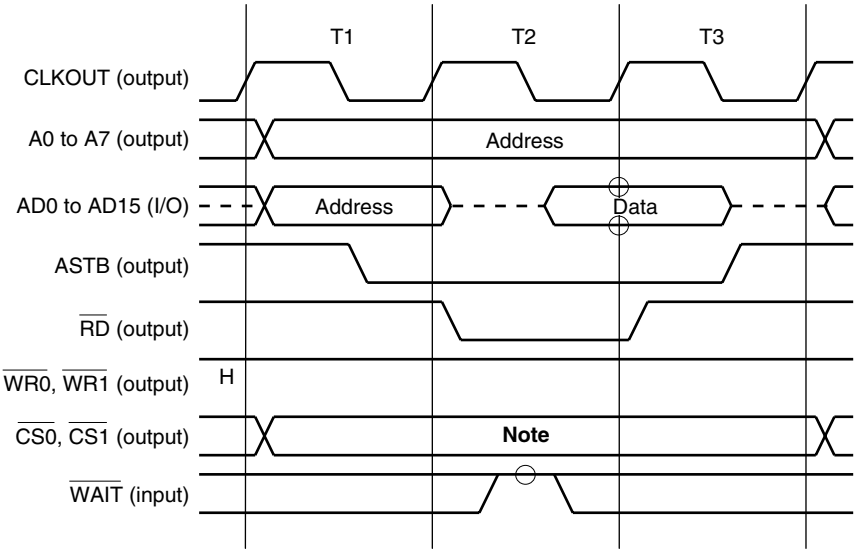
Table 18-2. Bus Cycles in Which Wait Function Is Valid

Bus Cycle	Wait Type	Programmable Wait Setting			Wait by WAIT Pin
		Register	Bit	Number of Waits	
SRAM, external ROM, external I/O cycles	Address setup wait	AWC	ASWn	0, 1	× (invalid)
	Address hold wait	AWC	AHWn	0, 1	× (invalid)
	Data wait	DWC0	DWn2 to DWn0	0 to 7	√ (valid)

Remark n = 0, 1

18.8 Bus Timing

(1) Read cycle (basic cycle)



Note Only the CS space that can be accessed becomes active.

Remarks 1. The circle ○ indicates the sampling timing.

2. The broken lines indicate the high-impedance state.

19.4 Transfer Modes

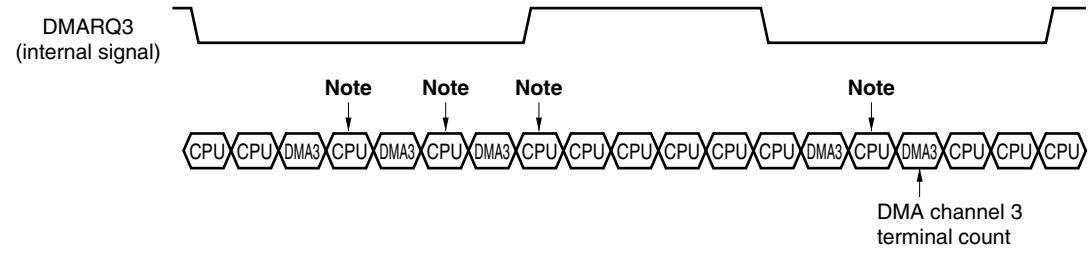
19.4.1 Single transfer mode

In single transfer mode, the DMAC releases the bus at each byte/halfword transfer. If there is a subsequent DMA transfer request, transfer is performed again once. This operation continues until a terminal count occurs.

When the DMAC has released the bus, if another higher priority DMA transfer request is issued, the higher priority DMA request always takes precedence. If another DMA transfer request with a lower priority occurs one clock after single transfer has been completed, however, this request does not take precedence even if the previous DMA transfer request signal with a higher priority remains active. DMA transfer with the newly requested lower priority request is executed after the CPU bus has been released.

Figures 19-1 to 19-4 show examples of single transfer.

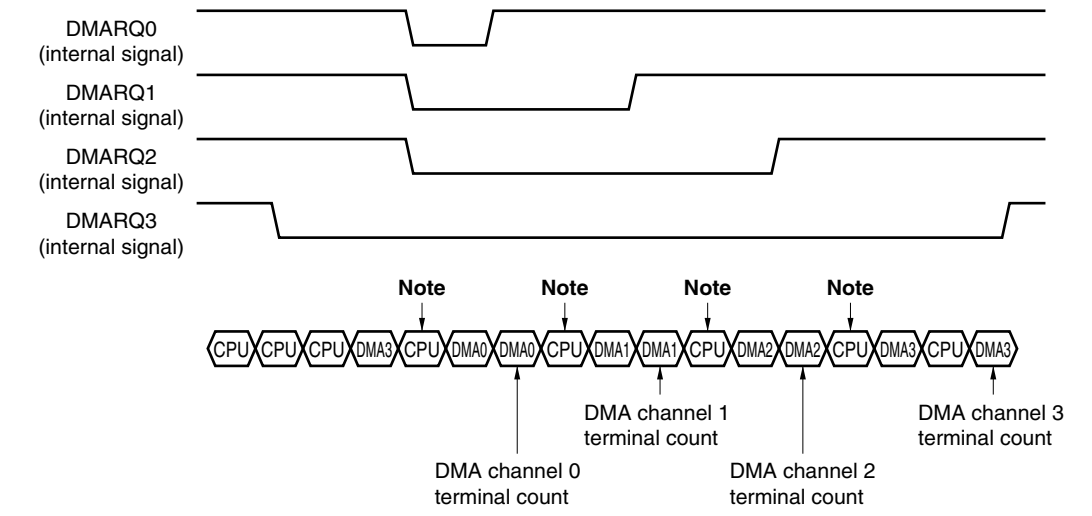
Figure 19-1. Single Transfer Example 1



Note The bus is always released.

Figure 19-2 shows an example of a single transfer in which a higher priority DMA request is issued. DMA channels 0 to 2 are in the block transfer mode and channel 3 is in the single transfer mode.

Figure 19-2. Single Transfer Example 2



Note The bus is always released.

CHAPTER 21 STANDBY FUNCTION

21.1 Overview

The power consumption of the system can be effectively reduced by using the standby modes in combination and selecting the appropriate mode for the application. The available standby modes are listed in Table 21-1.

Table 21-1. Standby Modes

Mode	Functional Outline
HALT mode	Mode to stop only the operating clock of the CPU
IDLE mode	Mode to stop all the operations of the internal circuit except the oscillator, PLL, CSIB in the slave mode, clock monitor, low-voltage detector (LVI), power-on-clear circuit (POC)
STOP mode	Mode to stop all the operations of the internal circuit except the CSIB in the slave mode, low-voltage detector (LVI), power-on-clear circuit (POC)

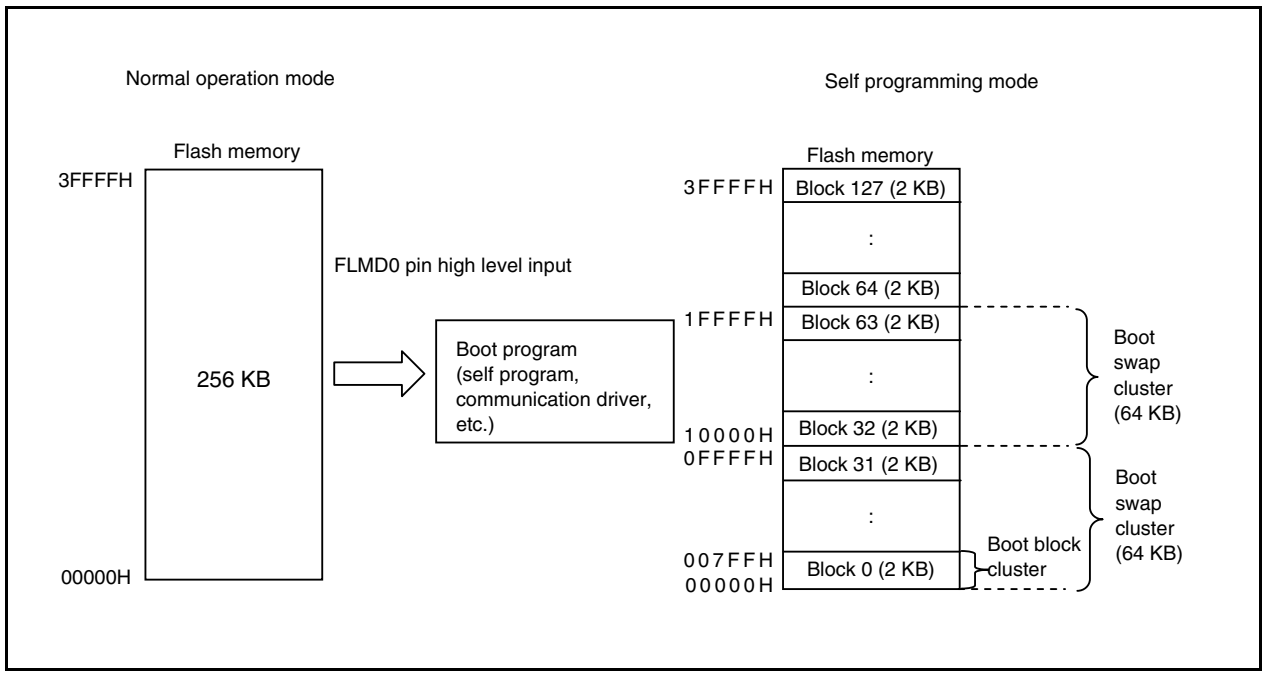
27.9.2 Features

(1) Flash memory self programming

Flash memory self programming is used to erase or write the flash memory by calling the flash function from a program stored in an area other than the flash memory area to be erased or written. To store the program that implements self programming in the area to be erased or written, copy the program to the internal RAM area, execute the program at the copy destination, and call the flash function.

To call the flash function, change the mode from the normal operation mode to the self programming mode by using the flash programming mode control register.

Figure 27-3. Self Programming



(a) Boot swap cluster

The contents of the boot swap cluster of the lower address side (00000H to 0FFFFH) and the boot swap cluster of the higher address side (10000H to 1FFFFH) can be interchanged while flash memory programming is performed.

(b) Boot block cluster

By specifying the boot block cluster from 00000H in 2 KB units, the contents of the boot block cluster can be protected from rewriting.

28.1.9 Characteristics of A/D converters 0 and 1

(T_A = –40 to +85°C, V_{DD0} = V_{DD1} = EV_{DD0} = EV_{DD1} = AV_{DD0} = AV_{DD1} = AV_{DD2} = AV_{REFP0} = AV_{REFP1} = 4.0 to 5.5 V, V_{SS0} = V_{SS1} = EV_{SS0} = EV_{SS1} = AV_{SS0} = AV_{SS1} = AV_{SS2} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			12	12	12	bit
Overall error[Note 1]					±10	LSB
Conversion time	t_{CONV}	f_{AD01} = 16 MHz, ADAnCTC register = 0BH or 0CH	2.0			μs
		f_{AD01} = 12 MHz, ADAnCTC register = 00H			7.42	μs
Zero scale error[Note 1]					±10	LSB
Full-scale error[Note 1]					±10	LSB
Integral linearity error[Note 1]					±4	LSB
Differential linearity error[Note 1]					±2.5	LSB
Analog reference voltage	AV_{DD}		4.0		5.5	V
Analog input voltage	V_{IAN}		AV_{SS}		AV_{DD}	V
AV_{DD} supply current[Note 2]	AI_{DD}	Operating		4.5	7.5	mA
	AI_{DDS}	In STOP mode[Note 3]		3.5	17.5	μs

Notes 1. Excludes quantization error (±0.5 LSB).

2. This value is for only one A/D converter (A/D converter 0 or 1).

3. Stop the operation of A/D converters 0 and 1 (ADnSCM.ADnCE bit = 0) before setting STOP mode.

Remarks 1. LSB: Least Significant Bit

2. f_{AD01}: Base clock of A/D converters 0 and 1

3. n = 0, 1

28.2.14 Low-voltage detector (LVI)

(T_A = –40 to +85°C, V_{DD0} = V_{DD1} = EV_{DD0} = EV_{DD1} = EV_{DD2} = AV_{DD0} = AV_{DD1} = AV_{DD2} = 3.5 to 5.5 V, V_{SS0} = V_{SS1} = EV_{SS0} = EV_{SS1} = EV_{SS2} = AV_{SS0} = AV_{SS1} = AV_{SS2} = 0 V, C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	TYP.	MAX.	Unit
LVI detection voltage	V_{LVI0}		LVIS.LVIS0 bit = 0	4.2	4.4	4.6	V
	V_{LVI1}		LVIS.LVIS0 bit = 1	4.0	4.2	4.4	V
Response time 1[Note]	t_{LD}	<102>	After V_{DD0} and V_{DD1} reach V_{LVI0}/V_{LVI1} (MAX.) or drop to V_{LVI0}/V_{LVI1} (MIN.)		0.2	2.0	ms
Minimum width of V_{DD0}, V_{DD1}	t_{LW}	<103>		0.2			ms
Reference voltage stabilization wait time	t_{LWAIT}	<104>	After V_{DD0} and V_{DD1} reach POC detection voltage (MIN.) and the LVIM.LVION bit is changed from 0 to 1		0.1		ms

Note The time required to output an interrupt request signal (INTLVIL, INTLVIH) or internal reset signal (LVIRES) after the LVI detection voltage is detected.