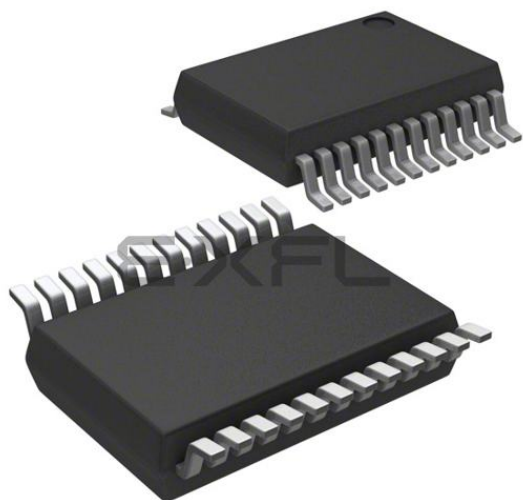




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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	19
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-LSSOP (0.220", 5.60mm Width)
Supplier Device Package	24-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f213g2cnsp-w4

1.1.2 Specifications

Tables 1.1 and 1.2 outline the Specifications for R8C/3GC Group.

Table 1.1 Specifications for R8C/3GC Group (1)

Item	Function	Specification
CPU	Central processing unit	R8C CPU core • Number of fundamental instructions: 89 • Minimum instruction execution time: 50 ns ($f(XIN) = 20$ MHz, $VCC = 2.7$ to 5.5 V) 200 ns ($f(XIN) = 5$ MHz, $VCC = 1.8$ to 5.5 V) • Multiplier: 16 bits $\times$ 16 bits $\rightarrow$ 32 bits • Multiply-accumulate instruction: 16 bits $\times$ 16 bits + 32 bits $\rightarrow$ 32 bits • Operation mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM, RAM, Data flash	Refer to Table 1.3 Product List for R8C/3GC Group .
Power Supply Voltage Detection	Voltage detection circuit	• Power-on reset • Voltage detection 3 (detection level of voltage detection 0 and voltage detection 1 selectable)
I/O Ports	Programmable I/O ports	• Input-only: 1 pin • CMOS I/O ports: 19, selectable pull-up resistor • High current drive ports: 19
Clock	Clock generation circuits	4 circuits: XIN clock oscillation circuit, XCIN clock oscillation circuit (32 kHz), High-speed on-chip oscillator (with frequency adjustment function), Low-speed on-chip oscillator • Oscillation stop detection: XIN clock oscillation stop detection function • Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16 • Low power consumption modes: - Standard operating mode (high-speed clock, low-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode
Interrupts		Real-time clock (timer RE) • Number of interrupt vectors: 69 • External Interrupt: 7 ($INT \times 3$, Key input $\times 4$) • Priority levels: 7 levels
Watchdog Timer		• 14 bits $\times$ 1 (with prescaler) • Reset start selectable • Low-speed on-chip oscillator for watchdog timer selectable
DTC (Data Transfer Controller)		• 1 channel • Activation sources: 23 • Transfer modes: 2 (normal mode, repeat mode)
Timer	Timer RA	8 bits $\times$ 1 (with 8-bit prescaler) Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RB	8 bits $\times$ 1 (with 8-bit prescaler) Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timer RC	16 bits $\times$ 1 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin)
	Timer RE	8 bits $\times$ 1 Real-time clock mode (count seconds, minutes, hours, days of week)

1.2 Product List

Table 1.3 lists Product List for R8C/3GC Group, and Figure 1.1 shows a Part Number, Memory Size, and Package of R8C/3GC Group.

Table 1.3 Product List for R8C/3GC Group

Current of Oct 2010

Part No.	ROM Capacity		RAM Capacity	Package Type	Remarks
	Program ROM	Data flash			
R5F213G2CNNP	8 Kbytes	1 Kbyte × 4	1 Kbyte	PWQN0024KC-A	N version
R5F213G4CNNP	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PWQN0024KC-A	
R5F213G5CNNP	24 Kbytes	1 Kbyte × 4	2 Kbytes	PWQN0024KC-A	
R5F213G6CNNP	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PWQN0024KC-A	
R5F213G1CNSP	4 Kbytes	1 Kbyte × 4	512 byte	PLSP0024JB-A	
R5F213G2CNSP	8 Kbytes	1 Kbyte × 4	1 Kbyte	PLSP0024JB-A	
R5F213G4CNSP	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PLSP0024JB-A	
R5F213G5CNSP	24 Kbytes	1 Kbyte × 4	2 Kbytes	PLSP0024JB-A	
R5F213G6CNSP	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PLSP0024JB-A	
R5F213G1CDSP	4 Kbytes	1 Kbyte × 4	512 byte	PLSP0024JB-A	D version
R5F213G2CDSP	8 Kbytes	1 Kbyte × 4	1 Kbyte	PLSP0024JB-A	
R5F213G4CDSP	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PLSP0024JB-A	
R5F213G5CDSP	24 Kbytes	1 Kbyte × 4	2 Kbytes	PLSP0024JB-A	
R5F213G6CDSP	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PLSP0024JB-A	

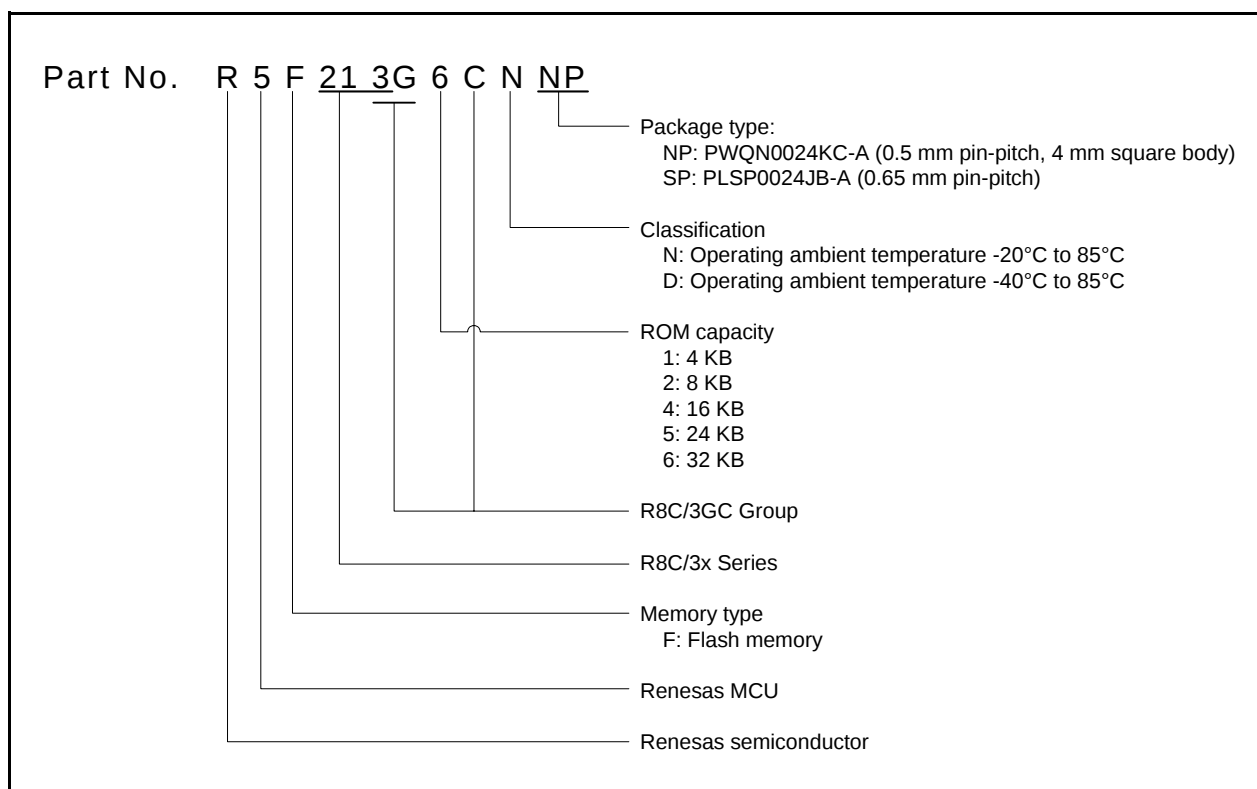


Figure 1.1 Part Number, Memory Size, and Package of R8C/3GC Group

Table 1.4 Pin Name Information by Pin Number

Pin Number	Control Pin	Port	I/O Pin Functions for Peripheral Modules					
			Interrupt	Timer	Serial Interface	SSU	I ² C bus	A/D Converter, D/A Converter, Comparator B
1	MODE							
2	RESET							
3	XOUT(/XCOUT)	P4_7						
4	VSS/AVSS							
5	XIN(/XCIN)	P4_6						
6	VCC/AVCC							
7		P3_7		TRAO	(RXD2/SCL2/ TXD2/SDA2)	SSO	SDA	
8		P3_5		(TRCIOD)	(CLK2)	SSCK	SCL	
9		P3_4		(TRCIOC)	(RXD2/SCL2/ TXD2/SDA2)	SSI		IVREF3
10		P3_3	INT3	(TRCCLK)	(CTS2/RTS2)	SCS		IVCMP3
11		P4_5	INT0		(RXD2/SCL2)			ADTRG
12		P1_7	INT1	(TRAIO)				IVCMP1
13		P1_6			(CLK0)			IVREF1
14		P1_5	(INT1)	(TRAIO)	(RXD0)			
15		P1_4		(TRCCLK)	(TXD0)			
16		P1_3	KI3	TRBO/ (TRCIOC)				AN11
17		P1_2	KI2	(TRCIOB)				AN10
18		P1_1	KI1	(TRCIOA/ TRCTRG)				AN9
19		P1_0	KI0	(TRCIOD)				AN8
20		P0_7		(TRCIOC)				AN0/DA1
21		P0_6		(TRCIOD)				AN1/DA0
22		P0_2		(TRCIOA/ TRCTRG)				AN5
23		P0_1		(TRCIOA/ TRCTRG)				AN6
24		P4_2						VREF

Note:

1. Can be assigned to the pin in parentheses by a program.

Table 1.5 Pin Name Information by Pin Number

Pin Number	Control Pin	Port	I/O Pin Functions for Peripheral Modules					
			Interrupt	Timer	Serial Interface	SSU	I ² C bus	A/D Converter, D/A Converter, Comparator B
1		P0_2		(TRCIOA/TRCTRG)				AN5
2		P0_1		(TRCIOA/TRCTRG)				AN6
3		P4_2						VREF
4	MODE							
5	$\overline{\text{RESET}}$							
6	XOUT(/XCOUT)	P4_7						
7	VSS/AVSS							
8	XIN(/XCIN)	P4_6						
9	VCC/AVCC							
10		P3_7		TRAO	(RXD2/SCL2/TXD2/SDA2)	SSO	SDA	
11		P3_5		(TRCIOD)	(CLK2)	SSCK	SCL	
12		P3_4		(TRCIOC)	(RXD2/SCL2/TXD2/SDA2)	SSI		IVREF3
13		P3_3	$\overline{\text{INT3}}$	(TRCCLK)	($\overline{\text{CTS2}}$ / $\overline{\text{RTS2}}$)	$\overline{\text{SCS}}$		IVCMP3
14		P4_5	$\overline{\text{INT0}}$		(RXD2/SCL2)			$\overline{\text{ADTRG}}$
15		P1_7	$\overline{\text{INT1}}$	(TRAIO)				IVCMP1
16		P1_6			(CLK0)			IVREF1
17		P1_5	($\overline{\text{INT1}}$)	(TRAIO)	(RXD0)			
18		P1_4		(TRCCLK)	(TXD0)			
19		P1_3	$\overline{\text{KI3}}$	TRBO/(TRCIOC)				AN11
20		P1_2	$\overline{\text{KI2}}$	(TRCIOB)				AN10
21		P1_1	$\overline{\text{KI1}}$	(TRCIOA/TRCTRG)				AN9
22		P1_0	$\overline{\text{KI0}}$	(TRCIOD)				AN8
23		P0_7		(TRCIOC)				AN0/DA1
24		P0_6		(TRCIOD)				AN1/DA0

Note:

1. Can be assigned to the pin in parentheses by a program.

1.5 Pin Functions

Tables 1.6 and 1.7 list Pin Functions.

Table 1.6 Pin Functions (1)

Item	Pin Name	I/O Type	Description
Power supply input	VCC, VSS	–	Apply 1.8 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	–	Power supply for the A/D converter. Connect a capacitor between AVCC and AVSS.
Reset input	$\overline{\text{RESET}}$	I	Input “L” on this pin resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
XIN clock input	XIN	I	These pins are provided for XIN clock generation circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins ⁽¹⁾ . To use an external clock, input it to the XOUT pin and leave the XIN pin open.
XIN clock output	XOUT	I/O	
XCIN clock input	XCIN	I	These pins are provided for XCIN clock generation circuit I/O. Connect a crystal oscillator between the XCIN and XCOU pins ⁽¹⁾ . To use an external clock, input it to the XCIN pin and leave the XCOU pin open.
XCIN clock output	XCOU	O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$, $\overline{\text{INT1}}$, $\overline{\text{INT3}}$	I	$\overline{\text{INT}}$ interrupt input pins. $\overline{\text{INT0}}$ is timer RB, and RC input pin.
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Key input interrupt input pins
Timer RA	TRAIO	I/O	Timer RA I/O pin
	TRA0	O	Timer RA output pin
Timer RB	TRBO	O	Timer RB output pin
Timer RC	TRCCLK	I	External clock input pin
	TRCTRG	I	External trigger input pin
	TRCIOA, TRCIOB, TRCIOC, TRCIOD	I/O	Timer RC I/O pins
Serial interface	CLK0, CLK2	I/O	Transfer clock I/O pins
	RXD0, RXD2	I	Serial data input pins
	TXD0, TXD2	O	Serial data output pins
	$\overline{\text{CTS2}}$	I	Transmission control input pin
	$\overline{\text{RTS2}}$	O	Reception control output pin
	SCL2	I/O	I ² C mode clock I/O pin
	SDA2	I/O	I ² C mode data I/O pin
I ² C bus	SCL	I/O	Clock I/O pin
	SDA	I/O	Data I/O pin
SSU	SSI	I/O	Data I/O pin
	$\overline{\text{SCS}}$	I/O	Chip-select signal I/O pin
	SSCK	I/O	Clock I/O pin
	SSO	I/O	Data I/O pin

I: Input O: Output I/O: Input and output

Note:

1. Refer to the oscillator manufacturer for oscillation characteristics.

Table 4.2 SFR Information (2) (1)

Address	Register	Symbol	After Reset
003Ah	Voltage Monitor 2 Circuit Control Register	VW2C	10000010b
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			
0040h			
0041h	Flash Memory Ready Interrupt Control Register	FMRDYIC	XXXXX000b
0042h			
0043h			
0044h			
0045h			
0046h			
0047h	Timer RC Interrupt Control Register	TRCIC	XXXXX000b
0048h			
0049h			
004Ah	Timer RE Interrupt Control Register	TREIC	XXXXX000b
004Bh	UART2 Transmit Interrupt Control Register	S2TIC	XXXXX000b
004Ch	UART2 Receive Interrupt Control Register	S2RIC	XXXXX000b
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh	SSU Interrupt Control Register / IIC bus Interrupt Control Register (2)	SSUIC / IICIC	XXXXX000b
0050h			
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h			
0054h			
0055h			
0056h	Timer RA Interrupt Control Register	TRAIC	XXXXX000b
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh			
005Ch			
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh	UART2 Bus Collision Detection Interrupt Control Register	U2BCNIC	XXXXX000b
005Fh			
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh			
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h	Voltage Monitor 1 Interrupt Control Register	VCMP1IC	XXXXX000b
0073h	Voltage Monitor 2 Interrupt Control Register	VCMP2IC	XXXXX000b
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

X: Undefined

Notes:

1. The blank areas are reserved and cannot be accessed by users.
2. Selectable by the IICSEL bit in the SSUICSR register.

Table 4.6 SFR Information (6) (1)

Address	Register	Symbol	After Reset
0140h			
0141h			
0142h			
0143h			
0144h			
0145h			
0146h			
0147h			
0148h			
0149h			
014Ah			
014Bh			
014Ch			
014Dh			
014Eh			
014Fh			
0150h			
0151h			
0152h			
0153h			
0154h			
0155h			
0156h			
0157h			
0158h			
0159h			
015Ah			
015Bh			
015Ch			
015Dh			
015Eh			
015Fh			
0160h			
0161h			
0162h			
0163h			
0164h			
0165h			
0166h			
0167h			
0168h			
0169h			
016Ah			
016Bh			
016Ch			
016Dh			
016Eh			
016Fh			
0170h			
0171h			
0172h			
0173h			
0174h			
0175h			
0176h			
0177h			
0178h			
0179h			
017Ah			
017Bh			
017Ch			
017Dh			
017Eh			
017Fh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.11 SFR Information (11) ⁽¹⁾

Address	Register	Symbol	After Reset
2CB0h	DTC Control Data 14	DTCD14	XXh
2CB1h			XXh
2CB2h			XXh
2CB3h			XXh
2CB4h			XXh
2CB5h			XXh
2CB6h			XXh
2CB7h			XXh
2CB8h	DTC Control Data 15	DTCD15	XXh
2CB9h			XXh
2CBAh			XXh
2CBBh			XXh
2CBCh			XXh
2CBDh			XXh
2CBEh			XXh
2CBFh			XXh
2CC0h	DTC Control Data 16	DTCD16	XXh
2CC1h			XXh
2CC2h			XXh
2CC3h			XXh
2CC4h			XXh
2CC5h			XXh
2CC6h			XXh
2CC7h			XXh
2CC8h	DTC Control Data 17	DTCD17	XXh
2CC9h			XXh
2CCAh			XXh
2CCBh			XXh
2CCCh			XXh
2CCDh			XXh
2CCEh			XXh
2CCFh			XXh
2CD0h	DTC Control Data 18	DTCD18	XXh
2CD1h			XXh
2CD2h			XXh
2CD3h			XXh
2CD4h			XXh
2CD5h			XXh
2CD6h			XXh
2CD7h			XXh
2CD8h	DTC Control Data 19	DTCD19	XXh
2CD9h			XXh
2CDAh			XXh
2CDBh			XXh
2CDCh			XXh
2CDDh			XXh
2CDEh			XXh
2CDFh			XXh
2CE0h	DTC Control Data 20	DTCD20	XXh
2CE1h			XXh
2CE2h			XXh
2CE3h			XXh
2CE4h			XXh
2CE5h			XXh
2CE6h			XXh
2CE7h			XXh
2CE8h	DTC Control Data 21	DTCD21	XXh
2CE9h			XXh
2CEAh			XXh
2CEBh			XXh
2CECh			XXh
2CEDh			XXh
2CEEh			XXh
2CEFh			XXh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 5.2 Recommended Operating Conditions

Symbol	Parameter				Conditions	Standard			Unit
						Min.	Typ.	Max.	
Vcc/AVcc	Supply voltage					1.8	–	5.5	V
Vss/AVss	Supply voltage					–	0	–	V
VIH	Input “H” voltage	Other than CMOS input				0.8 Vcc	–	Vcc	V
		CMOS input	Input level switching function (I/O port)	Input level selection: 0.35 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0.5 Vcc	–	Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0.55 Vcc	–	Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0.65 Vcc	–	Vcc	V
			Input level selection: 0.5 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0.65 Vcc	–	Vcc	V	
				2.7 V ≤ Vcc < 4.0 V	0.7 Vcc	–	Vcc	V	
				1.8 V ≤ Vcc < 2.7 V	0.8 Vcc	–	Vcc	V	
			Input level selection: 0.7 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0.85 Vcc	–	Vcc	V	
				2.7 V ≤ Vcc < 4.0 V	0.85 Vcc	–	Vcc	V	
				1.8 V ≤ Vcc < 2.7 V	0.85 Vcc	–	Vcc	V	
	External clock input (XOUT)				1.2	–	Vcc	V	
VIL	Input “L” voltage	Other than CMOS input				0	–	0.2 Vcc	V
		CMOS input	Input level switching function (I/O port)	Input level selection: 0.35 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0	–	0.2 Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0	–	0.2 Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0	–	0.2 Vcc	V
			Input level selection: 0.5 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0	–	0.4 Vcc	V	
				2.7 V ≤ Vcc < 4.0 V	0	–	0.3 Vcc	V	
				1.8 V ≤ Vcc < 2.7 V	0	–	0.2 Vcc	V	
			Input level selection: 0.7 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0	–	0.55 Vcc	V	
				2.7 V ≤ Vcc < 4.0 V	0	–	0.45 Vcc	V	
				1.8 V ≤ Vcc < 2.7 V	0	–	0.35 Vcc	V	
	External clock input (XOUT)				0	–	0.4	V	
IOH(sum)	Peak sum output “H” current	Sum of all pins IOH(peak)				–	–	–160	mA
IOH(sum)	Average sum output “H” current	Sum of all pins IOH(avg)				–	–	–80	mA
IOH(peak)	Peak output “H” current	Drive capacity Low				–	–	–10	mA
		Drive capacity High				–	–	–40	mA
IOH(avg)	Average output “H” current	Drive capacity Low				–	–	–5	mA
		Drive capacity High				–	–	–20	mA
IOL(sum)	Peak sum output “L” current	Sum of all pins IOL(peak)				–	–	160	mA
IOL(sum)	Average sum output “L” current	Sum of all pins IOL(avg)				–	–	80	mA
IOL(peak)	Peak output “L” current	Drive capacity Low				–	–	10	mA
		Drive capacity High				–	–	40	mA
IOL(avg)	Average output “L” current	Drive capacity Low				–	–	5	mA
		Drive capacity High				–	–	20	mA
f(XIN)	XIN clock input oscillation frequency				2.7 V ≤ Vcc ≤ 5.5 V	–	–	20	MHz
					1.8 V ≤ Vcc < 2.7 V	–	–	5	MHz
f(XCIN)	XCIN clock input oscillation frequency				1.8 V ≤ Vcc ≤ 5.5 V	–	32.768	50	kHz
fOCO40M	When used as the count source for timer RC ⁽³⁾				2.7 V ≤ Vcc ≤ 5.5 V	32	–	40	MHz
fOCO-F	fOCO-F frequency				2.7 V ≤ Vcc ≤ 5.5 V	–	–	20	MHz
					1.8 V ≤ Vcc < 2.7 V	–	–	5	MHz
–	System clock frequency				2.7 V ≤ Vcc ≤ 5.5 V	–	–	20	MHz
					1.8 V ≤ Vcc < 2.7 V	–	–	5	MHz
f(BCLK)	CPU clock frequency				2.7 V ≤ Vcc ≤ 5.5 V	–	–	20	MHz
					1.8 V ≤ Vcc < 2.7 V	–	–	5	MHz

Notes:

1. V_{CC} = 1.8 to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.
3. f_{OCO40M} can be used as the count source for timer RC in the range of V_{CC} = 2.7 V to 5.5V.

Table 5.3 A/D Converter Characteristics

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
–	Resolution		Vref = AVCC		–	–	10	Bit
–	Absolute accuracy	10-bit mode	Vref = AVCC = 5.0 V	AN0, AN1, AN5, AN6 input, AN8 to AN11 input	–	–	±3	LSB
			Vref = AVCC = 3.3 V	AN0, AN1, AN5, AN6 input, AN8 to AN11 input	–	–	±5	LSB
			Vref = AVCC = 3.0 V	AN0, AN1, AN5, AN6 input, AN8 to AN11 input	–	–	±5	LSB
			Vref = AVCC = 2.2 V	AN0, AN1, AN5, AN6 input, AN8 to AN11 input	–	–	±5	LSB
		8-bit mode	Vref = AVCC = 5.0 V	AN0, AN1, AN5, AN6 input, AN8 to AN11 input	–	–	±2	LSB
			Vref = AVCC = 3.3 V	AN0, AN1, AN5, AN6 input, AN8 to AN11 input	–	–	±2	LSB
			Vref = AVCC = 3.0 V	AN0, AN1, AN5, AN6 input, AN8 to AN11 input	–	–	±2	LSB
			Vref = AVCC = 2.2 V	AN0, AN1, AN5, AN6 input, AN8 to AN11 input	–	–	±2	LSB
φAD	A/D conversion clock		4.0 V ≤ Vref = AVCC ≤ 5.5 V (2)		2	–	20	MHz
			3.2 V ≤ Vref = AVCC ≤ 5.5 V (2)		2	–	16	MHz
			2.7 V ≤ Vref = AVCC ≤ 5.5 V (2)		2	–	10	MHz
			2.2 V ≤ Vref = AVCC ≤ 5.5 V (2)		2	–	5	MHz
–	Tolerance level impedance				–	3	–	kΩ
tCONV	Conversion time	10-bit mode	Vref = AVCC = 5.0 V, φAD = 20 MHz		2.2	–	–	μs
		8-bit mode	Vref = AVCC = 5.0 V, φAD = 20 MHz		2.2	–	–	μs
tsAMP	Sampling time		φAD = 20 MHz		0.8	–	–	μs
Ivref	Vref current		VCC = 5 V, XIN = f1 = φAD = 20 MHz		–	45	–	μA
Vref	Reference voltage				2.2	–	AVCC	V
VIa	Analog input voltage (3)				0	–	Vref	V
OCVREF	On-chip reference voltage		2 MHz ≤ φAD ≤ 4 MHz		1.19	1.34	1.49	V

Notes:

- $V_{CC}/AV_{CC} = V_{ref} = 2.2$ to 5.5 V , $V_{SS} = 0\text{ V}$ and $T_{opr} = -20$ to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
- The A/D conversion result will be undefined in wait mode, stop mode, when the flash memory stops, and in low-current-consumption mode. Do not perform A/D conversion in these states or transition to these states during A/D conversion.
- When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 5.4 D/A Converter Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
—	Resolution		—	—	8	Bit
—	Absolute accuracy		—	—	2.5	LSB
t_{su}	Setup time		—	—	3	μs
R_o	Output resistor		—	6	—	$k\Omega$
I_{vref}	Reference power input current	(Note 2)	—	—	1.5	mA

Notes:

1. $V_{CC}/AV_{CC} = V_{ref} = 2.7$ to 5.5 V and $T_{opr} = -20$ to $85^{\circ}C$ (N version) / -40 to $85^{\circ}C$ (D version), unless otherwise specified.
2. This applies when one D/A converter is used and the value of the DA_i register ($i = 0$ or 1) for the unused D/A converter is $00h$. The resistor ladder of the A/D converter is not included.

Table 5.5 Comparator B Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{ref}	$IVREF1$, $IVREF3$ input reference voltage		0	—	$V_{CC} - 1.4$	V
V_i	$IVCMP1$, $IVCMP3$ input voltage		-0.3	—	$V_{CC} + 0.3$	V
—	Offset		—	5	100	mV
t_d	Comparator output delay time ⁽²⁾	$V_i = V_{ref} \pm 100$ mV	—	0.1	—	μs
I_{CMP}	Comparator operating current	$V_{CC} = 5.0$ V	—	17.5	—	μA

Notes:

1. $V_{CC} = 2.7$ to 5.5 V, $T_{opr} = -20$ to $85^{\circ}C$ (N version) / -40 to $85^{\circ}C$ (D version), unless otherwise specified.
2. When the digital filter is disabled.

Table 5.8 Voltage Detection 0 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet0	Voltage detection level Vdet0_0 (2)		1.80	1.90	2.05	V
	Voltage detection level Vdet0_1 (2)		2.15	2.35	2.50	V
	Voltage detection level Vdet0_2 (2)		2.70	2.85	3.05	V
	Voltage detection level Vdet0_3 (2)		3.55	3.80	4.05	V
–	Voltage detection 0 circuit response time (4)	At the falling of Vcc from 5 V to (Vdet0_0 – 0.1) V	–	6	150	μs
–	Voltage detection circuit self power consumption	VCA25 = 1, Vcc = 5.0 V	–	1.5	–	μA
td(E-A)	Waiting time until voltage detection circuit operation starts (3)		–	–	100	μs

Notes:

1. The measurement condition is Vcc = 1.8 V to 5.5 V and Topr = –20 to 85°C (N version) / –40 to 85°C (D version).
2. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.
4. Time until the voltage monitor 0 reset is generated after the voltage passes Vdet0.

Table 5.9 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet1	Voltage detection level Vdet1_0 (2)	At the falling of Vcc	2.00	2.20	2.40	V
	Voltage detection level Vdet1_1 (2)	At the falling of Vcc	2.15	2.35	2.55	V
	Voltage detection level Vdet1_2 (2)	At the falling of Vcc	2.30	2.50	2.70	V
	Voltage detection level Vdet1_3 (2)	At the falling of Vcc	2.45	2.65	2.85	V
	Voltage detection level Vdet1_4 (2)	At the falling of Vcc	2.60	2.80	3.00	V
	Voltage detection level Vdet1_5 (2)	At the falling of Vcc	2.75	2.95	3.15	V
	Voltage detection level Vdet1_6 (2)	At the falling of Vcc	2.85	3.10	3.40	V
	Voltage detection level Vdet1_7 (2)	At the falling of Vcc	3.00	3.25	3.55	V
	Voltage detection level Vdet1_8 (2)	At the falling of Vcc	3.15	3.40	3.70	V
	Voltage detection level Vdet1_9 (2)	At the falling of Vcc	3.30	3.55	3.85	V
	Voltage detection level Vdet1_A (2)	At the falling of Vcc	3.45	3.70	4.00	V
	Voltage detection level Vdet1_B (2)	At the falling of Vcc	3.60	3.85	4.15	V
	Voltage detection level Vdet1_C (2)	At the falling of Vcc	3.75	4.00	4.30	V
	Voltage detection level Vdet1_D (2)	At the falling of Vcc	3.90	4.15	4.45	V
	Voltage detection level Vdet1_E (2)	At the falling of Vcc	4.05	4.30	4.60	V
	Voltage detection level Vdet1_F (2)	At the falling of Vcc	4.20	4.45	4.75	V
–	Hysteresis width at the rising of Vcc in voltage detection 1 circuit	Vdet1_0 to Vdet1_5 selected	–	0.07	–	V
		Vdet1_6 to Vdet1_F selected	–	0.10	–	V
–	Voltage detection 1 circuit response time (3)	At the falling of Vcc from 5 V to (Vdet1_0 – 0.1) V	–	60	150	μs
–	Voltage detection circuit self power consumption	VCA26 = 1, Vcc = 5.0 V	–	1.7	–	μA
td(E-A)	Waiting time until voltage detection circuit operation starts (4)		–	–	100	μs

Notes:

1. The measurement condition is Vcc = 1.8 V to 5.5 V and Topr = –20 to 85°C (N version) / –40 to 85°C (D version).
2. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
3. Time until the voltage monitor 1 interrupt request is generated after the voltage passes Vdet1.
4. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

**Table 5.12 High-speed On-Chip Oscillator Circuit Electrical Characteristics
(Package Type: PWQN0024KC-A)**

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
—	High-speed on-chip oscillator frequency after reset	$V_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$ $-20^{\circ}\text{C} \leq T_{opr} \leq 85^{\circ}\text{C}$	37.80	40	42.60	MHz
	High-speed on-chip oscillator frequency when the FRA4 register correction value is written into the FRA1 register and the FRA5 register correction value into the FRA3 register ⁽²⁾	$V_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$ $-20^{\circ}\text{C} \leq T_{opr} \leq 85^{\circ}\text{C}$	34.836	36.864	39.261	MHz
	High-speed on-chip oscillator frequency when the FRA6 register correction value is written into the FRA1 register and the FRA7 register correction value into the FRA3 register	$V_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$ $-20^{\circ}\text{C} \leq T_{opr} \leq 85^{\circ}\text{C}$	30.24	32	34.08	MHz
—	Oscillation stability time	$V_{CC} = 5.0 \text{ V}$, $T_{opr} = 25^{\circ}\text{C}$	—	0.5	3	ms
—	Self power consumption at oscillation	$V_{CC} = 5.0 \text{ V}$, $T_{opr} = 25^{\circ}\text{C}$	—	400	—	μA

Notes:

1. $V_{CC} = 1.8$ to 5.5 V , $T_{opr} = -20$ to 85°C (N version), unless otherwise specified.
2. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

**Table 5.13 High-speed On-Chip Oscillator Circuit Electrical Characteristics
(Package Type: PLSP0024JB-A)**

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
—	High-speed on-chip oscillator frequency after reset	$V_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$ $-20^{\circ}\text{C} \leq T_{opr} \leq 85^{\circ}\text{C}$	38.4	40	41.6	MHz
		$V_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$ $-40^{\circ}\text{C} \leq T_{opr} \leq 85^{\circ}\text{C}$	38.0	40	42.0	MHz
	High-speed on-chip oscillator frequency when the FRA4 register correction value is written into the FRA1 register and the FRA5 register correction value into the FRA3 register ⁽²⁾	$V_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$ $-20^{\circ}\text{C} \leq T_{opr} \leq 85^{\circ}\text{C}$	35.389	36.864	38.338	MHz
		$V_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$ $-40^{\circ}\text{C} \leq T_{opr} \leq 85^{\circ}\text{C}$	35.020	36.864	38.707	MHz
	High-speed on-chip oscillator frequency when the FRA6 register correction value is written into the FRA1 register and the FRA7 register correction value into the FRA3 register	$V_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$ $-20^{\circ}\text{C} \leq T_{opr} \leq 85^{\circ}\text{C}$	30.72	32	33.28	MHz
		$V_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$ $-40^{\circ}\text{C} \leq T_{opr} \leq 85^{\circ}\text{C}$	30.40	32	33.60	MHz
—	Oscillation stability time	$V_{CC} = 5.0 \text{ V}$, $T_{opr} = 25^{\circ}\text{C}$	—	0.5	3	ms
—	Self power consumption at oscillation	$V_{CC} = 5.0 \text{ V}$, $T_{opr} = 25^{\circ}\text{C}$	—	400	—	μA

Notes:

1. $V_{CC} = 1.8$ to 5.5 V , $T_{opr} = -20$ to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

Table 5.14 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		60	125	250	kHz
—	Oscillation stability time	$V_{CC} = 5.0 \text{ V}$, $T_{opr} = 25^{\circ}\text{C}$	—	30	100	μs
—	Self power consumption at oscillation	$V_{CC} = 5.0 \text{ V}$, $T_{opr} = 25^{\circ}\text{C}$	—	2	—	μA

Note:

1. $V_{CC} = 1.8$ to 5.5 V , $T_{opr} = -20$ to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.

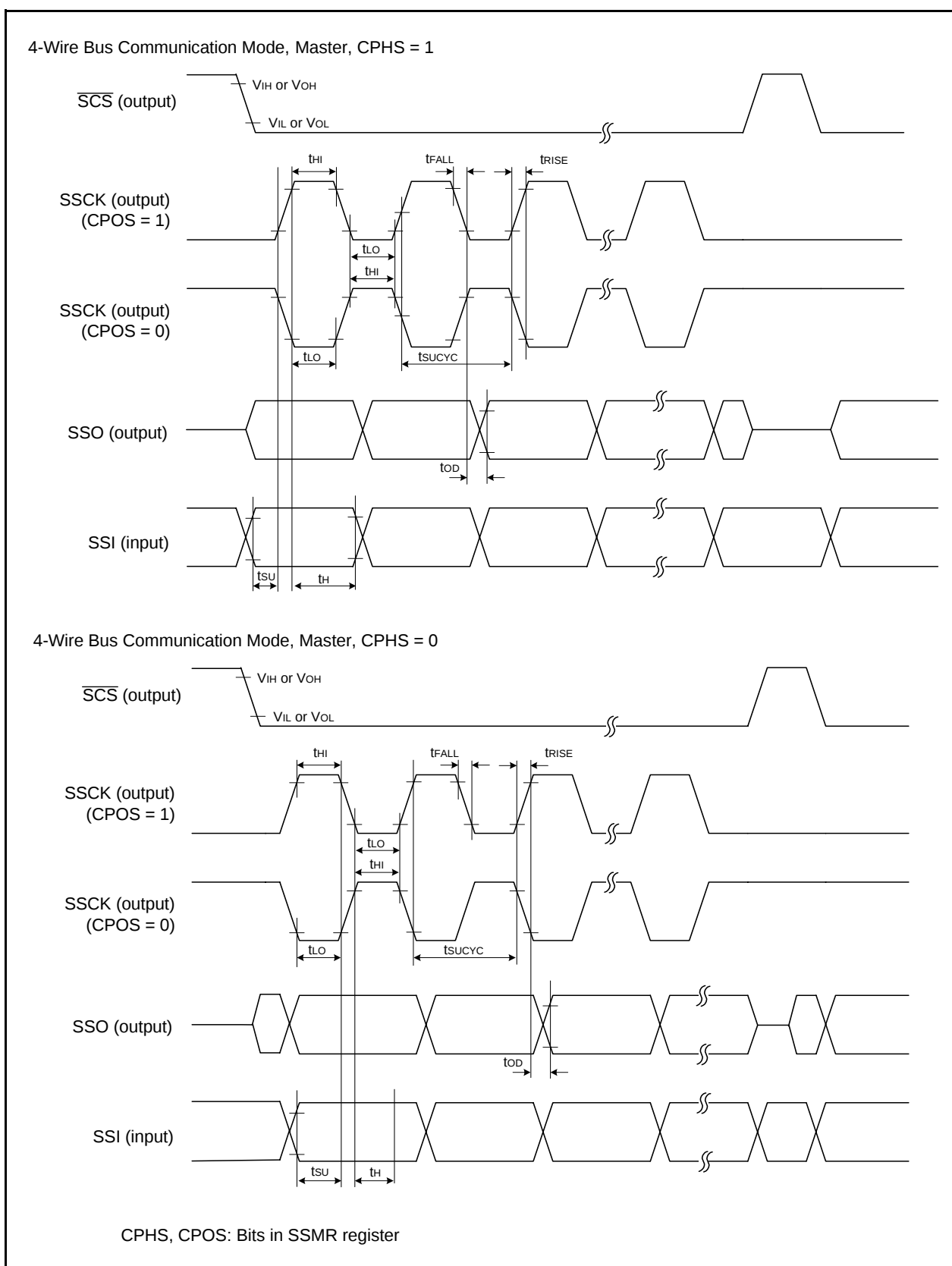


Figure 5.4 I/O Timing of Synchronous Serial Communication Unit (SSU) (Master)

Table 5.18 Electrical Characteristics (1) [4.2 V ≤ Vcc ≤ 5.5 V]

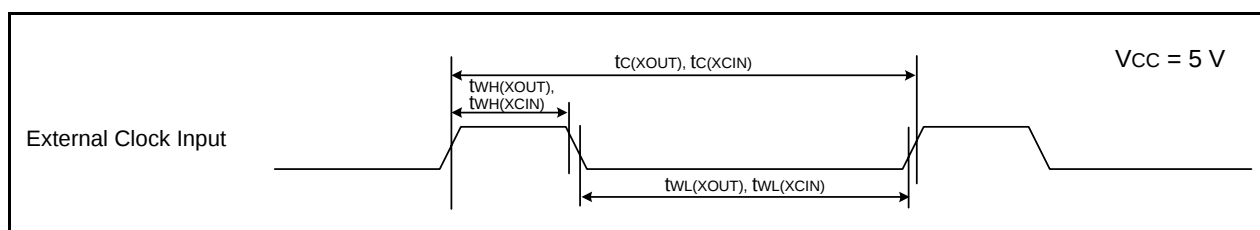
Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
VOH	Output "H" voltage	Other than XOUT	Drive capacity High Vcc = 5 V	IOH = -20 mA	Vcc - 2.0	—	Vcc	V
			Drive capacity Low Vcc = 5 V	IOH = -5 mA	Vcc - 2.0	—	Vcc	V
		XOUT	Vcc = 5 V	IOH = -200 μA	1.0	—	Vcc	V
VOL	Output "L" voltage	Other than XOUT	Drive capacity High Vcc = 5 V	IOL = 20 mA	—	—	2.0	V
			Drive capacity Low Vcc = 5 V	IOL = 5 mA	—	—	2.0	V
		XOUT	Vcc = 5 V	IOL = 200 μA	—	—	0.5	V
VT+-VT-	Hysteresis	INT0, INT1, INT3, KI0, KI1, KI2, KI3, TRAIO, TRBO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRCTRG, TRCCLK, ADTRG, RXD0, RXD2, CLK0, CLK2, SSI, SCL, SDA, SSO			0.1	1.2	—	V
		RESET			0.1	1.2	—	V
IiH	Input "H" current		VI = 5 V, Vcc = 5.0 V		—	—	5.0	μA
IiL	Input "L" current		VI = 0 V, Vcc = 5.0 V		—	—	-5.0	μA
RPULLUP	Pull-up resistance		VI = 0 V, Vcc = 5.0 V		25	50	100	kΩ
RfXIN	Feedback resistance	XIN			—	0.3	—	MΩ
RfXCIN	Feedback resistance	XCIN			—	8	—	MΩ
V _{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

Note:

1. 4.2 V ≤ Vcc ≤ 5.5 V and T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 20 MHz, unless otherwise specified.

Timing Requirements**(Unless Otherwise Specified: $V_{CC} = 5\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{opr} = 25^\circ\text{C}$)****Table 5.20 External Clock Input (XOUT, XCIN)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XOUT)}$	XOUT input cycle time	50	–	ns
$t_{WH(XOUT)}$	XOUT input “H” width	24	–	ns
$t_{WL(XOUT)}$	XOUT input “L” width	24	–	ns
$t_{c(XCIN)}$	XCIN input cycle time	14	–	μs
$t_{WH(XCIN)}$	XCIN input “H” width	7	–	μs
$t_{WL(XCIN)}$	XCIN input “L” width	7	–	μs

**Figure 5.8 External Clock Input Timing Diagram when $V_{CC} = 5\text{ V}$** **Table 5.21 TRAIO Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	100	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	40	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	40	–	ns

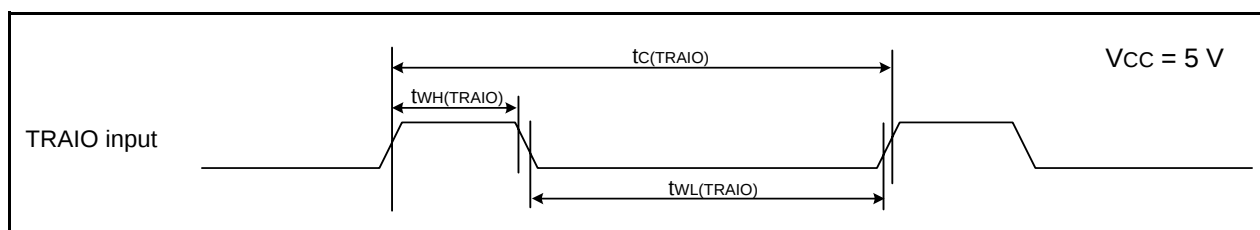
**Figure 5.9 TRAIO Input Timing Diagram when $V_{CC} = 5\text{ V}$**

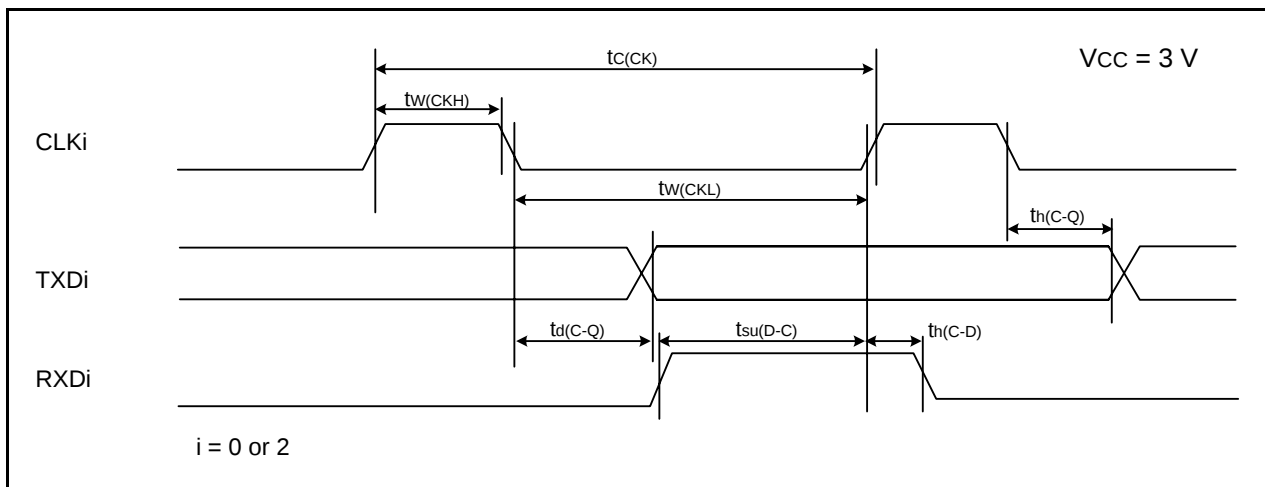
Table 5.25 Electrical Characteristics (4) [$2.7\text{ V} \leq V_{CC} < 3.3\text{ V}$]
($T_{opr} = -20\text{ to }85^{\circ}\text{C}$ (N version) / $-40\text{ to }85^{\circ}\text{C}$ (D version), unless otherwise specified.)

Symbol	Parameter		Condition	Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	3.5	10	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	1.5	7.5	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	7.0	15	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	3.0	–	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	4.0	–	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	1.5	–	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-16 MSTIIC = MSTTRD = MSTTRC = 1	–	1	–	mA
			Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	–	90	390
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division, FMR27 = 1, VCA20 = 0	–	80	400	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division, Program operation on RAM Flash memory off, FMSTP = 1, VCA20 = 0	–	40	–	μA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	–	15	90	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	–	4	80	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (peripheral clock off) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	–	3.5	–	μA
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	2.0	5.0	μA
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	5.0	–	μA

Table 5.28 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300	—	ns
$t_{w(CKH)}$	CLKi input "H" width	150	—	ns
$t_{w(CKL)}$	CLKi Input "L" width	150	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	70	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

i = 0 or 2

**Figure 5.14 Serial Interface Timing Diagram when Vcc = 3 V****Table 5.29 External Interrupt $\overline{INTi}$ (i = 0, 1, 3) Input, Key Input Interrupt $\overline{Kli}$ (i = 0 to 3)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input "H" width, $\overline{Kli}$ input "H" width	380 (1)	—	ns
$t_{w(INL)}$	$\overline{INTi}$ input "L" width, $\overline{Kli}$ input "L" width	380 (2)	—	ns

Notes:

1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

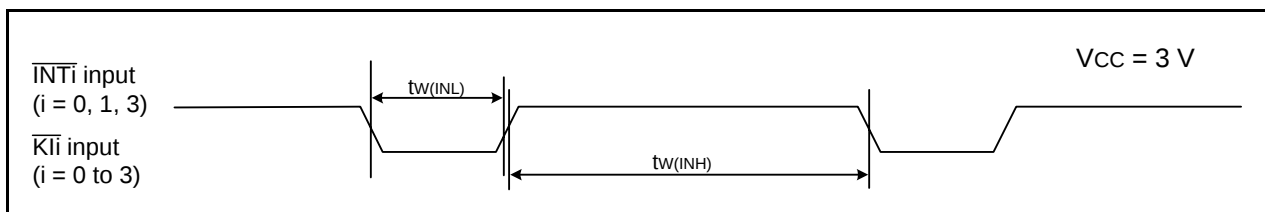
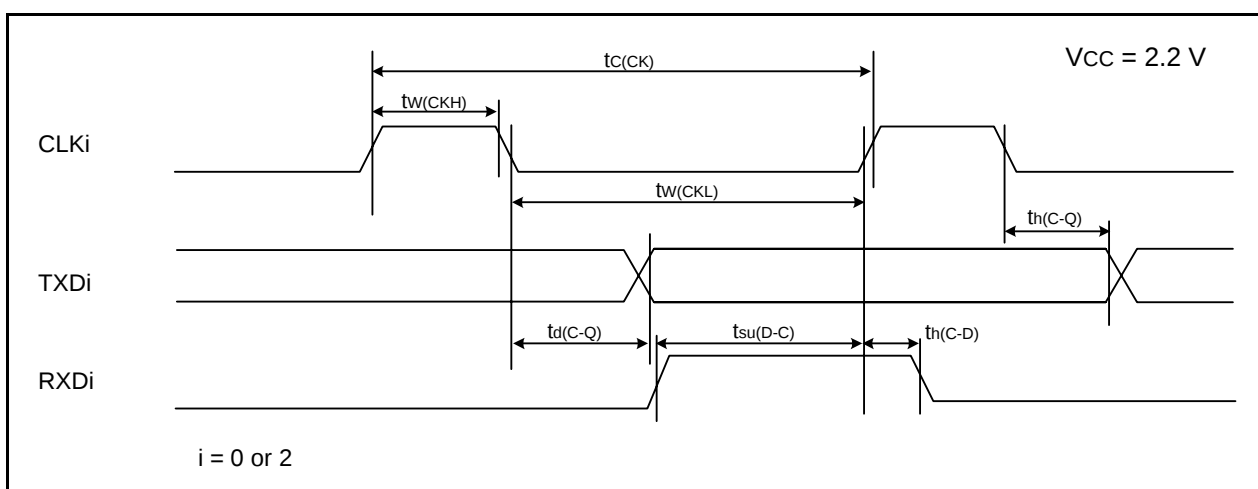
**Figure 5.15 Input Timing Diagram for External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{Kli}$ when Vcc = 3 V**

Table 5.34 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	800	—	ns
$t_{w(CKH)}$	CLKi input "H" width	400	—	ns
$t_{w(CKL)}$	CLKi input "L" width	400	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	200	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	150	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

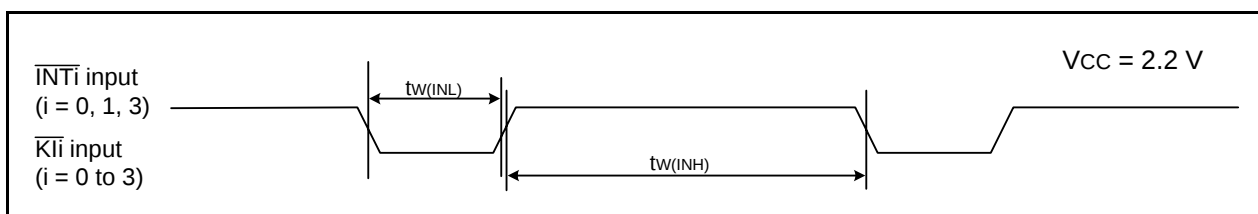
i = 0 or 2

**Figure 5.18 Serial Interface Timing Diagram when Vcc = 2.2 V****Table 5.35 External Interrupt $\overline{INTi}$ (i = 0, 1, 3) Input, Key Input Interrupt $\overline{Kli}$ (i = 0 to 3)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input "H" width, $\overline{Kli}$ input "H" width	1000 ⁽¹⁾	—	ns
$t_{w(INL)}$	$\overline{INTi}$ input "L" width, $\overline{Kli}$ input "L" width	1000 ⁽²⁾	—	ns

Notes:

- When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
- When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

**Figure 5.19 Input Timing Diagram for External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{Kli}$ when Vcc = 2.2 V**

