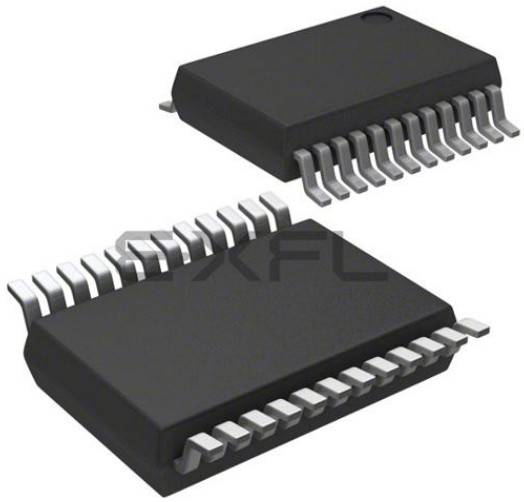
Renesas Electronics America Inc - R5F213G5CDSP#U0 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	19
Program Memory Size	24KB (24K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-LSSOP (0.220", 5.60mm Width)
Supplier Device Package	24-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f213g5cdsp-u0

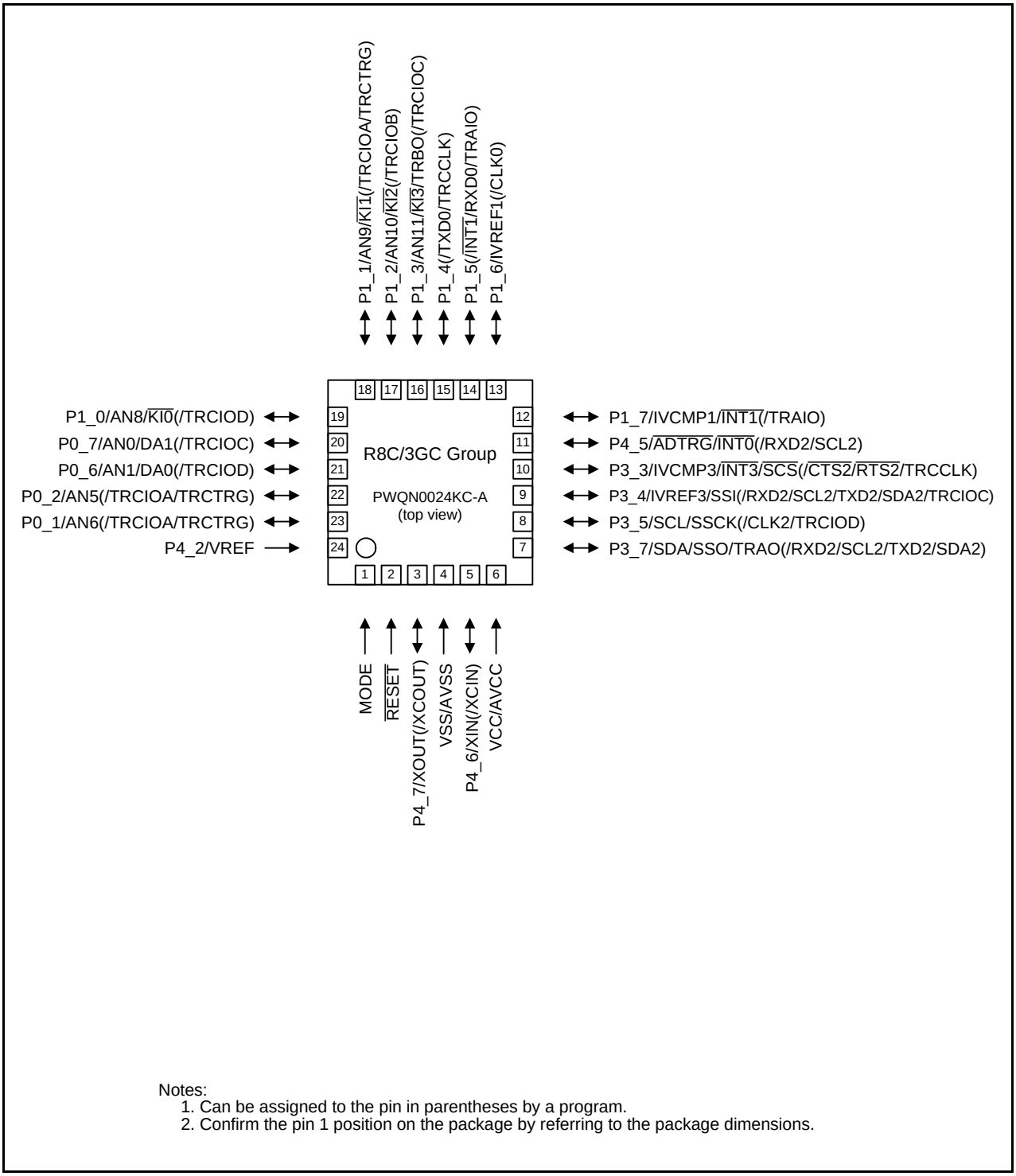
Table 1.2 Specifications for R8C/3GC Group (2)

Item	Function	Specification
Serial Interface	UART0	Clock synchronous serial I/O/UART
	UART2	Clock synchronous serial I/O/UART, I²C mode (I²C-bus), multiprocessor communication function
Synchronous Serial Communication Unit (SSU)		1 (shared with I²C-bus)
I²C bus		1 (shared with SSU)
LIN Module		Hardware LIN: 1 (timer RA, UART0)
A/D Converter		10-bit resolution × 8 channels, includes sample and hold function, with sweep mode
D/A Converter		8-bit resolution × 2 circuits
Comparator B		2 circuits
Flash Memory		• Programming and erasure voltage: VCC = 2.7 to 5.5 V • Programming and erasure endurance: 10,000 times (data flash) 1,000 times (program ROM) • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function • Background operation (BGO) function
Operating Frequency/Supply Voltage		f(XIN) = 20 MHz (VCC = 2.7 to 5.5 V) f(XIN) = 5 MHz (VCC = 1.8 to 5.5 V)
Current Consumption		Typ. 6.5 mA (VCC = 5.0 V, f(XIN) = 20 MHz) Typ. 3.5 mA (VCC = 3.0 V, f(XIN) = 10 MHz) Typ. 3.5 μA (VCC = 3.0 V, wait mode (f(XCIN) = 32 kHz)) Typ. 2.0 μA (VCC = 3.0 V, stop mode)
Operating Ambient Temperature		-20 to 85°C (N version) -40 to 85°C (D version) (1)
Package		24-pin HWQFN Package code: PWQN0024KC-A 24-pin LSSOP Package code: PLSP0024JB-A (previous code: 24P2F-A)

Note:
1. Specify the D version if D version functions are to be used.

1.4 Pin Assignment

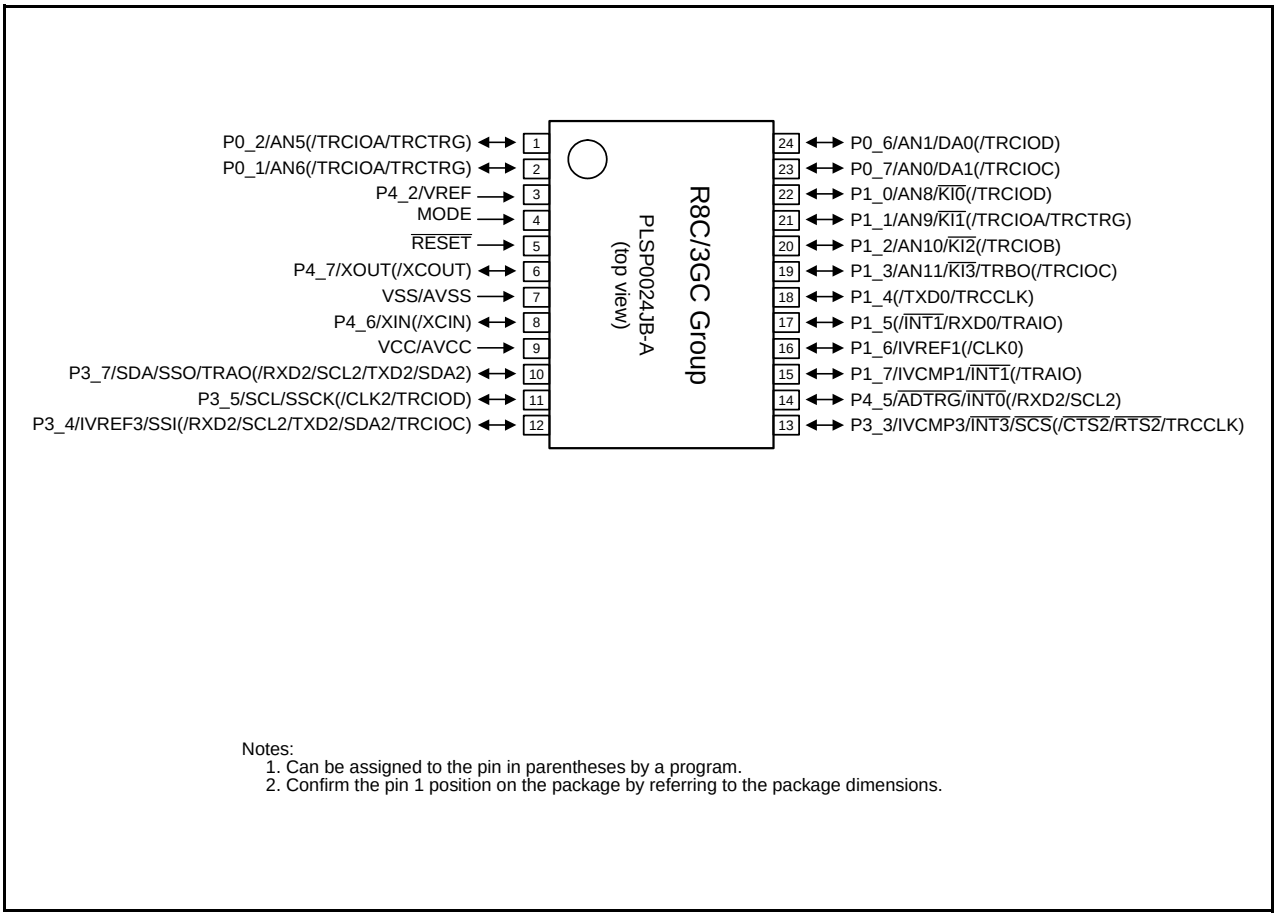
Figure 1.3 shows Pin Assignment (Top View) of PWQN0024KC-A Package. Table 1.4 outlines the Pin Name Information by Pin Number.



Notes:
1. Can be assigned to the pin in parentheses by a program.
2. Confirm the pin 1 position on the package by referring to the package dimensions.

Figure 1.3 Pin Assignment (Top View) of PWQN0024KC-A Package

Figure 1.4 shows Pin Assignment (Top View) of PLSP0024JB-A Package. Table 1.5 outlines the Pin Name Information by Pin Number.



Notes:
1. Can be assigned to the pin in parentheses by a program.
2. Confirm the pin 1 position on the package by referring to the package dimensions.

Figure 1.4 Pin Assignment (Top View) of PLSP0024JB-A Package

1.5 Pin Functions

Tables 1.6 and 1.7 list Pin Functions.

Table 1.6 Pin Functions (1)

Item	Pin Name	I/O Type	Description
Power supply input	VCC, VSS	–	Apply 1.8 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	–	Power supply for the A/D converter. Connect a capacitor between AVCC and AVSS.
Reset input	$\overline{\text{RESET}}$	I	Input “L” on this pin resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
XIN clock input	XIN	I	These pins are provided for XIN clock generation circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins (1). To use an external clock, input it to the XOUT pin and leave the XIN pin open.
XIN clock output	XOUT	I/O	
XCIN clock input	XCIN	I	These pins are provided for XCIN clock generation circuit I/O. Connect a crystal oscillator between the XCIN and XCOUT pins (1). To use an external clock, input it to the XCIN pin and leave the XCOUT pin open.
XCIN clock output	XCOUT	O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$, $\overline{\text{INT1}}$, $\overline{\text{INT3}}$	I	$\overline{\text{INT}}$ interrupt input pins. $\overline{\text{INT0}}$ is timer RB, and RC input pin.
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Key input interrupt input pins
Timer RA	TRAIO	I/O	Timer RA I/O pin
	TRAO	O	Timer RA output pin
Timer RB	TRBO	O	Timer RB output pin
Timer RC	TRCCLK	I	External clock input pin
	TRCTRG	I	External trigger input pin
	TRCIOA, TRCIOB, TRCIOC, TRCIOD	I/O	Timer RC I/O pins
Serial interface	CLK0, CLK2	I/O	Transfer clock I/O pins
	RXD0, RXD2	I	Serial data input pins
	TXD0, TXD2	O	Serial data output pins
	$\overline{\text{CTS2}}$	I	Transmission control input pin
	$\overline{\text{RTS2}}$	O	Reception control output pin
	SCL2	I/O	I^2C mode clock I/O pin
	SDA2	I/O	I^2C mode data I/O pin
I^2C bus	SCL	I/O	Clock I/O pin
	SDA	I/O	Data I/O pin
SSU	SSI	I/O	Data I/O pin
	$\overline{\text{SCS}}$	I/O	Chip-select signal I/O pin
	SSCK	I/O	Clock I/O pin
	SSO	I/O	Data I/O pin

I: Input O: Output I/O: Input and output

Note:

1. Refer to the oscillator manufacturer for oscillation characteristics.

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.
Interrupts are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.
The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has higher priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.12 list the special function registers. Table 4.13 lists the ID Code Areas and Option Function Select Area.

Table 4.1 SFR Information (1) [1]

Address	Register	Symbol	After Reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	00101000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h	Module Standby Control Register	MSTCR	00h
0009h	System Clock Control Register 3	CM3	00h
000Ah	Protect Register	PRCR	00h
000Bh	Reset Source Determination Register	RSTFR	0XXXXXXXb [2]
000Ch	Oscillation Stop Detection Register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDTC	00111111b
0010h			
0011h			
0012h			
0013h			
0014h			
0015h	High-Speed On-Chip Oscillator Control Register 7	FRA7	When shipping
0016h			
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h 10000000b [3]
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	00h
0024h	High-Speed On-Chip Oscillator Control Register 1	FRA1	When shipping
0025h	High-Speed On-Chip Oscillator Control Register 2	FRA2	00h
0026h	On-Chip Reference Voltage Control Register	OCVREFCR	00h
0027h			
0028h	Clock Prescaler Reset Flag	CPSRF	00h
0029h	High-Speed On-Chip Oscillator Control Register 4	FRA4	When Shipping
002Ah	High-Speed On-Chip Oscillator Control Register 5	FRA5	When Shipping
002Bh	High-Speed On-Chip Oscillator Control Register 6	FRA6	When Shipping
002Ch			
002Dh			
002Eh			
002Fh	High-Speed On-Chip Oscillator Control Register 3	FRA3	When shipping
0030h	Voltage Monitor Circuit Control Register	CMPA	00h
0031h	Voltage Monitor Circuit Edge Select Register	VCAC	00h
0032h			
0033h	Voltage Detect Register 1	VCA1	00001000b
0034h	Voltage Detect Register 2	VCA2	00h [4] 00100000b [5]
0035h			
0036h	Voltage Detection 1 Level Select Register	VD1LS	00000111b
0037h			
0038h	Voltage Monitor 0 Circuit Control Register	VW0C	1100X010b [4] 1100X011b [5]
0039h	Voltage Monitor 1 Circuit Control Register	VW1C	10001010b

X: Undefined

Notes:
1. The blank areas are reserved and cannot be accessed by users.
2. The CWR bit in the RSTFR register is set to 0 after power-on and voltage monitor 0 reset. Hardware reset, software reset, or watchdog timer reset does not affect this bit.
3. The CSPROINI bit in the OFS register is set to 0.
4. The LVDAS bit in the OFS register is set to 1.
5. The LVDAS bit in the OFS register is set to 0.

Table 4.2 SFR Information (2) (1)

Address	Register	Symbol	After Reset
003Ah	Voltage Monitor 2 Circuit Control Register	VW2C	10000010b
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			
0040h			
0041h	Flash Memory Ready Interrupt Control Register	FMRDYIC	XXXXX000b
0042h			
0043h			
0044h			
0045h			
0046h			
0047h	Timer RC Interrupt Control Register	TRCIC	XXXXX000b
0048h			
0049h			
004Ah	Timer RE Interrupt Control Register	TREIC	XXXXX000b
004Bh	UART2 Transmit Interrupt Control Register	S2TIC	XXXXX000b
004Ch	UART2 Receive Interrupt Control Register	S2RIC	XXXXX000b
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh	SSU Interrupt Control Register / IIC bus Interrupt Control Register (2)	SSUIC / IICIC	XXXXX000b
0050h			
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h			
0054h			
0055h			
0056h	Timer RA Interrupt Control Register	TRAIC	XXXXX000b
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh			
005Ch			
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh	UART2 Bus Collision Detection Interrupt Control Register	U2BCNIC	XXXXX000b
005Fh			
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh			
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h	Voltage Monitor 1 Interrupt Control Register	VCMP1IC	XXXXX000b
0073h	Voltage Monitor 2 Interrupt Control Register	VCMP2IC	XXXXX000b
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

X: Undefined

Notes:
1. The blank areas are reserved and cannot be accessed by users.
2. Selectable by the IICSEL bit in the SSUIICSR register.

Table 4.6 SFR Information (6) (1)

Address	Register	Symbol	After Reset
0140h			
0141h			
0142h			
0143h			
0144h			
0145h			
0146h			
0147h			
0148h			
0149h			
014Ah			
014Bh			
014Ch			
014Dh			
014Eh			
014Fh			
0150h			
0151h			
0152h			
0153h			
0154h			
0155h			
0156h			
0157h			
0158h			
0159h			
015Ah			
015Bh			
015Ch			
015Dh			
015Eh			
015Fh			
0160h			
0161h			
0162h			
0163h			
0164h			
0165h			
0166h			
0167h			
0168h			
0169h			
016Ah			
016Bh			
016Ch			
016Dh			
016Eh			
016Fh			
0170h			
0171h			
0172h			
0173h			
0174h			
0175h			
0176h			
0177h			
0178h			
0179h			
017Ah			
017Bh			
017Ch			
017Dh			
017Eh			
017Fh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.9 SFR Information (9) (1)

Address	Register	Symbol	After Reset
2C00h	DTC Transfer Vector Area		XXh
2C01h	DTC Transfer Vector Area		XXh
2C02h	DTC Transfer Vector Area		XXh
2C03h	DTC Transfer Vector Area		XXh
2C04h	DTC Transfer Vector Area		XXh
2C05h	DTC Transfer Vector Area		XXh
2C06h	DTC Transfer Vector Area		XXh
2C07h	DTC Transfer Vector Area		XXh
2C08h	DTC Transfer Vector Area		XXh
2C09h	DTC Transfer Vector Area		XXh
2C0Ah	DTC Transfer Vector Area		XXh
:	DTC Transfer Vector Area		XXh
:	DTC Transfer Vector Area		XXh
2C3Ah	DTC Transfer Vector Area		XXh
2C3Bh	DTC Transfer Vector Area		XXh
2C3Ch	DTC Transfer Vector Area		XXh
2C3Dh	DTC Transfer Vector Area		XXh
2C3Eh	DTC Transfer Vector Area		XXh
2C3Fh	DTC Transfer Vector Area		XXh
2C40h	DTC Control Data 0	DTCD0	XXh
2C41h			XXh
2C42h			XXh
2C43h			XXh
2C44h			XXh
2C45h			XXh
2C46h			XXh
2C47h			XXh
2C48h	DTC Control Data 1	DTCD1	XXh
2C49h			XXh
2C4Ah			XXh
2C4Bh			XXh
2C4Ch			XXh
2C4Dh			XXh
2C4Eh			XXh
2C4Fh			XXh
2C50h	DTC Control Data 2	DTCD2	XXh
2C51h			XXh
2C52h			XXh
2C53h			XXh
2C54h			XXh
2C55h			XXh
2C56h			XXh
2C57h			XXh
2C58h	DTC Control Data 3	DTCD3	XXh
2C59h			XXh
2C5Ah			XXh
2C5Bh			XXh
2C5Ch			XXh
2C5Dh			XXh
2C5Eh			XXh
2C5Fh			XXh
2C60h	DTC Control Data 4	DTCD4	XXh
2C61h			XXh
2C62h			XXh
2C63h			XXh
2C64h			XXh
2C65h			XXh
2C66h			XXh
2C67h			XXh
2C68h	DTC Control Data 5	DTCD5	XXh
2C69h			XXh
2C6Ah			XXh
2C6Bh			XXh
2C6Ch			XXh
2C6Dh			XXh
2C6Eh			XXh
2C6Fh			XXh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.12 SFR Information (12) (1)

Address	Register	Symbol	After Reset
2CF0h	DTC Control Data 22	DTCD22	XXh
2CF1h			XXh
2CF2h			XXh
2CF3h			XXh
2CF4h			XXh
2CF5h			XXh
2CF6h			XXh
2CF7h			XXh
2CF8h	DTC Control Data 23	DTCD23	XXh
2CF9h			XXh
2CFAh			XXh
2CFBh			XXh
2CFCh			XXh
2CFDh			XXh
2CFEh			XXh
2CFFh			XXh
2D00h			
:			
2FFFh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.13 ID Code Areas and Option Function Select Area

Address	Area Name	Symbol	After Reset
:			
FFDBh	Option Function Select Register 2	OFS2	(Note 1)
:			
FFDFh	ID1		(Note 2)
:			
FFE3h	ID2		(Note 2)
:			
FFEBh	ID3		(Note 2)
:			
FFEFh	ID4		(Note 2)
:			
FFF3h	ID5		(Note 2)
:			
FFF7h	ID6		(Note 2)
:			
FFFBh	ID7		(Note 2)
:			
FFFFh	Option Function Select Register	OFS	(Note 1)

Notes:

1. The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the option function select area. If the block including the option function select area is erased, the option function select area is set to FFh.
   When blank products are shipped, the option function select area is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the option function select area is the value programmed by the user.
2. The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the ID code areas. If the block including the ID code areas is erased, the ID code areas are set to FFh.
   When blank products are shipped, the ID code areas are set to FFh. They are set to the written value after written by the user.
   When factory-programming products are shipped, the value of the ID code areas is the value programmed by the user.

Table 5.2 Recommended Operating Conditions

Symbol	Parameter				Conditions	Standard			Unit
						Min.	Typ.	Max.	
V_{CC}/AV_{CC}	Supply voltage					1.8	–	5.5	V
V_{SS}/AV_{SS}	Supply voltage					–	0	–	V
V_{IH}	Input “H” voltage	Other than CMOS input				0.8 V_{CC}	–	V_{CC}	V
		CMOS input	Input level switching function (I/O port)	Input level selection: 0.35 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0.5 V_{CC}	–	V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0.55 V_{CC}	–	V_{CC}	V
					1.8 V ≤ V_{CC} < 2.7 V	0.65 V_{CC}	–	V_{CC}	V
				Input level selection: 0.5 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0.65 V_{CC}	–	V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0.7 V_{CC}	–	V_{CC}	V
					1.8 V ≤ V_{CC} < 2.7 V	0.8 V_{CC}	–	V_{CC}	V
				Input level selection: 0.7 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0.85 V_{CC}	–	V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0.85 V_{CC}	–	V_{CC}	V
					1.8 V ≤ V_{CC} < 2.7 V	0.85 V_{CC}	–	V_{CC}	V
		External clock input (XOUT)				1.2	–	V_{CC}	V
V_{IL}	Input “L” voltage	Other than CMOS input				0	–	0.2 V_{CC}	V
		CMOS input	Input level switching function (I/O port)	Input level selection: 0.35 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0	–	0.2 V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0	–	0.2 V_{CC}	V
					1.8 V ≤ V_{CC} < 2.7 V	0	–	0.2 V_{CC}	V
				Input level selection: 0.5 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0	–	0.4 V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0	–	0.3 V_{CC}	V
					1.8 V ≤ V_{CC} < 2.7 V	0	–	0.2 V_{CC}	V
				Input level selection: 0.7 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0	–	0.55 V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0	–	0.45 V_{CC}	V
					1.8 V ≤ V_{CC} < 2.7 V	0	–	0.35 V_{CC}	V
		External clock input (XOUT)				0	–	0.4	V
$I_{OH(sum)}$	Peak sum output “H” current	Sum of all pins $I_{OH(peak)}$				–	–	–160	mA
$I_{OH(sum)}$	Average sum output “H” current	Sum of all pins $I_{OH(avg)}$				–	–	–80	mA
$I_{OH(peak)}$	Peak output “H” current	Drive capacity Low				–	–	–10	mA
		Drive capacity High				–	–	–40	mA
$I_{OH(avg)}$	Average output “H” current	Drive capacity Low				–	–	–5	mA
		Drive capacity High				–	–	–20	mA
$I_{OL(sum)}$	Peak sum output “L” current	Sum of all pins $I_{OL(peak)}$				–	–	160	mA
$I_{OL(sum)}$	Average sum output “L” current	Sum of all pins $I_{OL(avg)}$				–	–	80	mA
$I_{OL(peak)}$	Peak output “L” current	Drive capacity Low				–	–	10	mA
		Drive capacity High				–	–	40	mA
$I_{OL(avg)}$	Average output “L” current	Drive capacity Low				–	–	5	mA
		Drive capacity High				–	–	20	mA
$f_{(XIN)}$	XIN clock input oscillation frequency				2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	20	MHz
					1.8 V ≤ V_{CC} < 2.7 V	–	–	5	MHz
$f_{(XCIN)}$	XCIN clock input oscillation frequency				1.8 V ≤ V_{CC} ≤ 5.5 V	–	32.768	50	kHz
fOCO40M	When used as the count source for timer RC (3)				2.7 V ≤ V_{CC} ≤ 5.5 V	32	–	40	MHz
fOCO-F	fOCO-F frequency				2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	20	MHz
					1.8 V ≤ V_{CC} < 2.7 V	–	–	5	MHz
–	System clock frequency				2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	20	MHz
					1.8 V ≤ V_{CC} < 2.7 V	–	–	5	MHz
$f_{(BCLK)}$	CPU clock frequency				2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	20	MHz
					1.8 V ≤ V_{CC} < 2.7 V	–	–	5	MHz

Notes:
1. V_{CC} = 1.8 to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.
3. fOCO40M can be used as the count source for timer RC in the range of V_{CC} = 2.7 V to 5.5V.

Table 5.3 A/D Converter Characteristics

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
–	Resolution		V_{ref} = AV_{CC}		–	–	10	Bit
–	Absolute accuracy	10-bit mode	V_{ref} = AV_{CC} = 5.0 V	AN0, AN1, AN5, AN6 input, AN8 to AN11 input	–	–	±3	LSB
			V_{ref} = AV_{CC} = 3.3 V	AN0, AN1, AN5, AN6 input, AN8 to AN11 input	–	–	±5	LSB
			V_{ref} = AV_{CC} = 3.0 V	AN0, AN1, AN5, AN6 input, AN8 to AN11 input	–	–	±5	LSB
			V_{ref} = AV_{CC} = 2.2 V	AN0, AN1, AN5, AN6 input, AN8 to AN11 input	–	–	±5	LSB
		8-bit mode	V_{ref} = AV_{CC} = 5.0 V	AN0, AN1, AN5, AN6 input, AN8 to AN11 input	–	–	±2	LSB
			V_{ref} = AV_{CC} = 3.3 V	AN0, AN1, AN5, AN6 input, AN8 to AN11 input	–	–	±2	LSB
			V_{ref} = AV_{CC} = 3.0 V	AN0, AN1, AN5, AN6 input, AN8 to AN11 input	–	–	±2	LSB
			V_{ref} = AV_{CC} = 2.2 V	AN0, AN1, AN5, AN6 input, AN8 to AN11 input	–	–	±2	LSB
ϕAD	A/D conversion clock		4.0 V ≤ V_{ref} = AV_{CC} ≤ 5.5 V (2)		2	–	20	MHz
			3.2 V ≤ V_{ref} = AV_{CC} ≤ 5.5 V (2)		2	–	16	MHz
			2.7 V ≤ V_{ref} = AV_{CC} ≤ 5.5 V (2)		2	–	10	MHz
			2.2 V ≤ V_{ref} = AV_{CC} ≤ 5.5 V (2)		2	–	5	MHz
–	Tolerance level impedance				–	3	–	kΩ
t_{CONV}	Conversion time	10-bit mode	V_{ref} = AV_{CC} = 5.0 V, ϕAD = 20 MHz		2.2	–	–	µs
		8-bit mode	V_{ref} = AV_{CC} = 5.0 V, ϕAD = 20 MHz		2.2	–	–	µs
t_{SAMP}	Sampling time		ϕAD = 20 MHz		0.8	–	–	µs
I_{Vref}	V_{ref} current		V_{CC} = 5 V, XIN = f1 = ϕAD = 20 MHz		–	45	–	µA
V_{ref}	Reference voltage				2.2	–	AV_{CC}	V
V_{IA}	Analog input voltage (3)				0	–	V_{ref}	V
OCVREF	On-chip reference voltage		2 MHz ≤ ϕAD ≤ 4 MHz		1.19	1.34	1.49	V

Notes:
1. V_{CC}/AV_{CC} = V_{ref} = 2.2 to 5.5 V, V_{SS} = 0 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. The A/D conversion result will be undefined in wait mode, stop mode, when the flash memory stops, and in low-current-consumption mode. Do not perform A/D conversion in these states or transition to these states during A/D conversion.
3. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 5.8 Voltage Detection 0 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det0}	Voltage detection level Vdet0_0 (2)		1.80	1.90	2.05	V
	Voltage detection level Vdet0_1 (2)		2.15	2.35	2.50	V
	Voltage detection level Vdet0_2 (2)		2.70	2.85	3.05	V
	Voltage detection level Vdet0_3 (2)		3.55	3.80	4.05	V
–	Voltage detection 0 circuit response time (4)	At the falling of V_{CC} from 5 V to (Vdet0_0 – 0.1) V	–	6	150	µs
–	Voltage detection circuit self power consumption	VCA25 = 1, V_{CC} = 5.0 V	–	1.5	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (3)		–	–	100	µs

Notes:
1. The measurement condition is V_{CC} = 1.8 V to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version).
2. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.
4. Time until the voltage monitor 0 reset is generated after the voltage passes V_{det0}.

Table 5.9 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det1}	Voltage detection level Vdet1_0 (2)	At the falling of Vcc	2.00	2.20	2.40	V
	Voltage detection level Vdet1_1 (2)	At the falling of Vcc	2.15	2.35	2.55	V
	Voltage detection level Vdet1_2 (2)	At the falling of Vcc	2.30	2.50	2.70	V
	Voltage detection level Vdet1_3 (2)	At the falling of Vcc	2.45	2.65	2.85	V
	Voltage detection level Vdet1_4 (2)	At the falling of Vcc	2.60	2.80	3.00	V
	Voltage detection level Vdet1_5 (2)	At the falling of Vcc	2.75	2.95	3.15	V
	Voltage detection level Vdet1_6 (2)	At the falling of Vcc	2.85	3.10	3.40	V
	Voltage detection level Vdet1_7 (2)	At the falling of Vcc	3.00	3.25	3.55	V
	Voltage detection level Vdet1_8 (2)	At the falling of Vcc	3.15	3.40	3.70	V
	Voltage detection level Vdet1_9 (2)	At the falling of Vcc	3.30	3.55	3.85	V
	Voltage detection level Vdet1_A (2)	At the falling of Vcc	3.45	3.70	4.00	V
	Voltage detection level Vdet1_B (2)	At the falling of Vcc	3.60	3.85	4.15	V
	Voltage detection level Vdet1_C (2)	At the falling of Vcc	3.75	4.00	4.30	V
	Voltage detection level Vdet1_D (2)	At the falling of Vcc	3.90	4.15	4.45	V
	Voltage detection level Vdet1_E (2)	At the falling of Vcc	4.05	4.30	4.60	V
	Voltage detection level Vdet1_F (2)	At the falling of Vcc	4.20	4.45	4.75	V
–	Hysteresis width at the rising of Vcc in voltage detection 1 circuit	Vdet1_0 to Vdet1_5 selected	–	0.07	–	V
		Vdet1_6 to Vdet1_F selected	–	0.10	–	V
–	Voltage detection 1 circuit response time (3)	At the falling of V_{CC} from 5 V to (Vdet1_0 – 0.1) V	–	60	150	µs
–	Voltage detection circuit self power consumption	VCA26 = 1, V_{CC} = 5.0 V	–	1.7	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (4)		–	–	100	µs

Notes:
1. The measurement condition is V_{CC} = 1.8 V to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version).
2. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
3. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V_{det1}.
4. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

Table 5.12 High-speed On-Chip Oscillator Circuit Electrical Characteristics (Package Type: PWQN0024KC-A)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
–	High-speed on-chip oscillator frequency after reset	V_{CC} = 1.8 V to 5.5 V –20°C ≤ T_{opr} ≤ 85°C	37.80	40	42.60	MHz
	High-speed on-chip oscillator frequency when the FRA4 register correction value is written into the FRA1 register and the FRA5 register correction value into the FRA3 register (2)	V_{CC} = 1.8 V to 5.5 V –20°C ≤ T_{opr} ≤ 85°C	34.836	36.864	39.261	MHz
	High-speed on-chip oscillator frequency when the FRA6 register correction value is written into the FRA1 register and the FRA7 register correction value into the FRA3 register	V_{CC} = 1.8 V to 5.5 V –20°C ≤ T_{opr} ≤ 85°C	30.24	32	34.08	MHz
–	Oscillation stability time	V_{CC} = 5.0 V, T_{opr} = 25°C	–	0.5	3	ms
–	Self power consumption at oscillation	V_{CC} = 5.0 V, T_{opr} = 25°C	–	400	–	µA

Notes:
1. V_{CC} = 1.8 to 5.5 V, T_{opr} = –20 to 85°C (N version), unless otherwise specified.
2. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

Table 5.13 High-speed On-Chip Oscillator Circuit Electrical Characteristics (Package Type: PLSP0024JB-A)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
–	High-speed on-chip oscillator frequency after reset	V_{CC} = 1.8 V to 5.5 V –20°C ≤ T_{opr} ≤ 85°C	38.4	40	41.6	MHz
		V_{CC} = 1.8 V to 5.5 V –40°C ≤ T_{opr} ≤ 85°C	38.0	40	42.0	MHz
	High-speed on-chip oscillator frequency when the FRA4 register correction value is written into the FRA1 register and the FRA5 register correction value into the FRA3 register (2)	V_{CC} = 1.8 V to 5.5 V –20°C ≤ T_{opr} ≤ 85°C	35.389	36.864	38.338	MHz
		V_{CC} = 1.8 V to 5.5 V –40°C ≤ T_{opr} ≤ 85°C	35.020	36.864	38.707	MHz
	High-speed on-chip oscillator frequency when the FRA6 register correction value is written into the FRA1 register and the FRA7 register correction value into the FRA3 register	V_{CC} = 1.8 V to 5.5 V –20°C ≤ T_{opr} ≤ 85°C	30.72	32	33.28	MHz
		V_{CC} = 1.8 V to 5.5 V –40°C ≤ T_{opr} ≤ 85°C	30.40	32	33.60	MHz
–	Oscillation stability time	V_{CC} = 5.0 V, T_{opr} = 25°C	–	0.5	3	ms
–	Self power consumption at oscillation	V_{CC} = 5.0 V, T_{opr} = 25°C	–	400	–	µA

Notes:
1. V_{CC} = 1.8 to 5.5 V, T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

Table 5.14 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		60	125	250	kHz
–	Oscillation stability time	V_{CC} = 5.0 V, T_{opr} = 25°C	–	30	100	µs
–	Self power consumption at oscillation	V_{CC} = 5.0 V, T_{opr} = 25°C	–	2	–	µA

Note:
1. V_{CC} = 1.8 to 5.5 V, T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.

Table 5.15 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during power-on (2)		–	–	2,000	µs

Notes:
1. The measurement condition is V_{CC} = 1.8 to 5.5 V and T_{opr} = 25°C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.

Table 5.16 Timing Requirements of Synchronous Serial Communication Unit (SSU) (1)

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
t_{SUCYC}	SSCK clock cycle time			4	–	–	t_{CYC} (2)
t_{HI}	SSCK clock “H” width			0.4	–	0.6	t_{SUCYC}
t_{LO}	SSCK clock “L” width			0.4	–	0.6	t_{SUCYC}
t_{RISE}	SSCK clock rising time	Master		–	–	1	t_{CYC} (2)
		Slave		–	–	1	µs
t_{FALL}	SSCK clock falling time	Master		–	–	1	t_{CYC} (2)
		Slave		–	–	1	µs
t_{SU}	SSO, SSI data input setup time			100	–	–	ns
t_H	SSO, SSI data input hold time			1	–	–	t_{CYC} (2)
t_{LEAD}	$\overline{SCS}$ setup time	Slave		$1t_{CYC}$ + 50	–	–	ns
t_{LAG}	$\overline{SCS}$ hold time	Slave		$1t_{CYC}$ + 50	–	–	ns
t_{OD}	SSO, SSI data output delay time			–	–	1	t_{CYC} (2)
t_{SA}	SSI slave access time		2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	$1.5t_{CYC}$ + 100	ns
			1.8 V ≤ V_{CC} < 2.7 V	–	–	$1.5t_{CYC}$ + 200	ns
t_{OR}	SSI slave out open time		2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	$1.5t_{CYC}$ + 100	ns
			1.8 V ≤ V_{CC} < 2.7 V	–	–	$1.5t_{CYC}$ + 200	ns

Notes:
1. V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. $1t_{CYC}$ = 1/f1(s)

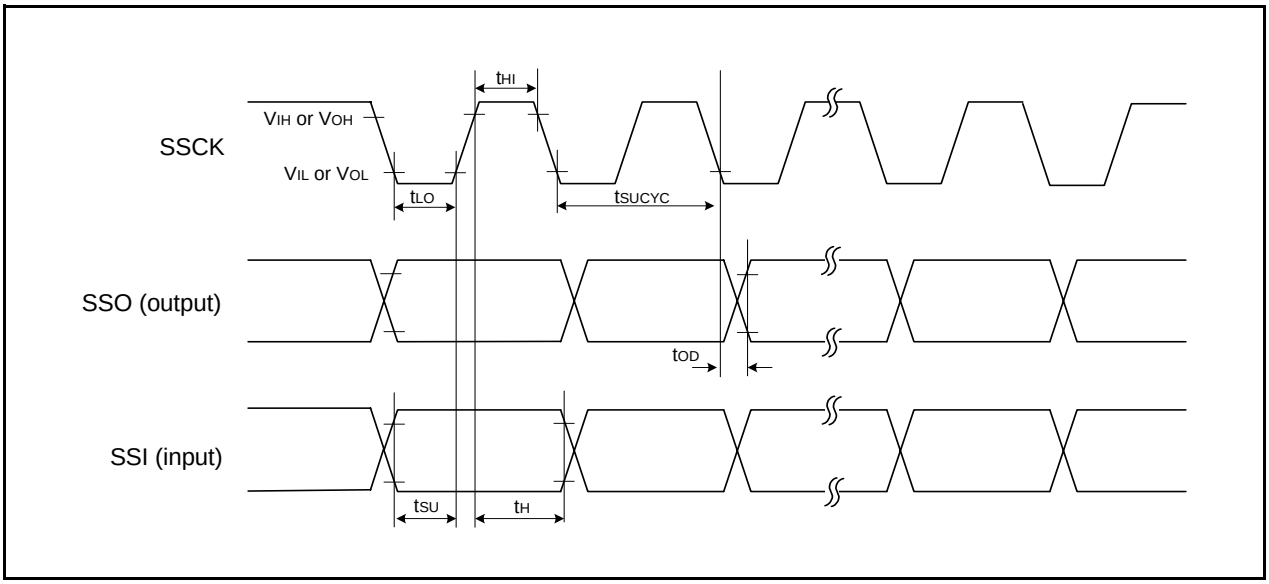


Figure 5.6 I/O Timing of Synchronous Serial Communication Unit (SSU) (Clock Synchronous Communication Mode)

Timing Requirements
(Unless Otherwise Specified: V_{CC} = 5 V, V_{SS} = 0 V at Topr = 25°C)

Table 5.20 External Clock Input (XOUT, XCIN)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XOUT)}$	XOUT input cycle time	50	–	ns
$t_{WH(XOUT)}$	XOUT input “H” width	24	–	ns
$t_{WL(XOUT)}$	XOUT input “L” width	24	–	ns
$t_{c(XCIN)}$	XCIN input cycle time	14	–	µs
$t_{WH(XCIN)}$	XCIN input “H” width	7	–	µs
$t_{WL(XCIN)}$	XCIN input “L” width	7	–	µs

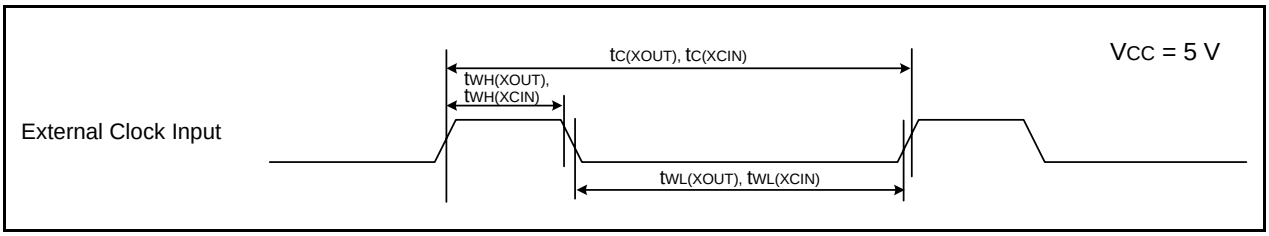


Figure 5.8 External Clock Input Timing Diagram when VCC = 5 V

Table 5.21 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	100	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	40	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	40	–	ns

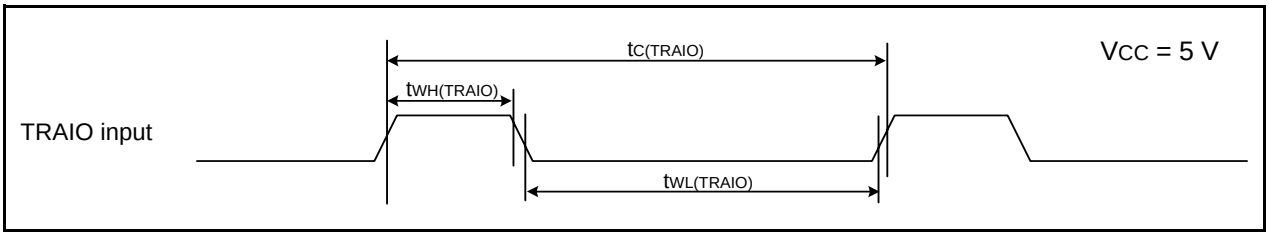


Figure 5.9 TRAIO Input Timing Diagram when V_{CC} = 5 V

Table 5.22 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200	–	ns
$t_{W(CKH)}$	CLKi input “H” width	100	–	ns
$t_{W(CKL)}$	CLKi input “L” width	100	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	50	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0 or 2

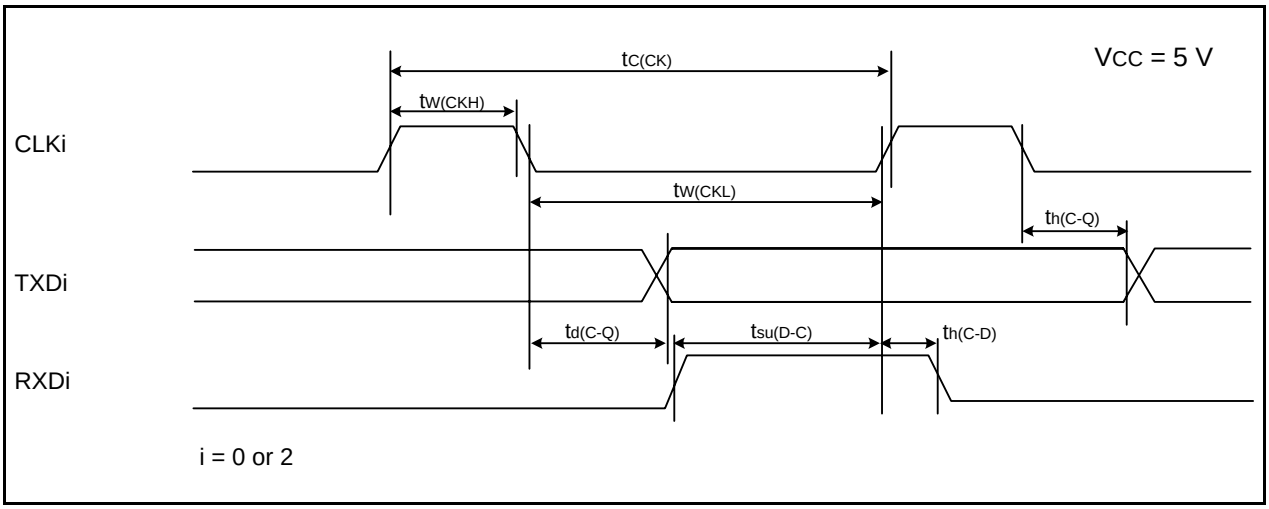


Figure 5.10 Serial Interface Timing Diagram when VCC = 5 V

Table 5.23 External Interrupt $\overline{INTi}$ (i = 0, 1, 3) Input, Key Input Interrupt $\overline{KIi}$ (i = 0 to 3)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width, $\overline{KIi}$ input “H” width	250 (1)	–	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width, $\overline{KIi}$ input “L” width	250 (2)	–	ns

Notes:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

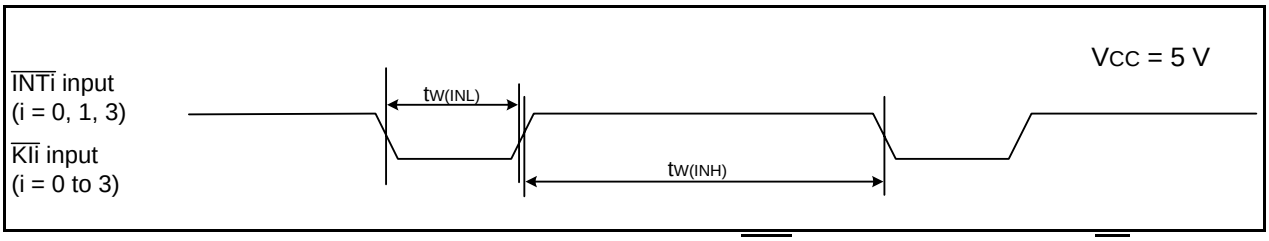


Figure 5.11 Input Timing Diagram for External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{KIi}$ when Vcc = 5 V

Timing Requirements
(Unless Otherwise Specified: Vcc = 2.2 V, Vss = 0 V at Topr = 25°C)

Table 5.32 External Clock Input (XOUT, XCIN)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XOUT)}$	XOUT input cycle time	200	–	ns
$t_{WH(XOUT)}$	XOUT input “H” width	90	–	ns
$t_{WL(XOUT)}$	XOUT input “L” width	90	–	ns
$t_{c(XCIN)}$	XCIN input cycle time	14	–	µs
$t_{WH(XCIN)}$	XCIN input “H” width	7	–	µs
$t_{WL(XCIN)}$	XCIN input “L” width	7	–	µs

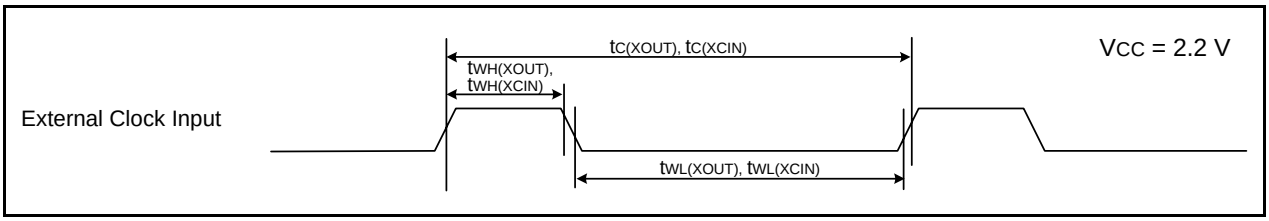


Figure 5.16 External Clock Input Timing Diagram when Vcc = 2.2 V

Table 5.33 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	500	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	200	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	200	–	ns

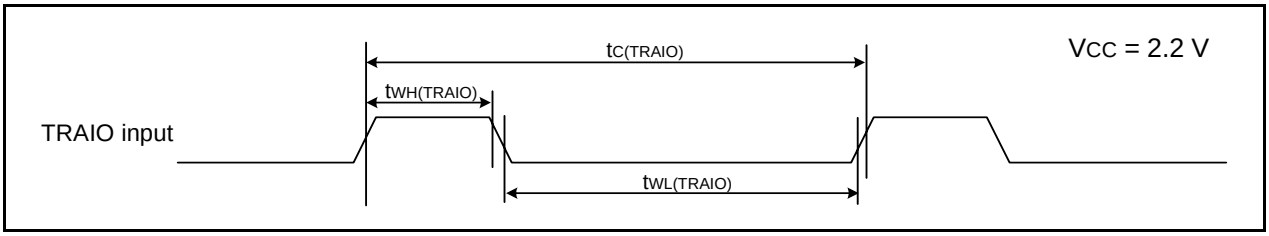
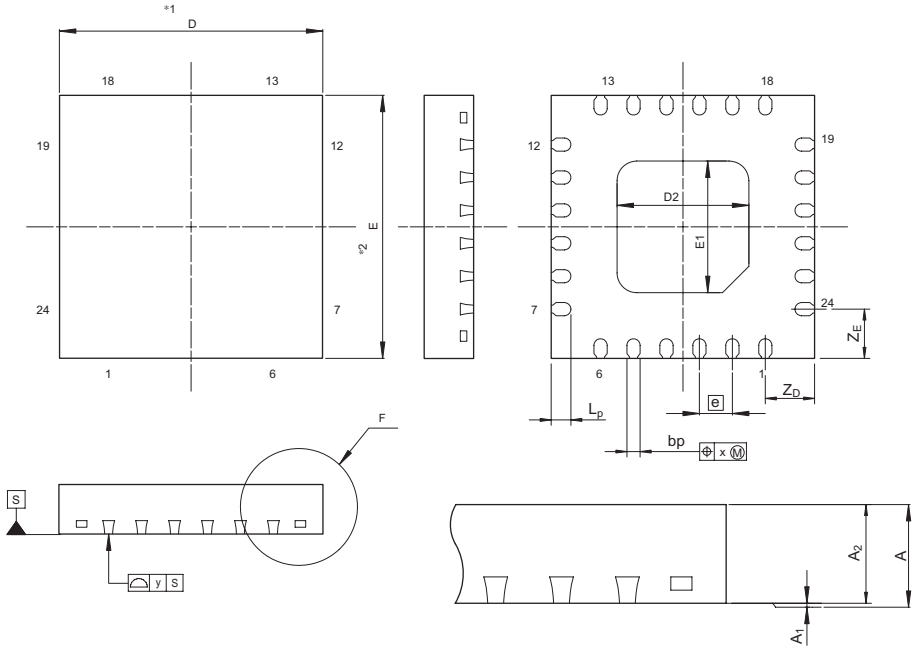


Figure 5.17 TRAIO Input Timing Diagram when Vcc = 2.2 V

Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Electronics website.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-HWQFN24-4x4-0.50	PWQN0024KC-A	24PJS-A	0.03g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	3.9	4.0	4.1
E	3.9	4.0	4.1
A_2	—	0.75	—
A	—	—	0.8
A_1	0	0	0.05
b_p	0.15	0.2	0.25
e	—	0.5	—
L_p	0.20	0.30	0.40
x	—	—	0.05
y	—	—	0.05
Z_D	—	0.75	—
Z_E	—	0.75	—
D_2	—	2.0	—
E_1	—	2.0	—