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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	19
Program Memory Size	24KB (24K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-LSSOP (0.220", 5.60mm Width)
Supplier Device Package	24-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f213g5cns-p-u0

1.1.2 Specifications

Tables 1.1 and 1.2 outline the Specifications for R8C/3GC Group.

Table 1.1 Specifications for R8C/3GC Group (1)

Item	Function	Specification
CPU	Central processing unit	R8C CPU core <ul style="list-style-type: none"> • Number of fundamental instructions: 89 • Minimum instruction execution time: <ul style="list-style-type: none"> 50 ns ($f(XIN) = 20$ MHz, $VCC = 2.7$ to 5.5 V) 200 ns ($f(XIN) = 5$ MHz, $VCC = 1.8$ to 5.5 V) • Multiplier: 16 bits \times 16 bits \rightarrow 32 bits • Multiply-accumulate instruction: 16 bits \times 16 bits + 32 bits \rightarrow 32 bits • Operation mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM, RAM, Data flash	Refer to Table 1.3 Product List for R8C/3GC Group .
Power Supply Voltage Detection	Voltage detection circuit	<ul style="list-style-type: none"> • Power-on reset • Voltage detection 3 (detection level of voltage detection 0 and voltage detection 1 selectable)
I/O Ports	Programmable I/O ports	<ul style="list-style-type: none"> • Input-only: 1 pin • CMOS I/O ports: 19, selectable pull-up resistor • High current drive ports: 19
Clock	Clock generation circuits	4 circuits: XIN clock oscillation circuit, XCIN clock oscillation circuit (32 kHz), High-speed on-chip oscillator (with frequency adjustment function), Low-speed on-chip oscillator <ul style="list-style-type: none"> • Oscillation stop detection: XIN clock oscillation stop detection function • Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16 • Low power consumption modes: <ul style="list-style-type: none"> Standard operating mode (high-speed clock, low-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode
Interrupts		Real-time clock (timer RE) <ul style="list-style-type: none"> • Number of interrupt vectors: 69 • External Interrupt: 7 (INT \times 3, Key input \times 4) • Priority levels: 7 levels
Watchdog Timer		<ul style="list-style-type: none"> • 14 bits \times 1 (with prescaler) • Reset start selectable • Low-speed on-chip oscillator for watchdog timer selectable
DTC (Data Transfer Controller)		<ul style="list-style-type: none"> • 1 channel • Activation sources: 23 • Transfer modes: 2 (normal mode, repeat mode)
Timer	Timer RA	8 bits \times 1 (with 8-bit prescaler) <ul style="list-style-type: none"> Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RB	8 bits \times 1 (with 8-bit prescaler) <ul style="list-style-type: none"> Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timer RC	16 bits \times 1 (with 4 capture/compare registers) <ul style="list-style-type: none"> Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin)
	Timer RE	8 bits \times 1 <ul style="list-style-type: none"> Real-time clock mode (count seconds, minutes, hours, days of week)

1.2 Product List

Table 1.3 lists Product List for R8C/3GC Group, and Figure 1.1 shows a Part Number, Memory Size, and Package of R8C/3GC Group.

Table 1.3 Product List for R8C/3GC Group

Current of Oct 2010

Part No.	ROM Capacity		RAM Capacity	Package Type	Remarks
	Program ROM	Data flash			
R5F213G2CNNP	8 Kbytes	1 Kbyte × 4	1 Kbyte	PWQN0024KC-A	N version
R5F213G4CNNP	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PWQN0024KC-A	
R5F213G5CNNP	24 Kbytes	1 Kbyte × 4	2 Kbytes	PWQN0024KC-A	
R5F213G6CNNP	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PWQN0024KC-A	
R5F213G1CNSP	4 Kbytes	1 Kbyte × 4	512 byte	PLSP0024JB-A	
R5F213G2CNSP	8 Kbytes	1 Kbyte × 4	1 Kbyte	PLSP0024JB-A	
R5F213G4CNSP	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PLSP0024JB-A	
R5F213G5CNSP	24 Kbytes	1 Kbyte × 4	2 Kbytes	PLSP0024JB-A	
R5F213G6CNSP	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PLSP0024JB-A	D version
R5F213G1CDSP	4 Kbytes	1 Kbyte × 4	512 byte	PLSP0024JB-A	
R5F213G2CDSP	8 Kbytes	1 Kbyte × 4	1 Kbyte	PLSP0024JB-A	
R5F213G4CDSP	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PLSP0024JB-A	
R5F213G5CDSP	24 Kbytes	1 Kbyte × 4	2 Kbytes	PLSP0024JB-A	
R5F213G6CDSP	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PLSP0024JB-A	

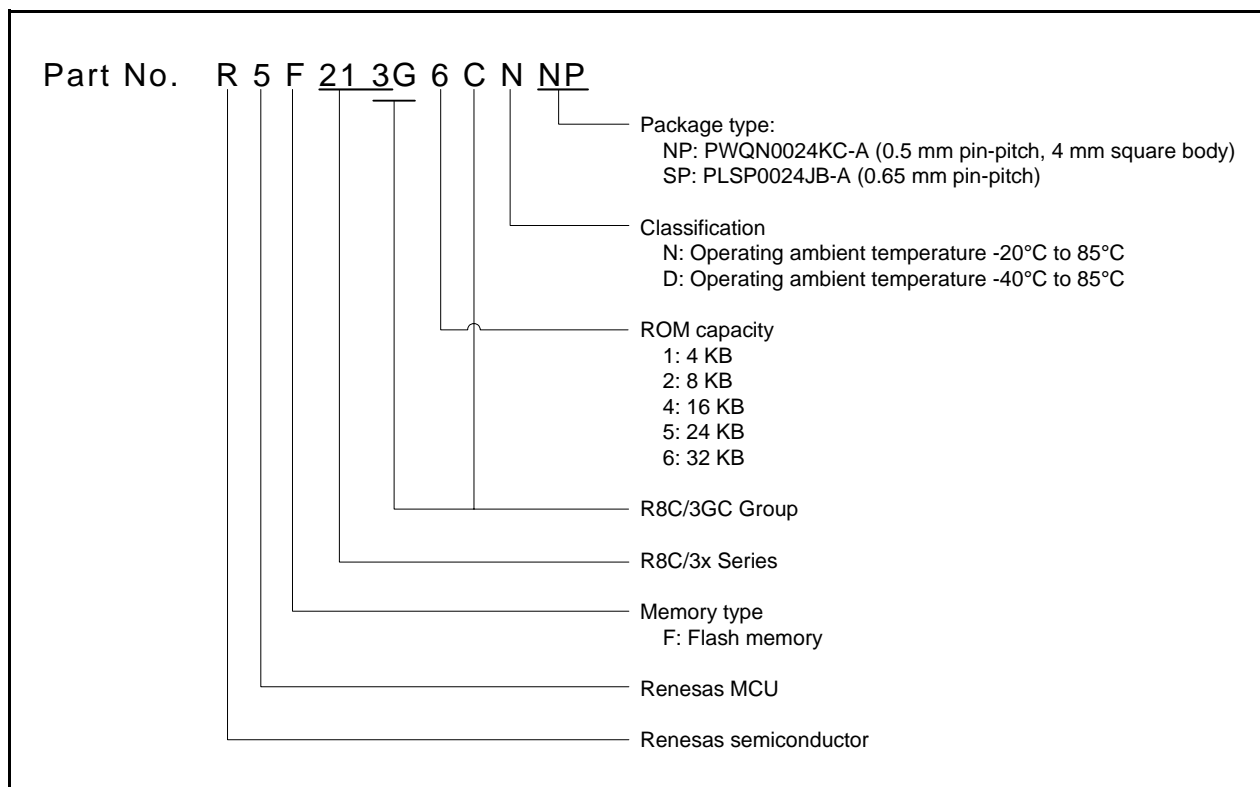


Figure 1.1 Part Number, Memory Size, and Package of R8C/3GC Group

Table 1.4 Pin Name Information by Pin Number

Pin Number	Control Pin	Port	I/O Pin Functions for Peripheral Modules					
			Interrupt	Timer	Serial Interface	SSU	I ² C bus	A/D Converter, D/A Converter, Comparator B
1	MODE							
2	RESET							
3	XOUT(/XCOUT)	P4_7						
4	VSS/AVSS							
5	XIN(/XCIN)	P4_6						
6	VCC/AVCC							
7		P3_7		TRAO	(RXD2/SCL2/ TXD2/SDA2)	SSO	SDA	
8		P3_5		(TRCIOD)	(CLK2)	SSCK	SCL	
9		P3_4		(TRCIOC)	(RXD2/SCL2/ TXD2/SDA2)	SSI		IVREF3
10		P3_3	INT3	(TRCCLK)	(CTS2/RTS2)	SCS		IVCMP3
11		P4_5	INT0		(RXD2/SCL2)			ADTRG
12		P1_7	INT1	(TRAIO)				IVCMP1
13		P1_6			(CLK0)			IVREF1
14		P1_5	(INT1)	(TRAIO)	(RXD0)			
15		P1_4		(TRCCLK)	(TXD0)			
16		P1_3	KI3	TRBO/ (TRCIOC)				AN11
17		P1_2	KI2	(TRCIOB)				AN10
18		P1_1	KI1	(TRCIOA/ TRCTRG)				AN9
19		P1_0	KI0	(TRCIOD)				AN8
20		P0_7		(TRCIOC)				AN0/DA1
21		P0_6		(TRCIOD)				AN1/DA0
22		P0_2		(TRCIOA/ TRCTRG)				AN5
23		P0_1		(TRCIOA/ TRCTRG)				AN6
24		P4_2						VREF

Note:

1. Can be assigned to the pin in parentheses by a program.

Table 1.7 Pin Functions (2)

Item	Pin Name	I/O Type	Description
Reference voltage input	VREF	I	Reference voltage input pin to A/D converter and D/A converter
A/D converter	AN0, AN1, AN5, AN6, AN8 to AN11	I	Analog input pins to A/D converter
	ADTRG	I	AD external trigger input pin
D/A converter	DA0, DA1	O	D/A converter output pins
Comparator B	IVCMP1, IVCMP3	I	Comparator B analog voltage input pins
	IVREF1, IVREF3	I	Comparator B reference voltage input pins
I/O port	P0_1, P0_2, P0_6, P0_7, P1_0 to P1_7, P3_3 to P3_5, P3_7, P4_5 to P4_7	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program. All ports can be used as LED drive ports.
Input port	P4_2	I	Input-only port

I: Input O: Output I/O: Input and output

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.

Interrupts are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.

The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has higher priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

Table 4.3 SFR Information (3) (1)

Address	Register	Symbol	After Reset
0080h	DTC Activation Control Register	DTCTL	00h
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h	DTC Activation Enable Register 0	DTCEN0	00h
0089h	DTC Activation Enable Register 1	DTCEN1	00h
008Ah	DTC Activation Enable Register 2	DTCEN2	00h
008Bh	DTC Activation Enable Register 3	DTCEN3	00h
008Ch			
008Dh	DTC Activation Enable Register 5	DTCEN5	00h
008Eh	DTC Activation Enable Register 6	DTCEN6	00h
008Fh			
0090h			
0091h			
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah			
009Bh			
009Ch			
009Dh			
009Eh			
009Fh			
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h	UART2 Transmit/Receive Mode Register	U2MR	00h
00A9h	UART2 Bit Rate Register	U2BRG	XXh
00AAh	UART2 Transmit Buffer Register	U2TB	XXh
00ABh			XXh
00ACh	UART2 Transmit/Receive Control Register 0	U2C0	00001000b
00ADh	UART2 Transmit/Receive Control Register 1	U2C1	00000010b
00AEh	UART2 Receive Buffer Register	U2RB	XXh
00AFh			XXh
00B0h	UART2 Digital Filter Function Select Register	URXDF	00h
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h			
00B9h			
00BAh			
00BBh	UART2 Special Mode Register 5	U2SMR5	00h
00BCh	UART2 Special Mode Register 4	U2SMR4	00h
00BDh	UART2 Special Mode Register 3	U2SMR3	000X0X0Xb
00BEh	UART2 Special Mode Register 2	U2SMR2	X0000000b
00BFh	UART2 Special Mode Register	U2SMR	X0000000b

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.6 SFR Information (6) (1)

Address	Register	Symbol	After Reset
0140h			
0141h			
0142h			
0143h			
0144h			
0145h			
0146h			
0147h			
0148h			
0149h			
014Ah			
014Bh			
014Ch			
014Dh			
014Eh			
014Fh			
0150h			
0151h			
0152h			
0153h			
0154h			
0155h			
0156h			
0157h			
0158h			
0159h			
015Ah			
015Bh			
015Ch			
015Dh			
015Eh			
015Fh			
0160h			
0161h			
0162h			
0163h			
0164h			
0165h			
0166h			
0167h			
0168h			
0169h			
016Ah			
016Bh			
016Ch			
016Dh			
016Eh			
016Fh			
0170h			
0171h			
0172h			
0173h			
0174h			
0175h			
0176h			
0177h			
0178h			
0179h			
017Ah			
017Bh			
017Ch			
017Dh			
017Eh			
017Fh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated Value	Unit
V _{CC} /AV _{CC}	Supply voltage		−0.3 to 6.5	V
V _I	Input voltage		−0.3 to V _{CC} + 0.3	V
V _O	Output voltage		−0.3 to V _{CC} + 0.3	V
P _d	Power dissipation	−40°C ≤ T _{opr} ≤ 85°C	500	mW
T _{opr}	Operating ambient temperature		−20 to 85 (N version) / −40 to 85 (D version)	°C
T _{stg}	Storage temperature		−65 to 150	°C

Table 5.3 A/D Converter Characteristics

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
–	Resolution		V _{ref} = AV _{CC}		–	–	10	Bit
–	Absolute accuracy	10-bit mode	V _{ref} = AV _{CC} = 5.0 V	AN0, AN1, AN5, AN6 input, AN8 to AN11 input	–	–	±3	LSB
			V _{ref} = AV _{CC} = 3.3 V	AN0, AN1, AN5, AN6 input, AN8 to AN11 input	–	–	±5	LSB
			V _{ref} = AV _{CC} = 3.0 V	AN0, AN1, AN5, AN6 input, AN8 to AN11 input	–	–	±5	LSB
			V _{ref} = AV _{CC} = 2.2 V	AN0, AN1, AN5, AN6 input, AN8 to AN11 input	–	–	±5	LSB
		8-bit mode	V _{ref} = AV _{CC} = 5.0 V	AN0, AN1, AN5, AN6 input, AN8 to AN11 input	–	–	±2	LSB
			V _{ref} = AV _{CC} = 3.3 V	AN0, AN1, AN5, AN6 input, AN8 to AN11 input	–	–	±2	LSB
			V _{ref} = AV _{CC} = 3.0 V	AN0, AN1, AN5, AN6 input, AN8 to AN11 input	–	–	±2	LSB
			V _{ref} = AV _{CC} = 2.2 V	AN0, AN1, AN5, AN6 input, AN8 to AN11 input	–	–	±2	LSB
φAD	A/D conversion clock		4.0 V ≤ V _{ref} = AV _{CC} ≤ 5.5 V ⁽²⁾		2	–	20	MHz
			3.2 V ≤ V _{ref} = AV _{CC} ≤ 5.5 V ⁽²⁾		2	–	16	MHz
			2.7 V ≤ V _{ref} = AV _{CC} ≤ 5.5 V ⁽²⁾		2	–	10	MHz
			2.2 V ≤ V _{ref} = AV _{CC} ≤ 5.5 V ⁽²⁾		2	–	5	MHz
–	Tolerance level impedance				–	3	–	kΩ
tCONV	Conversion time	10-bit mode	V _{ref} = AV _{CC} = 5.0 V, φAD = 20 MHz		2.2	–	–	μs
		8-bit mode	V _{ref} = AV _{CC} = 5.0 V, φAD = 20 MHz		2.2	–	–	μs
tsAMP	Sampling time		φAD = 20 MHz		0.8	–	–	μs
I _{Vref}	V _{ref} current		V _{CC} = 5 V, XIN = f1 = φAD = 20 MHz		–	45	–	μA
V _{ref}	Reference voltage				2.2	–	AV _{CC}	V
V _{IA}	Analog input voltage ⁽³⁾				0	–	V _{ref}	V
OCVREF	On-chip reference voltage		2 MHz ≤ φAD ≤ 4 MHz		1.19	1.34	1.49	V

Notes:

1. $V_{CC}/AV_{CC} = V_{ref} = 2.2$ to 5.5 V , $V_{SS} = 0\text{ V}$ and $T_{opr} = -20$ to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. The A/D conversion result will be undefined in wait mode, stop mode, when the flash memory stops, and in low-current-consumption mode. Do not perform A/D conversion in these states or transition to these states during A/D conversion.
3. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 5.8 Voltage Detection 0 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V _{det0}	Voltage detection level V _{det0_0} (2)		1.80	1.90	2.05	V
	Voltage detection level V _{det0_1} (2)		2.15	2.35	2.50	V
	Voltage detection level V _{det0_2} (2)		2.70	2.85	3.05	V
	Voltage detection level V _{det0_3} (2)		3.55	3.80	4.05	V
—	Voltage detection 0 circuit response time (4)	At the falling of V _{CC} from 5 V to (V _{det0_0} – 0.1) V	—	6	150	μs
—	Voltage detection circuit self power consumption	VCA25 = 1, V _{CC} = 5.0 V	—	1.5	—	μA
t _{d(E-A)}	Waiting time until voltage detection circuit operation starts (3)		—	—	100	μs

Notes:

1. The measurement condition is V_{CC} = 1.8 V to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version).
2. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.
4. Time until the voltage monitor 0 reset is generated after the voltage passes V_{det0}.

Table 5.9 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V _{det1}	Voltage detection level V _{det1_0} (2)	At the falling of V _{CC}	2.00	2.20	2.40	V
	Voltage detection level V _{det1_1} (2)	At the falling of V _{CC}	2.15	2.35	2.55	V
	Voltage detection level V _{det1_2} (2)	At the falling of V _{CC}	2.30	2.50	2.70	V
	Voltage detection level V _{det1_3} (2)	At the falling of V _{CC}	2.45	2.65	2.85	V
	Voltage detection level V _{det1_4} (2)	At the falling of V _{CC}	2.60	2.80	3.00	V
	Voltage detection level V _{det1_5} (2)	At the falling of V _{CC}	2.75	2.95	3.15	V
	Voltage detection level V _{det1_6} (2)	At the falling of V _{CC}	2.85	3.10	3.40	V
	Voltage detection level V _{det1_7} (2)	At the falling of V _{CC}	3.00	3.25	3.55	V
	Voltage detection level V _{det1_8} (2)	At the falling of V _{CC}	3.15	3.40	3.70	V
	Voltage detection level V _{det1_9} (2)	At the falling of V _{CC}	3.30	3.55	3.85	V
	Voltage detection level V _{det1_A} (2)	At the falling of V _{CC}	3.45	3.70	4.00	V
	Voltage detection level V _{det1_B} (2)	At the falling of V _{CC}	3.60	3.85	4.15	V
	Voltage detection level V _{det1_C} (2)	At the falling of V _{CC}	3.75	4.00	4.30	V
	Voltage detection level V _{det1_D} (2)	At the falling of V _{CC}	3.90	4.15	4.45	V
	Voltage detection level V _{det1_E} (2)	At the falling of V _{CC}	4.05	4.30	4.60	V
	Voltage detection level V _{det1_F} (2)	At the falling of V _{CC}	4.20	4.45	4.75	V
—	Hysteresis width at the rising of V _{CC} in voltage detection 1 circuit	V _{det1_0} to V _{det1_5} selected	—	0.07	—	V
		V _{det1_6} to V _{det1_F} selected	—	0.10	—	V
—	Voltage detection 1 circuit response time (3)	At the falling of V _{CC} from 5 V to (V _{det1_0} – 0.1) V	—	60	150	μs
—	Voltage detection circuit self power consumption	VCA26 = 1, V _{CC} = 5.0 V	—	1.7	—	μA
t _{d(E-A)}	Waiting time until voltage detection circuit operation starts (4)		—	—	100	μs

Notes:

1. The measurement condition is V_{CC} = 1.8 V to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version).
2. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
3. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V_{det1}.
4. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

Table 5.15 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t _{d(P-R)}	Time for internal power supply stabilization during power-on ⁽²⁾		—	—	2,000	μs

Notes:

1. The measurement condition is V_{CC} = 1.8 to 5.5 V and T_{opr} = 25°C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.

Table 5.16 Timing Requirements of Synchronous Serial Communication Unit (SSU) ⁽¹⁾

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
t _{SUCYC}	SSCK clock cycle time			4	—	—	t _{CYC} ⁽²⁾
t _{HI}	SSCK clock "H" width			0.4	—	0.6	t _{SUCYC}
t _{LO}	SSCK clock "L" width			0.4	—	0.6	t _{SUCYC}
t _{RISE}	SSCK clock rising time	Master		—	—	1	t _{CYC} ⁽²⁾
		Slave		—	—	1	μs
t _{FALL}	SSCK clock falling time	Master		—	—	1	t _{CYC} ⁽²⁾
		Slave		—	—	1	μs
t _{SU}	SSO, SSI data input setup time			100	—	—	ns
t _H	SSO, SSI data input hold time			1	—	—	t _{CYC} ⁽²⁾
t _{LEAD}	$\overline{\text{SCS}}$ setup time	Slave		1t _{CYC} + 50	—	—	ns
t _{LAG}	$\overline{\text{SCS}}$ hold time	Slave		1t _{CYC} + 50	—	—	ns
t _{OD}	SSO, SSI data output delay time			—	—	1	t _{CYC} ⁽²⁾
t _{SA}	SSI slave access time		2.7 V ≤ V _{CC} ≤ 5.5 V	—	—	1.5t _{CYC} + 100	ns
			1.8 V ≤ V _{CC} < 2.7 V	—	—	1.5t _{CYC} + 200	ns
t _{OR}	SSI slave out open time		2.7 V ≤ V _{CC} ≤ 5.5 V	—	—	1.5t _{CYC} + 100	ns
			1.8 V ≤ V _{CC} < 2.7 V	—	—	1.5t _{CYC} + 200	ns

Notes:

1. V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V and T_{opr} = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.
2. 1t_{CYC} = 1/f₁(s)

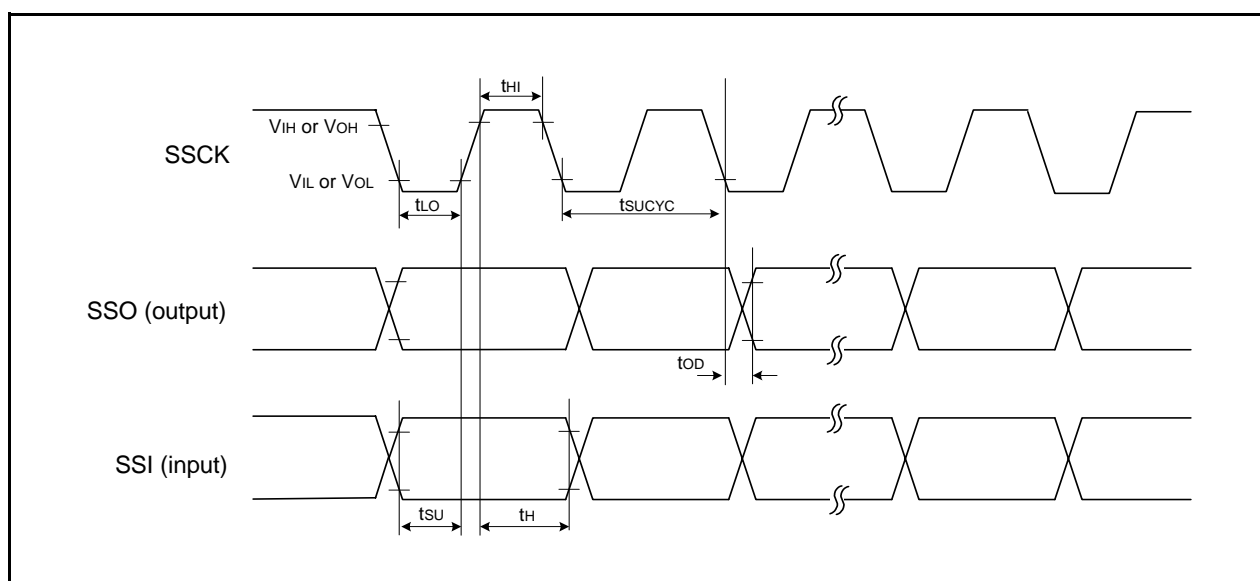
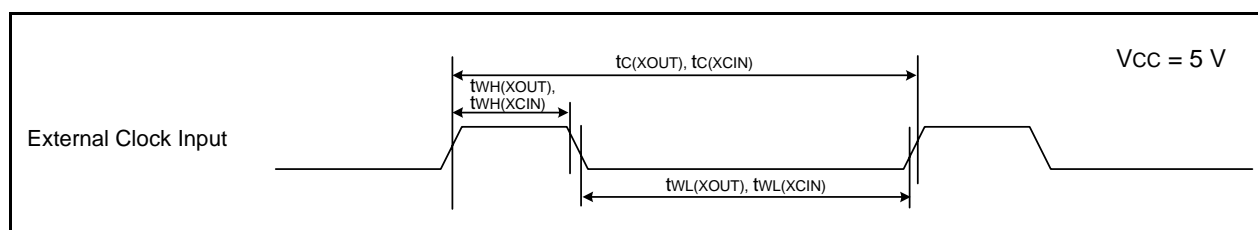


Figure 5.6 I/O Timing of Synchronous Serial Communication Unit (SSU) (Clock Synchronous Communication Mode)

Timing Requirements**(Unless Otherwise Specified: $V_{CC} = 5\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{opr} = 25^\circ\text{C}$)****Table 5.20 External Clock Input (XOUT, XCIN)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XOUT)}$	XOUT input cycle time	50	–	ns
$t_{WH(XOUT)}$	XOUT input “H” width	24	–	ns
$t_{WL(XOUT)}$	XOUT input “L” width	24	–	ns
$t_{c(XCIN)}$	XCIN input cycle time	14	–	μs
$t_{WH(XCIN)}$	XCIN input “H” width	7	–	μs
$t_{WL(XCIN)}$	XCIN input “L” width	7	–	μs

**Figure 5.8 External Clock Input Timing Diagram when $V_{CC} = 5\text{ V}$** **Table 5.21 TRAIO Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	100	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	40	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	40	–	ns

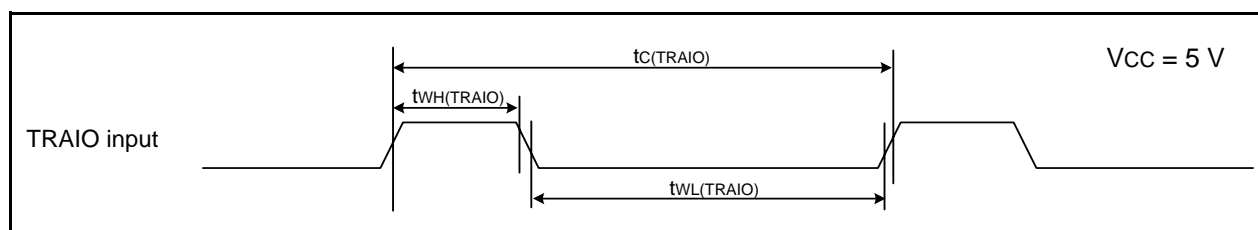
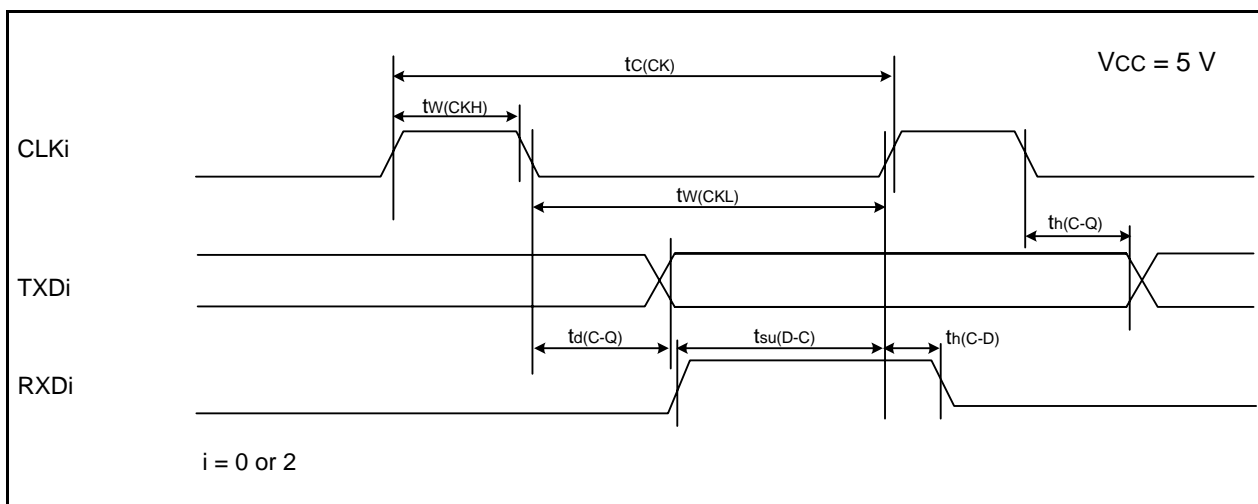
**Figure 5.9 TRAIO Input Timing Diagram when $V_{CC} = 5\text{ V}$**

Table 5.22 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200	—	ns
$t_{w(CKH)}$	CLKi input "H" width	100	—	ns
$t_{w(CKL)}$	CLKi input "L" width	100	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	50	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

i = 0 or 2

**Figure 5.10 Serial Interface Timing Diagram when Vcc = 5 V****Table 5.23 External Interrupt \overline{INTi} (i = 0, 1, 3) Input, Key Input Interrupt \overline{Kli} (i = 0 to 3)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	\overline{INTi} input "H" width, \overline{Kli} input "H" width	250 ⁽¹⁾	—	ns
$t_{w(INL)}$	\overline{INTi} input "L" width, \overline{Kli} input "L" width	250 ⁽²⁾	—	ns

Notes:

1. When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

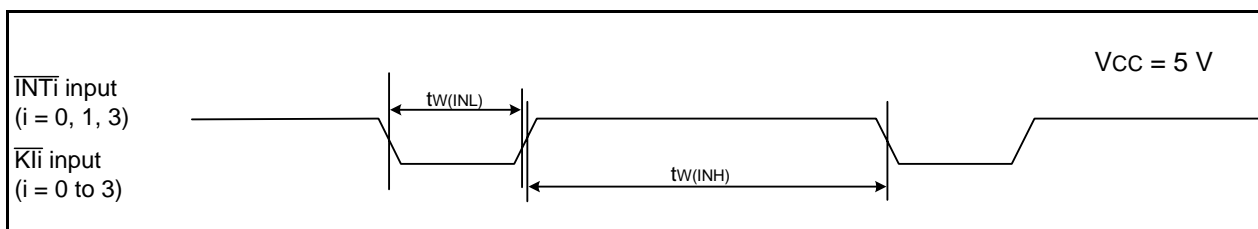
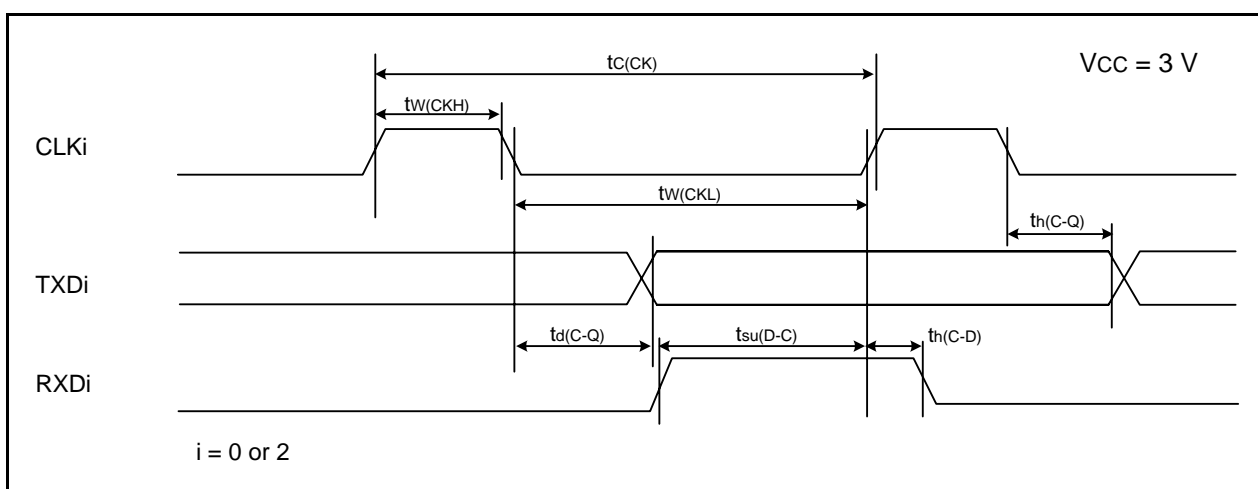
**Figure 5.11 Input Timing Diagram for External Interrupt \overline{INTi} and Key Input Interrupt \overline{Kli} when Vcc = 5 V**

Table 5.28 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300	—	ns
$t_{w(CKH)}$	CLKi input "H" width	150	—	ns
$t_{w(CKL)}$	CLKi Input "L" width	150	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	70	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

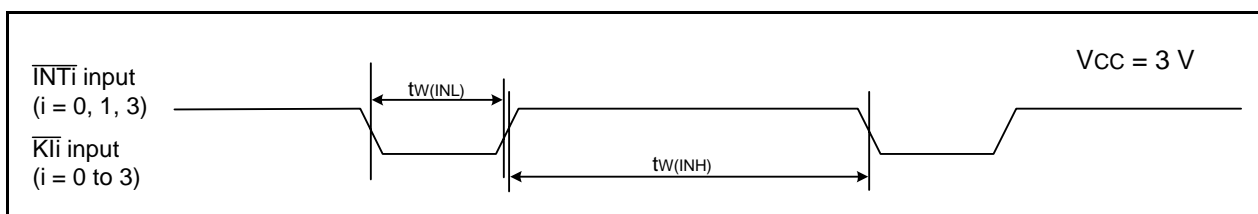
i = 0 or 2

**Figure 5.14 Serial Interface Timing Diagram when Vcc = 3 V****Table 5.29 External Interrupt \overline{INTi} (i = 0, 1, 3) Input, Key Input Interrupt \overline{Kli} (i = 0 to 3)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	\overline{INTi} input "H" width, \overline{Kli} input "H" width	380 (1)	—	ns
$t_{w(INL)}$	\overline{INTi} input "L" width, \overline{Kli} input "L" width	380 (2)	—	ns

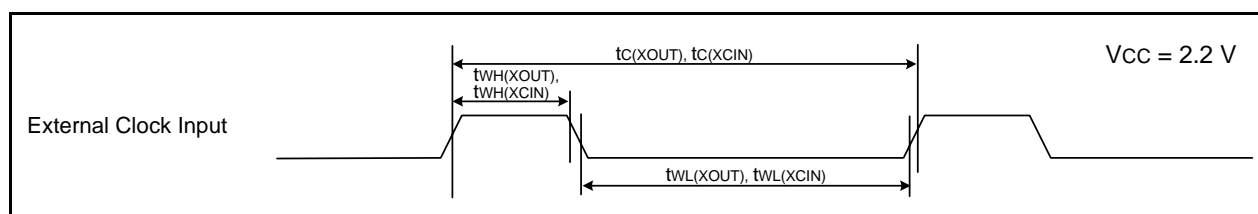
Notes:

- When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
- When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

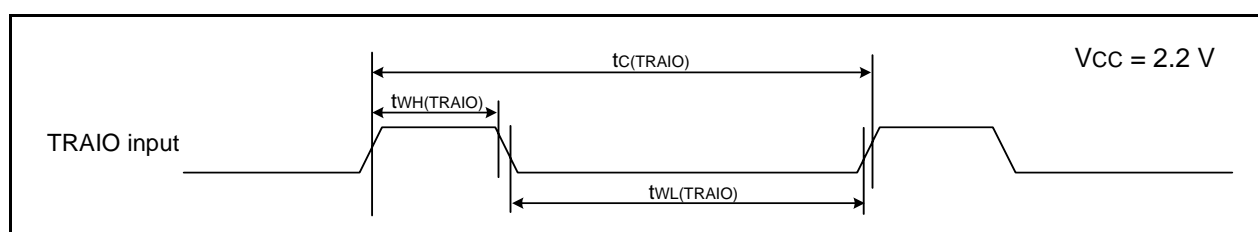
**Figure 5.15 Input Timing Diagram for External Interrupt \overline{INTi} and Key Input Interrupt \overline{Kli} when Vcc = 3 V**

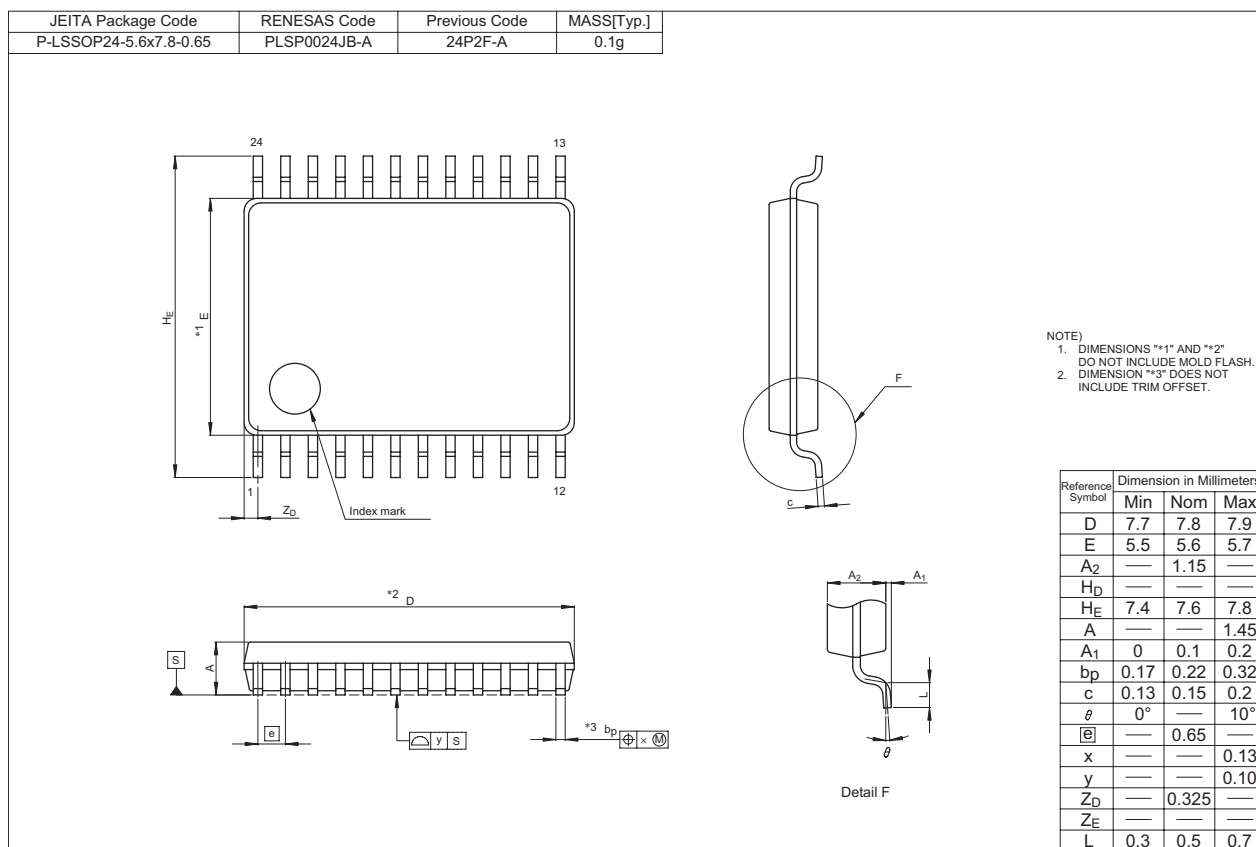
Timing Requirements**(Unless Otherwise Specified: $V_{CC} = 2.2\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{opr} = 25^{\circ}\text{C}$)****Table 5.32 External Clock Input (XOUT, XCIN)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XOUT)}$	XOUT input cycle time	200	–	ns
$t_{WH(XOUT)}$	XOUT input “H” width	90	–	ns
$t_{WL(XOUT)}$	XOUT input “L” width	90	–	ns
$t_{c(XCIN)}$	XCIN input cycle time	14	–	μs
$t_{WH(XCIN)}$	XCIN input “H” width	7	–	μs
$t_{WL(XCIN)}$	XCIN input “L” width	7	–	μs

**Figure 5.16 External Clock Input Timing Diagram when $V_{CC} = 2.2\text{ V}$** **Table 5.33 TRAIO Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	500	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	200	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	200	–	ns

**Figure 5.17 TRAIO Input Timing Diagram when $V_{CC} = 2.2\text{ V}$**



REVISION HISTORY	R8C/3GC Group Datasheet
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Rev.	Date	Description	
		Page	Summary
0.01	Oct. 30, 2009	—	First Edition issued
0.10	May 24, 2010	10	Table 1.6 XOUT: I → I/O
		28 to 54	"5. Electrical Characteristics" added
		55, 56	"Package Dimensions" revised
1.00	Oct 19, 2010	All	"Under development" deleted
		4	Table 1.3 QFN: D version deleted
		15	Figure 3.1 QFN: D version deleted
		31	Table 32.3 "tCONV", "tSAMP" revised
		37	Table 32.12 added, Table 32.13 revised

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

- The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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