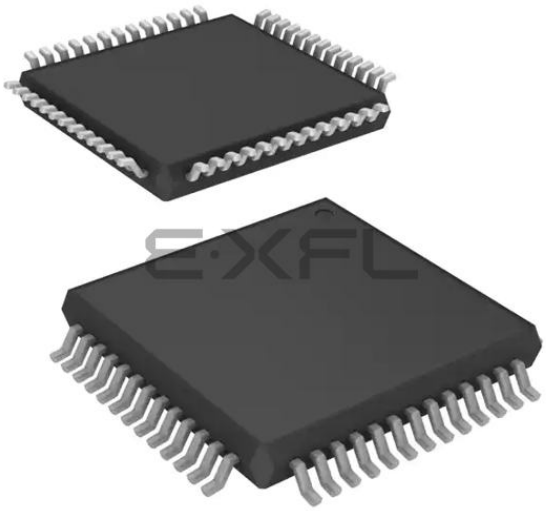
# Renesas Electronics America Inc - UPD78F0423GB-GAG-AX Datasheet



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## Applications of "Embedded - Microcontrollers"

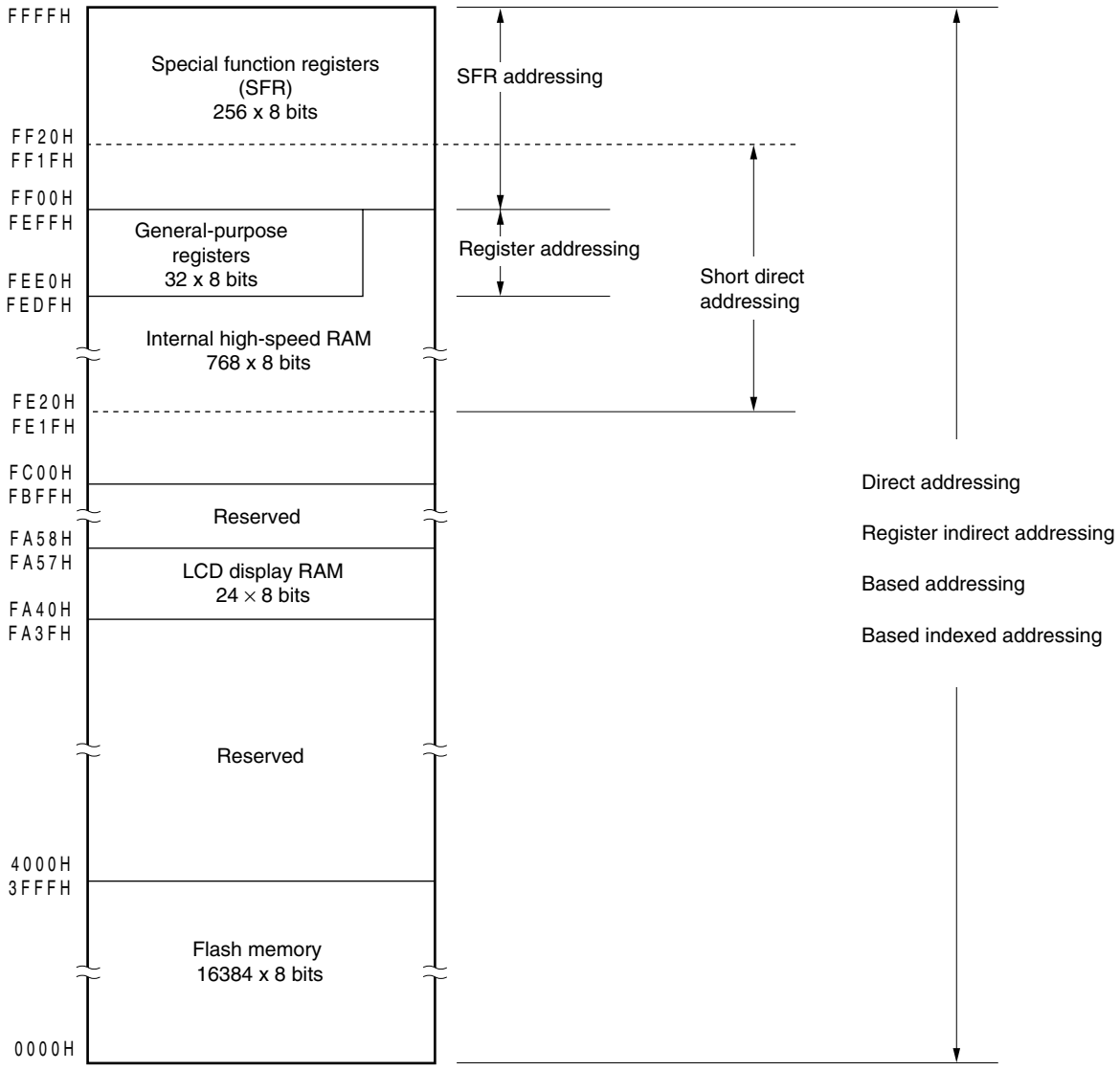
| Details | |
|---|---|
| Product Status | Active |
| Core Processor | 78K/0 |
| Core Size | 8-Bit |
| Speed | 10MHz |
| Connectivity | 3-Wire SIO, LINbus, UART/USART |
| Peripherals | LCD, LVD, POR, PWM, WDT |
| Number of I/O | 34 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 1K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 52-LQFP |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0423gb-gag-ax |

**(2) Non-port pins** **(1/3)**

| Function Name | I/O | Function | After Reset | Alternate Function |
|---|---|---|---|---|
| ANI0[Note] | Input | 10-bit successive approximation type A/D converter analog input. | Digital input port | P20/SEG23 |
| ANI1[Note] | | | | P21/SEG22 |
| ANI2[Note] | | | | P22/SEG21 |
| ANI3[Note] | | | | P23/SEG20 |
| ANI4[Note] | | | | P24/SEG19 |
| ANI5[Note] | | | | P25/SEG18 |
| $AV_{REF}$[Note] | Input | 10-bit successive approximation type A/D converter reference voltage input and positive power supply for port 2 | – | – |
| $AV_{SS}$[Note] | – | A/D converter ground potential. Make the same potential as $V_{SS}$. | – | – |
| SEG0 to SEG3 | Output | LCD controller/driver segment signal outputs | Output | COM4 to COM7 |
| SEG4 | | | Input port | P80 |
| SEG5, SEG6 | | | | P100, P101 |
| SEG7 | | | | P111 |
| SEG8 | | | | P112/TxD6 |
| SEG9 | | | | P113/RxD6 |
| SEG10 to SEG13 | | | | P140 to P143 |
| SEG14 to SEG17 | | | | P150 to P153 |
| SEG18 | | | | P25/ANI5[Note] |
| SEG19 | | | | P24/ANI4[Note] |
| SEG20 | | | | P23/ANI3[Note] |
| SEG21 | | | | P22/ANI2[Note] |
| SEG22 | | | | P21/ANI1[Note] |
| SEG23 | | | | P20/ANI0[Note] |
| COM0 to COM3 | Output | LCD controller/driver common signal outputs | Output | – |
| COM4 to COM7 | | | | SEG0 to SEG3 |
| $V_{LC0}$ to $V_{LC2}$ | – | LCD drive voltage | – | – |
| $V_{LC3}$ | | | Input port | P40/KR0 |

**Note** $\mu$PD78F043x only.

**Figure 3-6. Correspondence between Data Memory and Addressing (μPD78F0421, 78F0431)**



### 3.4.4 Short direct addressing

**[Function]**

The memory to be manipulated in the fixed space is directly addressed with 8-bit data in an instruction word.

This addressing is applied to the 256-byte space FE20H to FF1FH. Internal high-speed RAM and special function registers (SFRs) are mapped at FE20H to FEFFH and FF00H to FF1FH, respectively.

The SFR area (FF00H to FF1FH) where short direct addressing is applied is a part of the overall SFR area. Ports that are frequently accessed in a program and compare and capture registers of the timer/event counter are mapped in this area, allowing SFRs to be manipulated with a small number of bytes and clocks.

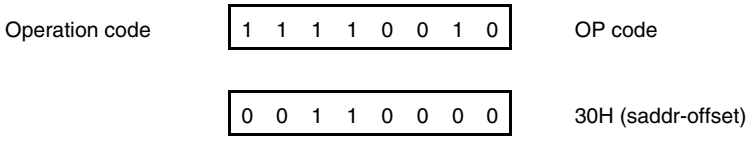
When 8-bit immediate data is at 20H to FFH, bit 8 of an effective address is set to 0. When it is at 00H to 1FH, bit 8 is set to 1. See the **[Illustration]** shown below.

**[Operand format]**

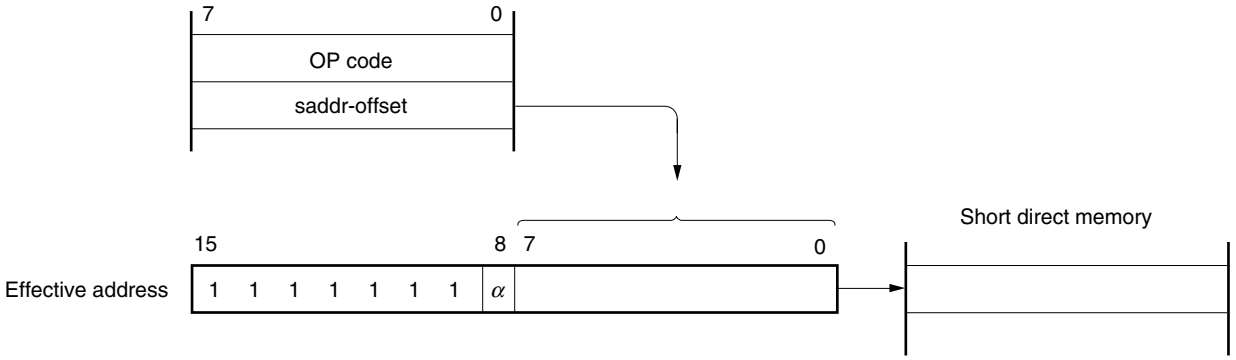
| Identifier | Description |
|---|---|
| saddr | Immediate data that indicate label or FE20H to FF1FH |
| saddrp | Immediate data that indicate label or FE20H to FF1FH (even address only) |

**[Description example]**

MOV 0FE30H, A ; When transferring the value of A register to the saddr (FE30H)




**[Illustration]**




When 8-bit immediate data is 20H to FFH, $\alpha = 0$

When 8-bit immediate data is 00H to 1FH, $\alpha = 1$

### 4.2.2 Port 2

Port 2 is a 6-bit I/O port with an output latch. Port 2 can be set to the input mode or output mode in 1-bit units using port mode register 2 (PM2).

This port can also be used for 10-bit successive approximation type A/D converter analog input ($\mu$PD78F043x only) and segment output.

To use P20/SEG23/ANI0[Note] to P25/SEG18/ANI5[Note] as digital input pins, set them to port function (other than segment output) by using the port function register 2 (PF2), to digital I/O by using ADPC0, and to input mode by using PM2. Use these pins starting from the lower bit.

P20/SEG23/ANI0[Note] to P25/SEG18/ANI5[Note] as digital output pins, set them to port function (other than segment output) by using the port function register 2 (PF2), to digital I/O by using ADPC0, and to output mode by using PM2. Use these pins starting from the lower bit.

Reset signal generation sets port 2 to input mode.

Figure 4-5 shows block diagrams of port 2.

**Table 4-4. Setting Functions of P20/SEG23/ANI0[Note] to P25/SEG18/ANI5[Note] Pins**

| PF2 | ADPC0[Note] | PM2 | ADS | P20/SEG23/ANI0[Note] to P25/SEG18/ANI5[Note] Pins |
|---|---|---|---|---|
| Digital/Analog selection | Analog input selection | Input mode | Does not select ANI. | Analog input (not to be converted) |
| | | | Selects ANI. | Analog input (to be converted by successive approximation type A/D converter) |
| | | Output mode | – | Setting prohibited |
| | Digital I/O selection | Input mode | – | Digital input |
| | | Output mode | – | Digital output |
| SEG output selection | – | – | – | Segment output |

**Note** $\mu$PD78F043x only.

**Remarks 1.** $f_X$: X1 clock oscillation frequency
**2.** $f_{RH}$: Internal high-speed oscillation clock frequency
**3.** $f_{EXCLK}$: External main system clock frequency
**4.** $f_{XH}$: High-speed system clock frequency
**5.** $f_{XP}$: Main system clock frequency
**6.** $f_{PRS}$: Peripheral hardware clock frequency
**7.** $f_{CPU}$: CPU clock frequency
**8.** $f_{XT}$: XT1 clock oscillation frequency
**9.** $f_{SUB}$: Subsystem clock frequency
**10.** $f_{RL}$: Internal low-speed oscillation clock frequency

## 5.3 Registers Controlling Clock Generator

The following eight registers are used to control the clock generator.

- Clock operation mode select register (OSCCTL)
- Processor clock control register (PCC)
- Internal oscillation mode register (RCM)
- Main OSC control register (MOC)
- Main clock mode register (MCM)
- Oscillation stabilization time counter status register (OSTC)
- Oscillation stabilization time select register (OSTS)
- Internal high-speed oscillation trimming register (HIOTRM)

**(1) Clock operation mode select register (OSCCTL)**

This register selects the operation modes of the high-speed system and subsystem clocks, and the gain of the on-chip oscillator.

OSCCTL can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

**(1) 8-bit timer counter 5n (TM5n)**

TM5n is an 8-bit register that counts the count pulses and is read-only.

The counter is incremented in synchronization with the rising edge of the count clock.

**Figure 7-4. Format of 8-Bit Timer Counter 5n (TM5n)**

Address: FF16H (TM50), FF6FH (TM51), FF51H (TM52) After reset: 00H R

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| TM5n (n = 0-2) | | | | | | | | |

In the following situations, the count value is cleared to 00H.

<1> Reset signal generation

<2> When TCE5n is cleared

<3> Match of the TM5n and CR5n.

**(2) 8-bit timer compare register 5n (CR5n)**

CR5n can be read and written by an 8-bit memory manipulation instruction.

The value set in CR5n is constantly compared with the 8-bit timer counter 5n (TM5n) count value, and an interrupt request (INTTM5n) is generated if they match.

The value of CR5n can be set within 00H to FFH.

Reset signal generation sets CR5n to 00H.

**Figure 7-5. Format of 8-Bit Timer Compare Register 5n (CR5n)**

Address: FF17H (CR50), FF41H (CR51), FF59H (CR52) After reset: 00H R/W

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| CR5n (n = 0-2) | | | | | | | | |

**Caution Do not write other values to CR5n during operation.**

**Remark** n = 0 to 2

**Cautions 1. When TMHE1 = 1, setting the other bits of TMHMD1 is prohibited. However, TMHMD1 can be refreshed (the same value is written).**

**2. In the PWM output mode and carrier generator mode, be sure to set the 8-bit timer H compare register 11 (CMP11) when starting the timer count operation (TMHE1 = 1) after the timer count operation was stopped (TMHE1 = 0) (be sure to set again even if setting the same value to CMP11).**

**3. When the carrier generator mode is used, set so that the count clock frequency of TMH1 becomes more than 6 times the count clock frequency of TM51.**

**4. The actual TOH1/P31/INTP3 pin output is determined depending on PM31 and P31, besides TOH1 output.**

**Remarks 1.** $f_{PRS}$: Peripheral hardware clock frequency

**2.** $f_{RL}$: Internal low-speed oscillation clock frequency

### 8.4.2 Operation as PWM output

In PWM output mode, a pulse with an arbitrary duty and arbitrary cycle can be output.

The 8-bit timer compare register 0n (CMP0n) controls the cycle of timer output (TOHn). Rewriting the CMP0n register during timer operation is prohibited.

The 8-bit timer compare register 1n (CMP1n) controls the duty of timer output (TOHn). Rewriting the CMP1n register during timer operation is possible.

The operation in PWM output mode is as follows.

PWM output (TOHn output) outputs an active level and 8-bit timer counter Hn is cleared to 0 when 8-bit timer counter Hn and the CMP0n register match after the timer count is started. PWM output (TOHn output) outputs an inactive level when 8-bit timer counter Hn and the CMP1n register match.

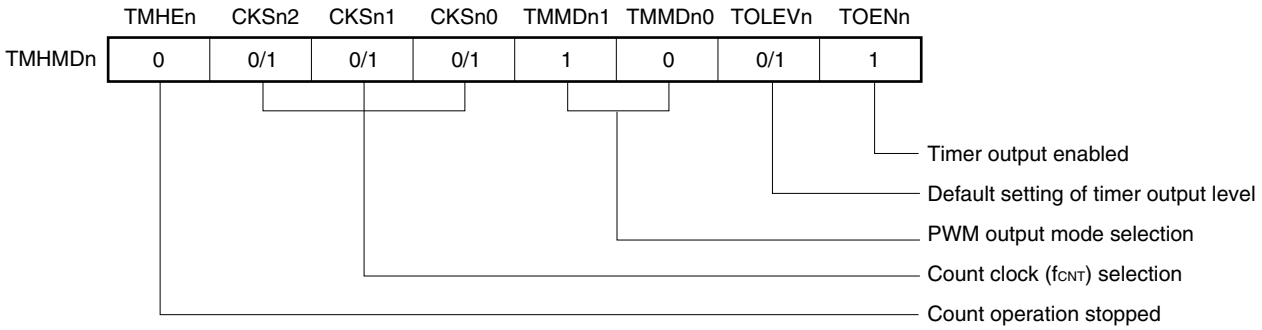
The timer output of TMH2 (PWM output) can only be used as an external event input enable signal of TM52. Note, no pins for external output are available.

Setting

<1> Set each register.

**Figure 8-13. Register Setting in PWM Output Mode**

**(i) Setting timer H mode register n (TMHMDn)**




**(ii) Setting CMP0n register**

- Compare value (N): Cycle setting

**(iii) Setting CMP1n register**

- Compare value (M): Duty setting

**Remarks 1.** n = 0 to 2, however, TOH0 and TOH1 only for TOHn

**2.** 00H ≤ CMP1n (M) < CMP0n (N) ≤ FFH

<2> The count operation starts when TMHEn = 1.

<3> The CMP0n register is the compare register that is to be compared first after counter operation is enabled. When the values of the 8-bit timer counter Hn and the CMP0n register match, the 8-bit timer counter Hn is cleared, an interrupt request signal (INTTMHn) is generated, an active level is output. At the same time, the compare register to be compared with the 8-bit timer counter Hn is changed from the CMP0n register to the CMP1n register.

**Table 9-2. Displayed Time Digits**

| 24-Hour System | 12-Hour System | 24-Hour System | 12-Hour System |
|---|---|---|---|
| 00 | 12 (AM12) | 12 | 32 (PM12) |
| 01 | 01 (AM1) | 13 | 21 (PM1) |
| 02 | 02 (AM2) | 14 | 22 (PM2) |
| 03 | 03 (AM3) | 15 | 23 (PM3) |
| 04 | 04 (AM4) | 16 | 24 (PM4) |
| 05 | 05 (AM5) | 17 | 25 (PM5) |
| 06 | 06 (AM6) | 18 | 26 (PM6) |
| 07 | 07 (AM7) | 19 | 27 (PM7) |
| 08 | 08 (AM8) | 20 | 28 (PM8) |
| 09 | 09 (AM9) | 21 | 29 (PM9) |
| 10 | 10 (AM10) | 22 | 30 (PM10) |
| 11 | 11 (AM11) | 23 | 31 (PM11) |

**(3) Real-time counter control register 1 (RTCC1)**

The RTCC1 register is an 8-bit register that is used to control the alarm interrupt function and the wait time of the counter.

RTCC1 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

**Figure 9-4. Format of Real-Time Counter Control Register 1 (RTCC1) (1/2)**

Address: FF8AH After reset: 00H R/W

| Symbol | <7> | <6> | 5 | <4> | <3> | 2 | <1> | <0> |
|---|---|---|---|---|---|---|---|---|
| RTCC1 | WALE | WALIE | 0 | WAFG | RIFG | 0 | RWST | RWAIT |

| WALE | Alarm operation control |
|---|---|
| 0 | Match operation is invalid. |
| 1 | Match operation is valid. |
| To set the registers of alarm (WALIE flag of RTCC1, ALARMWM register, ALARMWH register, and ALARMWW register), disable WALE (clear it to “0”). | |

| WALIE | Control of alarm interrupt (INTRTC) function operation |
|---|---|
| 0 | Does not generate interrupt on matching of alarm. |
| 1 | Generates interrupt on matching of alarm. |

| WAFG | Alarm detection status flag |
|---|---|
| 0 | Alarm mismatch |
| 1 | Detection of matching of alarm |
| This is a status flag that indicates detection of matching with the alarm. It is valid only when WALE = 1 and is set to “1” one clock (32.768 kHz) after matching of the alarm is detected. This flag is cleared when “0” is written to it. Writing “1” to it is invalid. | |

# CHAPTER 10 WATCHDOG TIMER

## 10.1 Functions of Watchdog Timer

The watchdog timer operates on the internal low-speed oscillation clock.

The watchdog timer is used to detect an inadvertent program loop. If a program loop is detected, an internal reset signal is generated.

Program loop is detected in the following cases.

- If the watchdog timer counter overflows
- If a 1-bit manipulation instruction is executed on the watchdog timer enable register (WDTE)
- If data other than “ACH” is written to WDTE
- If data is written to WDTE during a window close period
- If the instruction is fetched from an area not set by the IMS register (detection of an invalid check while the CPU hangs up)
- If the CPU accesses an area that is not set by the IMS register (excluding FB00H to FFFFH) by executing a read/write instruction (detection of an abnormal access during a CPU program loop)

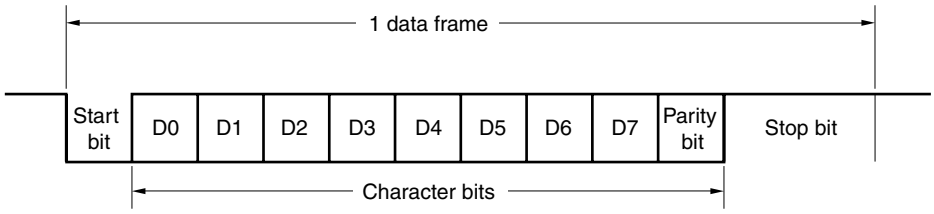
When a reset occurs due to the watchdog timer, bit 4 (WDTRF) of the reset control flag register (RESF) is set to 1. For details of RESF, see **CHAPTER 22 RESET FUNCTION**.

### (2) Communication operation

#### (a) Format and waveform example of normal transmit/receive data

Figures 13-7 and 13-8 show the format and waveform example of the normal transmit/receive data.

**Figure 13-7. Format of Normal UART Transmit/Receive Data**



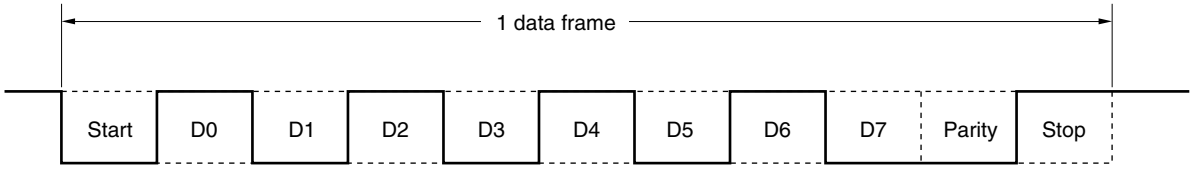

One data frame consists of the following bits.

- Start bit ... 1 bit
- Character bits ... 7 or 8 bits (LSB first)
- Parity bit ... Even parity, odd parity, 0 parity, or no parity
- Stop bit ... 1 or 2 bits

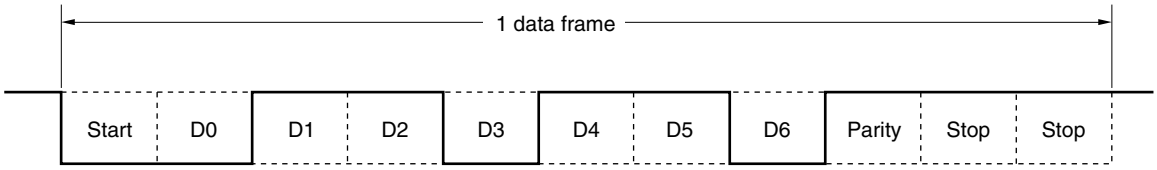
The character bit length, parity, and stop bit length in one data frame are specified by asynchronous serial interface operation mode register 0 (ASIM0).

**Figure 13-8. Example of Normal UART Transmit/Receive Data Waveform**

**1. Data length: 8 bits, Parity: Even parity, Stop bit: 1 bit, Communication data: 55H**




**2. Data length: 7 bits, Parity: Odd parity, Stop bit: 2 bits, Communication data: 36H**




**3. Data length: 8 bits, Parity: None, Stop bit: 1 bit, Communication data: 87H**

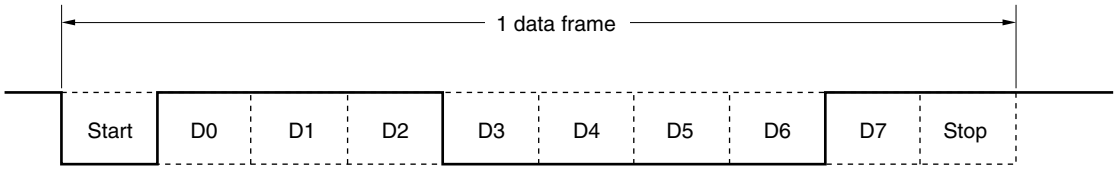
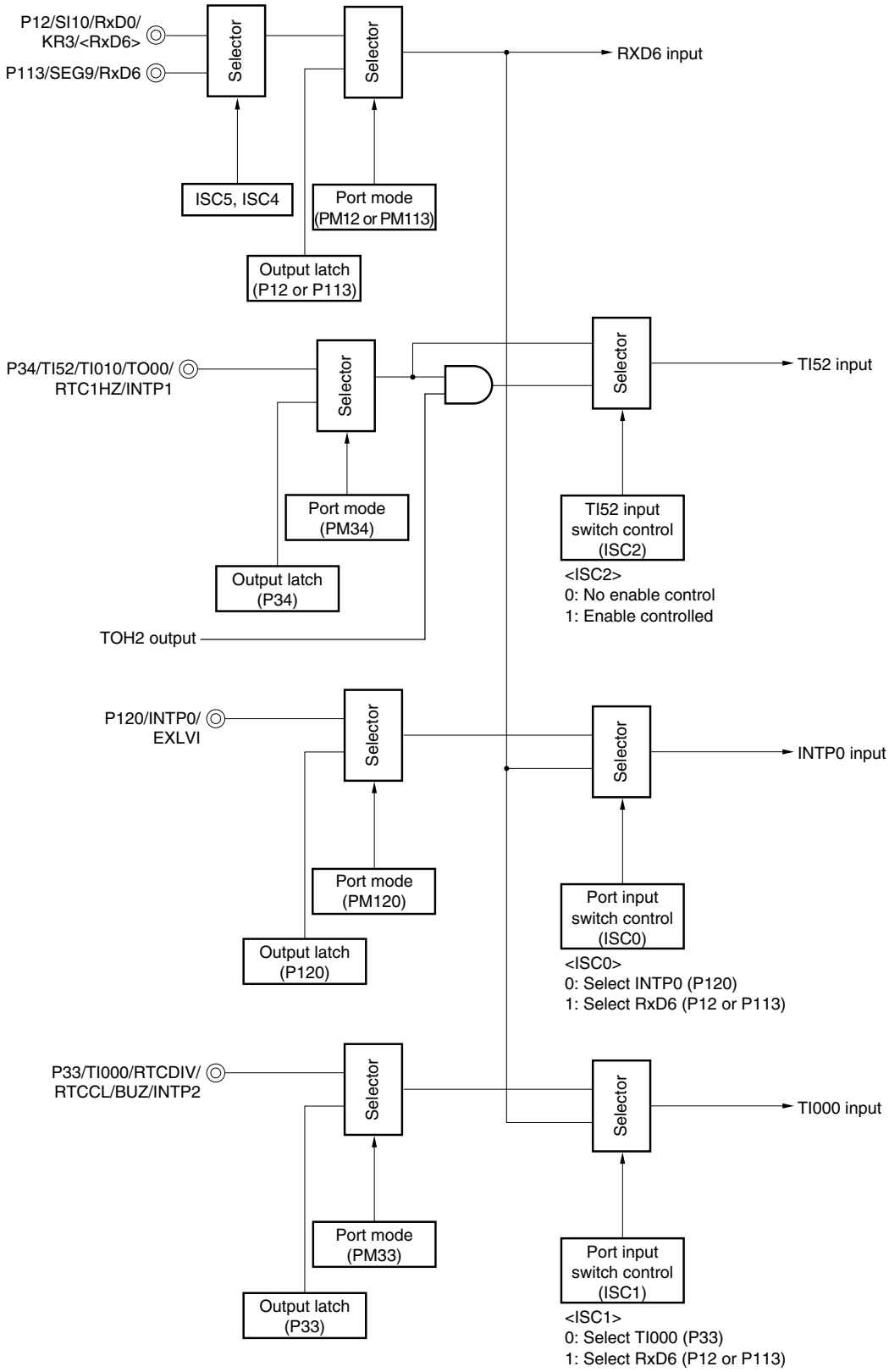


**Figure 14-3. Port Configuration for LIN Reception Operation**




**Remark** ISC0, ISC1, ISC2, ISC4, ISC5: Bits 0, 1, 2, 4 and 5 of the input switch control register (ISC) (see **Figure 14-11**)

**(d) Port mode register 3 (PM3)**

This register sets port 3 input/output in 1-bit units.

When using the P32/TOH0/MCGO pin for bit sequential data output, clear PM32 to 0 and clear the output latch of P32 to 0.

PM3 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

Address: FF23H After reset: FFH R/W

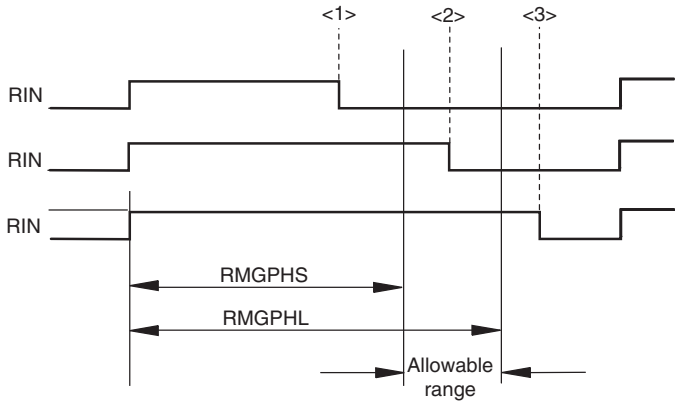
| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| PM3 | 1 | 1 | 1 | PM34 | PM33 | PM32 | PM31 | 1 |

| PM3n | P3n pin I/O mode selection (n = 1 to 4) |
|---|---|
| 0 | Output mode (output buffer on) |
| 1 | Input mode (output buffer off) |

### 18.4.3 Timing

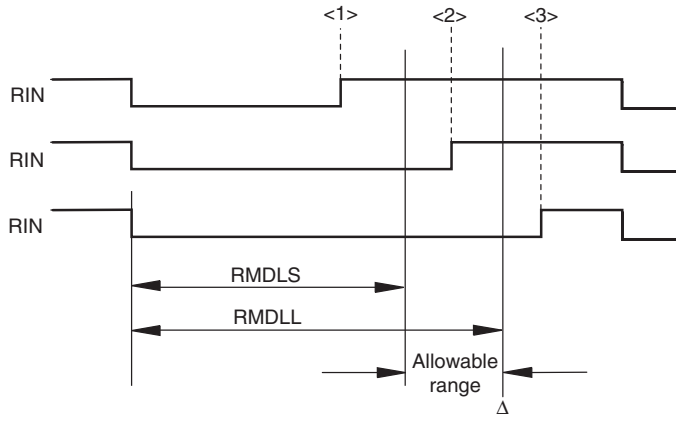
Operation varies depending on the positions of the RIN input waveform below.

#### (1) Guide pulse high level width determination




| Relationship Between RMGPHS/RMGPHL/Counter | Position of Waveform | Corresponding Operation |
|---|---|---|
| Counter < PMGPHS | <1>: Short | Measuring guide pulse high-level width is started from the next rising edge. |
| PMGPHS ≤ counter < PMGPHL | <2>: Within the range | INTGP is generated.<br>Data measurement is started. |
| PMGPHL ≤ counter | <3>: Long | Measuring guide pulse high-level width is started from the next rising edge. |

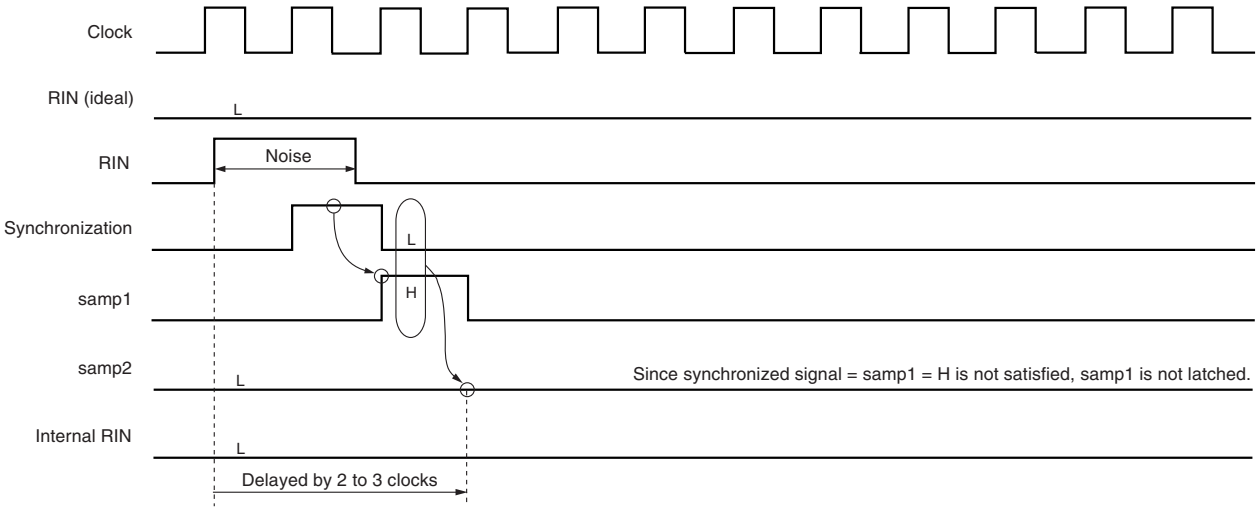
#### (2) Data low level width determination




| Relationship Between RMDLS/RMDLL/Counter | Position of Waveform | Corresponding Operation |
|---|---|---|
| Counter < RMDLS | <1>: Short | Error interrupt INTRERR is generated.<br>Measuring guide pulse high-level width is started. |
| RMDLS ≤ counter < RMDLL | <2>: Within the range | Measuring data high-level width is started. |
| RMDLL ≤ counter | <3>: Long | Measuring the end width is started from the Δ point. |

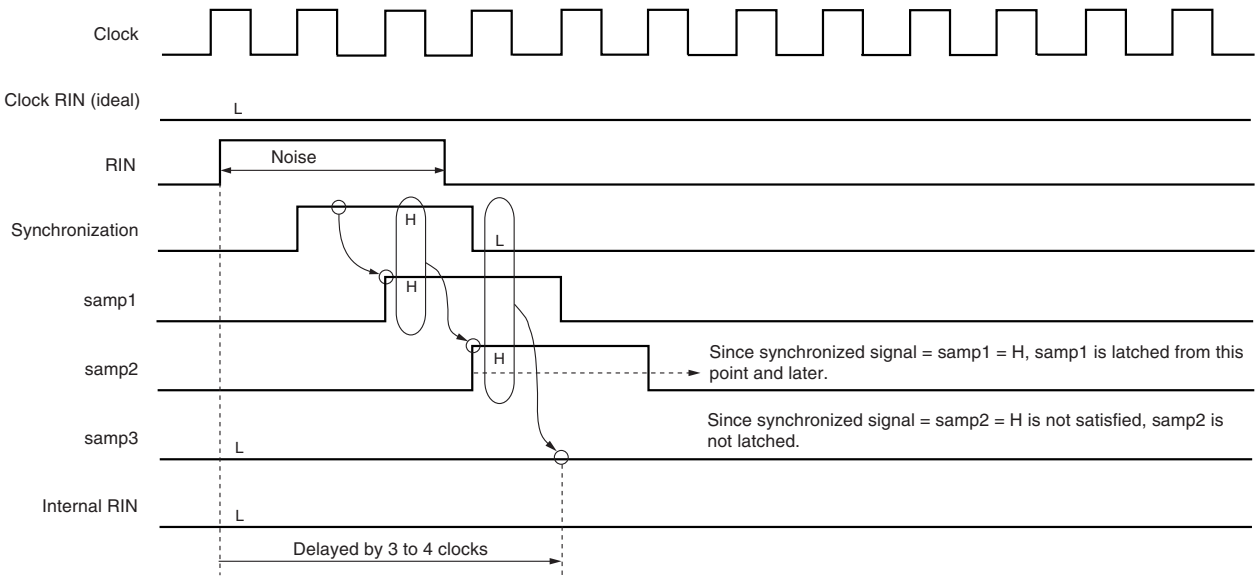
**Figure 18-10. Noise Elimination Operation Example (1/2)**

**(a) 1-clock noise elimination (PRSEN = 0, NCW = 0)**




**Remark** Internal RIN is a signal after synchronization and sampling are performed twice, and is therefore later than the actual signal input from the outside to the RIN pin by two to three clocks.

**(b) 2-clock noise elimination (PRSEN = 0, NCW = 1)**




**Remark** Internal RIN is a signal after synchronization and sampling are performed three times, and is therefore later than the actual signal input from the outside to the RIN pin by 3 to 4 clocks.

## 19.4 Interrupt Servicing Operations

### 19.4.1 Maskable interrupt acknowledgment

A maskable interrupt becomes acknowledgeable when the interrupt request flag is set to 1 and the mask (MK) flag corresponding to that interrupt request is cleared to 0. A vectored interrupt request is acknowledged if interrupts are in the interrupt enabled state (when the IE flag is set to 1). However, a low-priority interrupt request is not acknowledged during servicing of a higher priority interrupt request (when the ISP flag is reset to 0).

The times from generation of a maskable interrupt request until vectored interrupt servicing is performed are listed in Table 19-4 below.

For the interrupt request acknowledgment timing, see **Figures 19-8** and **19-9**.

**Table 19-4. Time from Generation of Maskable Interrupt Until Servicing**

| | Minimum Time | Maximum Time[Note] |
|---|---|---|
| When ××PR = 0 | 7 clocks | 32 clocks |
| When ××PR = 1 | 8 clocks | 33 clocks |

**Note** If an interrupt request is generated just before a divide instruction, the wait time becomes longer.

**Remark** 1 clock: $1/f_{CPU}$ ($f_{CPU}$: CPU clock)

If two or more maskable interrupt requests are generated simultaneously, the request with a higher priority level specified in the priority specification flag is acknowledged first. If two or more interrupts requests have the same priority level, the request with the highest default priority is acknowledged first.

An interrupt request that is held pending is acknowledged when it becomes acknowledgeable.

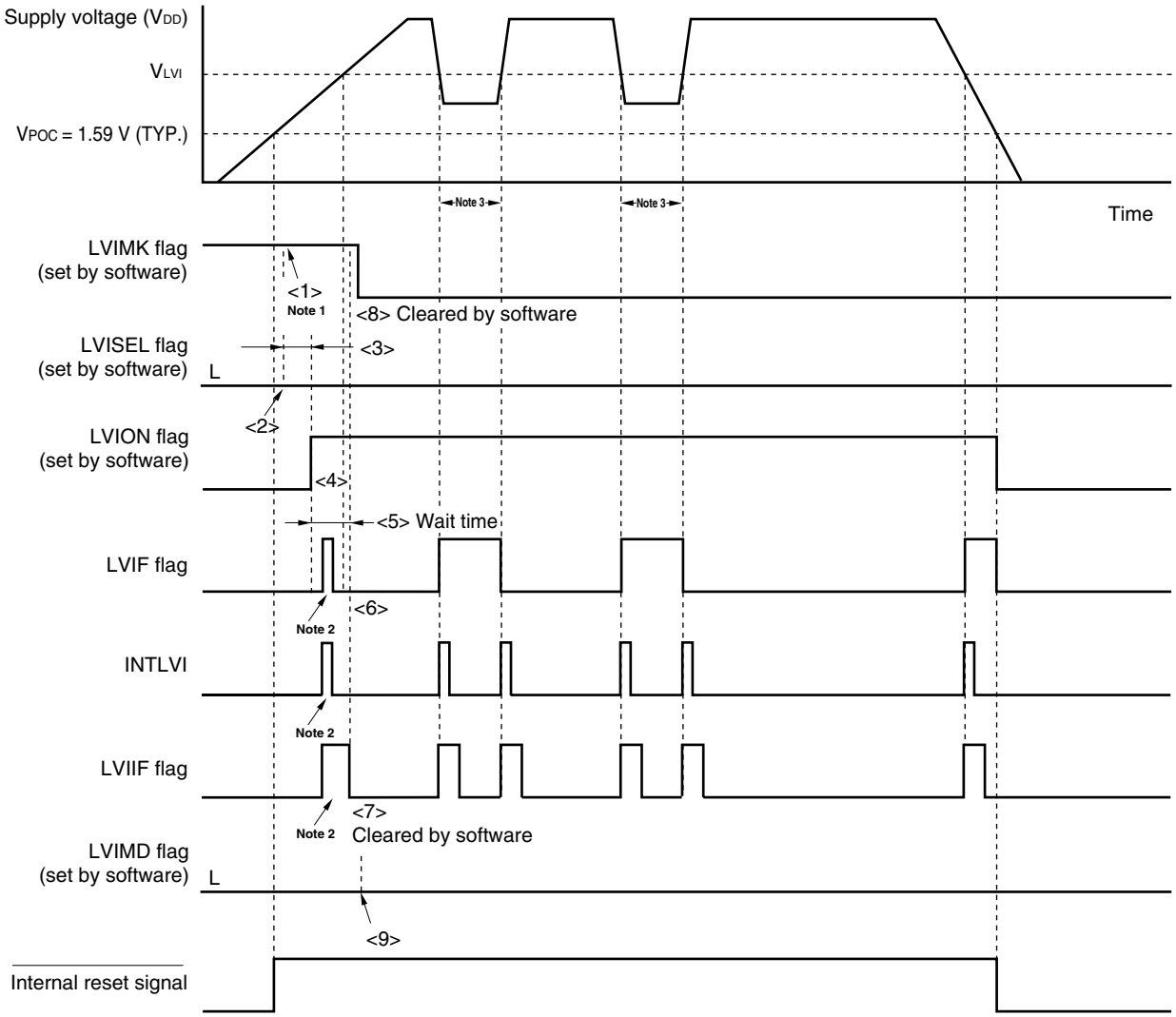
Figure 19-7 shows the interrupt request acknowledgment algorithm.

If a maskable interrupt request is acknowledged, the contents are saved into the stacks in the order of PSW, then PC, the IE flag is reset (0), and the contents of the priority specification flag corresponding to the acknowledged interrupt are transferred to the ISP flag. The vector table data determined for each interrupt request is the loaded into the PC and branched.

Restoring from an interrupt is possible by using the RETI instruction.

**Figure 24-7. Timing of Low-Voltage Detector Interrupt Signal Generation (Detects Level of Supply Voltage ($V_{DD}$)) (1/2)**

**(1) In 1.59 V POC mode (option byte: POCMODE = 0)**




**Notes 1.** The LVIMK flag is set to "1" by reset signal generation.

**2.** The interrupt request signal (INTLVI) is generated and the LVIF and LVIIF flags may be set (1).

**3.** If LVION is cleared (0) in a state below the LVI detection voltage, an INTLVI signal is generated and LVIIF becomes 1.

**Remark** <1> to <9> in Figure 24-7 above correspond to <1> to <9> in the description of "When starting operation" in **24.4.2 (1) When detecting level of supply voltage ($V_{DD}$)**.

## 25.2 Format of Option Byte

The format of the option byte is shown below.

**Figure 25-1. Format of Option Byte (1/2)**

Address: 0080H/1080H[Note]

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | WINDOW1 | WINDOW0 | WDTON | WDCS2 | WDCS1 | WDCS0 | LSROSC |

| WINDOW1 | WINDOW0 | Watchdog timer window open period |
|---|---|---|
| 0 | 0 | 25% |
| 0 | 1 | 50% |
| 1 | 0 | 75% |
| 1 | 1 | 100% |

| WDTON | Operation control of watchdog timer counter/illegal access detection |
|---|---|
| 0 | Counter operation disabled (counting stopped after reset), illegal access detection operation disabled |
| 1 | Counter operation enabled (counting started after reset), illegal access detection operation enabled |

| WDCS2 | WDCS1 | WDCS0 | Watchdog timer overflow time |
|---|---|---|---|
| 0 | 0 | 0 | $2^{10}/f_{RL}$ (3.88 ms) |
| 0 | 0 | 1 | $2^{11}/f_{RL}$ (7.76 ms) |
| 0 | 1 | 0 | $2^{12}/f_{RL}$ (15.52 ms) |
| 0 | 1 | 1 | $2^{13}/f_{RL}$ (31.03 ms) |
| 1 | 0 | 0 | $2^{14}/f_{RL}$ (62.06 ms) |
| 1 | 0 | 1 | $2^{15}/f_{RL}$ (124.12 ms) |
| 1 | 1 | 0 | $2^{16}/f_{RL}$ (248.24 ms) |
| 1 | 1 | 1 | $2^{17}/f_{RL}$ (496.48 ms) |

| LSROSC | Internal low-speed oscillator operation |
|---|---|
| 0 | Can be stopped by software (stopped when 1 is written to bit 1 (LSRSTOP) of RCM register) |
| 1 | Cannot be stopped (not stopped even if 1 is written to LSRSTOP bit) |

**Note** Set a value that is the same as that of 0080H to 1080H because 0080H and 1080H are switched during the boot swap operation.

**Cautions 1. The combination of WDCS2 = WDCS1 = WDCS0 = 0 and WINDOW1 = WINDOW0 = 0 is prohibited.**

**2. The watchdog timer continues its operation during self-programming and EEPROM emulation of the flash memory. During processing, the interrupt acknowledge time is delayed. Set the overflow time and window size taking this delay into consideration.**

**3. If LSROSC = 0 (oscillation can be stopped by software), the count clock is not supplied to the watchdog timer in the HALT and STOP modes, regardless of the setting of bit 1 (LSRSTOP) of the internal oscillation mode register (RCM).**
**When 8-bit timer H1 operates with the internal low-speed oscillation clock, the count clock is supplied to 8-bit timer H1 even in the HALT/STOP mode.**

**4. Be sure to clear bit 7 to 0.**

**Remarks 1.** $f_{RL}$: Internal low-speed oscillation clock frequency

**2.** ( ): $f_{RL}$ = 264 kHz (MAX.)

**DC Characteristics (3/5)**

**($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $AV_{REF}$ ≤ $V_{DD}$, $V_{SS}$ = $AV_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Input leakage current, high | $I_{LIH1}$ | P11 to P13, P31 to P34, P40, P41, P80, P100, P101, P111 to P113, P120, P140 to P143, P150 to P153, FLMD0, $\overline{\text{RESET}}$ | $V_I = V_{DD}$ | | | 1 | μA |
| | $I_{LIH2}$ | P20 to P25 | $V_I = AV_{REF} = V_{DD}$ | | | 1 | μA |
| | $I_{LIH3}$ | P121 to 124 (X1, X2, XT1, XT2) | $V_I = V_{DD}$ I/O port mode | | | 1 | μA |
| | | | OSC mode | | | 20 | μA |
| Input leakage current, low | $I_{LIL1}$ | P11 to P13, P31 to P34, P40, P41, P80, P100, P101, P111 to P113, P120, P140 to P143, P150 to P153, FLMD0, $\overline{\text{RESET}}$ | $V_I = V_{SS}$ | | | –1 | μA |
| | $I_{LIL2}$ | P20 to P25 | $V_I = V_{SS}$, $AV_{REF} = V_{DD}$ | | | –1 | μA |
| | $I_{LIL3}$ | P121 to 124 (X1, X2, XT1, XT2) | $V_I = V_{SS}$ I/O port mode | | | –1 | μA |
| | | | OSC mode | | | –20 | μA |
| Pull-up resistor | $R_U$ | $V_I = V_{SS}$ | | 10 | 20 | 100 | kΩ |
| FLMD0 supply voltage | $V_{IL}$ | In normal operation mode | | 0 | | $0.2V_{DD}$ | V |
| | $V_{IH}$ | In self-programming mode | | $0.8V_{DD}$ | | $V_{DD}$ | V |

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

**(2) Serial interface**

**($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $AV_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Transfer rate | | | | | 250 | kbps |

**(3) Serial interface**

**($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $AV_{SS}$ = 0 V)**

**(a) UART6 (Dedicated baud rate generator output)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Transfer rate | | | | | 625 | kbps |

**(b) UART0 (Dedicated baud rate generator output)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Transfer rate | | | | | 625 | kbps |