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#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

E·XFI

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I <sup>2</sup> C, LINbus, SPI, TSI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LVD, POR, PWM, WDT
Number of I/O	54
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mkl15z128vlh4r

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

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# 3.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

## 3.2.1 Example

This is an example of an operating behavior, which is guaranteed if you meet the accompanying operating requirements:

Symbol	Description	Min.	Max.	Unit
I <sub>WP</sub>	Digital I/O weak pullup/ pulldown current	10	130	μA

## 3.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

## 3.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

# 3.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

- Operating ratings apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

## 3.4.1 Example

This is an example of an operating rating:

Symbol	Description	Min.	Max.	Unit
V <sub>DD</sub>	1.0 V core supply voltage	-0.3	1.2	V

## 3.5 Result of exceeding a rating



# 3.6 Relationship between ratings and operating requirements



## 3.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

## 3.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

## 3.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Тур.	Max.	Unit
I <sub>WP</sub>	Digital I/O weak pullup/pulldown current	10	70	130	μΑ

## 3.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



# 3.9 Typical Value Conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T <sub>A</sub>	Ambient temperature	25	٥C
V <sub>DD</sub>	3.3 V supply voltage	3.3	V

# 4 Ratings

## 4.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T <sub>STG</sub>	Storage temperature	-55	150	°C	1
T <sub>SDR</sub>	Solder temperature, lead-free	_	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, High Temperature Storage Life.

2. Determined according to IPC/JEDEC Standard J-STD-020, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.

## 4.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	_	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 4.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V <sub>HBM</sub>	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V <sub>CDM</sub>	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I <sub>LAT</sub>	Latch-up current at ambient temperature of 105°C	-100	+100	mA	

- 1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
- 2. Determined according to JEDEC Standard JESD22-C101, Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components.

## 4.4 Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V <sub>DD</sub>	Digital supply voltage	-0.3	3.8	V
I <sub>DD</sub>	Digital supply current	—	120	mA
V <sub>DIO</sub>	Digital pin input voltage (except RESET)	-0.3	3.6	V
V <sub>AIO</sub>	Analog pins <sup>1</sup> and RESET pin input voltage	-0.3	V <sub>DD</sub> + 0.3	V
۱ <sub>D</sub>	Instantaneous maximum current single pin limit (applies to all port pins)	-25	25	mA
V <sub>DDA</sub>	Analog supply voltage	$V_{DD} - 0.3$	V <sub>DD</sub> + 0.3	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

## 5 General

Table 3.	<ul> <li>Voltage and current operating behaviors (con</li> </ul>	itinued)
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Symbol	Description	Min.	Max.	Unit	Notes
R <sub>PU</sub>	Internal pullup resistors	20	50	kΩ	3
R <sub>PD</sub>	Internal pulldown resistors	20	50	kΩ	4

<sup>1.</sup> PTB0, PTB1, PTD6, and PTD7 I/O have both high drive and normal drive capability selected by the associated PTx\_PCRn[DSE] control bit. All other GPIOs are normal drive only.

2. Measured at  $V_{DD} = 3.6 V$ 

- 3. Measured at  $V_{DD}$  supply voltage =  $V_{DD}$  min and Vinput =  $V_{SS}$
- 4. Measured at  $V_{DD}$  supply voltage =  $V_{DD}$  min and Vinput =  $V_{DD}$

## 5.2.4 Power mode transition operating behaviors

All specifications except  $t_{POR}$  and VLLSx $\rightarrow$ RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 48 MHz
- Bus and flash clock = 24 MHz
- FEI clock mode

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
t <sub>POR</sub>	After a POR event, amount of time from the point $V_{DD}$ reaches 1.8 V to execution of the first instruction across the operating temperature range of the chip.		—	300	μs	
	• VLLS0 $\rightarrow$ RUN	_	95	115	μs	
	• VLLS1 $\rightarrow$ RUN	_	93	115	μs	
	• VLLS3 $\rightarrow$ RUN		42	53	μs	
	• LLS → RUN	_	4	4.6	μs	
	• VLPS → RUN		4	4.4	μs	
	• STOP $\rightarrow$ RUN		4	4.4	μs	

 Table 4. Power mode transition operating behaviors

## 5.2.5 Power consumption operating behaviors

Table 5. Power consumption operating behaviors

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
I <sub>DDA</sub>	Analog supply current	_	_	See note	mA	1
I <sub>DD_RUNCO_</sub> CM	Run mode current in compute operation - 48 MHz core / 24 MHz flash/ bus disabled, LPTMR running using 4MHz internal reference clock, CoreMark® benchmark code executing from flash • at 3.0 V	_	6.4	_	mA	2
I <sub>DD_RUNCO</sub>	Run mode current in compute operation - 48 MHz core / 24 MHz flash / bus clock disabled, code of while(1) loop executing from flash • at 3.0 V		4.1	5.2	mA	3
I <sub>DD_RUN</sub>	Run mode current - 48 MHz core / 24 MHz bus and flash, all peripheral clocks disabled, code of while(1) loop executing from flash • at 3.0 V	_	5.1	6.3	mA	3
I <sub>DD_RUN</sub>	Run mode current - 48 MHz core / 24 MHz bus and flash, all peripheral clocks enabled, code of while(1) loop executing from flash					3, 4,
	• at 25 °C	_	6.4	7.8	mA	
	• at 125 °C	_	6.8	8.3	mA	
I <sub>DD_WAIT</sub>	Wait mode current - core disabled / 48 MHz system / 24 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled • at 3.0 V	_	3.7	5.0	mA	3
I <sub>DD_WAIT</sub>	Wait mode current - core disabled / 24 MHz system / 24 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled • at 3.0 V	_	2.9	4.2	mA	3
I <sub>DD_PSTOP2</sub>	Stop mode current with partial stop 2 clocking option - core and system disabled / 10.5 MHz bus • at 3.0 V	_	2.5	3.7	mA	3
IDD_VLPRCO	Very low power run mode current in compute operation - 4 MHz core / 0.8 MHz flash / bus clock disabled, code of while(1) loop executing from flash • at 3.0 V		188	570	μΑ	5
IDD_VLPR	Very low power run mode current - 4 MHz core / 0.8 MHz bus and flash, all peripheral clocks disabled, code of while(1) loop executing from flash • at 3.0 V		224	613	μA	5

Table continues on the next page...

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
I <sub>DD_VLLS0</sub>	Very low-leakage stop mode 0 current (SMC_STOPCTRL[PORPO] = 0) at 3.0 V		381	043	nA	
	at 25 °C	_	956	11760		
	at 50 °C	_	2370	13260		
	at 70 °C	_	4800	15700		
	at 85 °C	_	12410	23480		
	at 105 °C					
I <sub>DD_VLLS0</sub>	Very low-leakage stop mode 0 current (SMC_STOPCTRL[PORPO] = 1) at 3.0 V	_	176	860		6
	at 25 °C	_	760	3577	nA	
	at 50 °C	_	2120	11660		
	at 70 °C	_	4500	18450		
	at 85 °C	_	12130	22441		
	at 105 °C					

### Table 5. Power consumption operating behaviors (continued)

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.

- 2. MCG configured for PEE mode. CoreMark benchmark compiled using Keil 4.54 with optimization level 3, optimized for time.
- 3. MCG configured for FEI mode.
- 4. Incremental current consumption from peripheral activity is not included.
- 5. MCG configured for BLPI mode.
- 6. No brownout

### Table 6. Low power mode peripheral adders — typical value

Symbol	Description		Temperature (°C)					Unit
		-40	25	50	70	85	105	
I <sub>IREFSTEN4MHz</sub>	4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled.	56	56	56	56	56	56	μA
IIREFSTEN32KHz	32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled.	52	52	52	52	52	52	μA
IEREFSTEN4MHz	External 4MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled.	206	228	237	245	251	258	uA

Table continues on the next page ...

- 2.  $V_{DD} = 3.3 \text{ V}, T_A = 25 \text{ °C}, f_{OSC} = 8 \text{ MHz}$  (crystal),  $f_{SYS} = 48 \text{ MHz}, f_{BUS} = 48 \text{ MHz}$
- 3. Specified according to Annex D of IEC Standard 61967-2, Measurement of Radiated Emissions TEM Cell and Wideband TEM Cell Method

## 5.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

- 1. Go to www.freescale.com.
- 2. Perform a keyword search for "EMC design."

## 5.2.8 Capacitance attributes

### Table 8. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C <sub>IN_A</sub>	Input capacitance: analog pins	—	7	pF
C <sub>IN_D</sub>	Input capacitance: digital pins	—	7	pF

## 5.3 Switching specifications

## 5.3.1 Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes			
	Normal run mode							
f <sub>SYS</sub>	System and core clock	_	48	MHz				
f <sub>BUS</sub>	Bus clock	_	24	MHz				
f <sub>FLASH</sub>	Flash clock	—	24	MHz				
f <sub>LPTMR</sub>	LPTMR clock	_	24	MHz				
	VLPR mode <sup>1</sup>				•			
f <sub>SYS</sub>	System and core clock	—	4	MHz				
f <sub>BUS</sub>	Bus clock	_	1	MHz				
f <sub>FLASH</sub>	Flash clock	_	1	MHz				
f <sub>LPTMR</sub>	LPTMR clock	—	24	MHz				
f <sub>ERCLK</sub>	External reference clock	_	16	MHz				
f <sub>LPTMR_pin</sub>	LPTMR clock	_	24	MHz				
f <sub>LPTMR_ERCL</sub>	LPTMR external reference clock	_	16	MHz				
к								

Table continues on the next page ...

## 6.2 System modules

There are no specifications necessary for the device's system modules.

## 6.3 Clock modules

## 6.3.1 MCG specifications

Symbol	Description		Min.	Тур.	Max.	Unit	Notes
f <sub>ints_ft</sub>	Internal reference factory trimmed at	frequency (slow clock) — nominal V <sub>DD</sub> and 25 °C	—	32.768	—	kHz	
f <sub>ints_t</sub>	Internal reference frequency (slow clock) — user trimmed		31.25	—	39.0625	kHz	
Δ <sub>fdco_res_t</sub>	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM		_	± 0.3	± 0.6	%f <sub>dco</sub>	1
∆f <sub>dco_t</sub>	Total deviation of t frequency over vol	rimmed average DCO output tage and temperature	—	+0.5/-0.7	± 3	%f <sub>dco</sub>	1, 2
Δf <sub>dco_t</sub>	Total deviation of t frequency over fixe range of 0 - 70 °C	_	± 0.4	± 1.5	%f <sub>dco</sub>	1, 2	
f <sub>intf_ft</sub>	Internal reference factory trimmed at	_	4	_	MHz		
∆f <sub>intf_ft</sub>	Frequency deviation of internal reference clock (fast clock) over temperature and voltage factory trimmed at nominal V <sub>DD</sub> and 25 °C		_	+1/-2	± 3	%f <sub>intf_ft</sub>	2
f <sub>intf_t</sub>	Internal reference trimmed at nomina	frequency (fast clock) — user al V <sub>DD</sub> and 25 °C	3	—	5	MHz	
f <sub>loc_low</sub>	Loss of external cl RANGE = 00	ock minimum frequency —	(3/5) x f <sub>ints_t</sub>	_	_	kHz	
f <sub>loc_high</sub>	Loss of external cl RANGE = 01, 10,	ock minimum frequency — or 11	(16/5) x f <sub>ints_t</sub>	_		kHz	
		FI	L	•			•
f <sub>fll_ref</sub>	FLL reference free	luency range	31.25		39.0625	kHz	
f <sub>dco</sub>	DCO output	Low range (DRS = 00)	20	20.97	25	MHz	3, 4
	frequency range	$640 \times f_{fll\_ref}$					
		Mid range (DRS = 01)	40	41.94	48	MHz	
		$1280 \times f_{fll\_ref}$					

### Table 12. MCG specifications

Table continues on the next page...

KL15 Sub-Family Data Sheet Data Sheet, Rev. 3, 9/19/2012.

#### Peripheral operating requirements and behaviors

Symbol	Description		Min.	Тур.	Max.	Unit	Notes
f <sub>dco_t_DMX32</sub>	DCO output	Low range (DRS = 00)	_	23.99	—	MHz	5, 6
	frequency	$732 \times f_{fll\_ref}$					
		Mid range (DRS = 01)	_	47.97	—	MHz	
		$1464 \times f_{fll\_ref}$					
J <sub>cyc_fll</sub>	FLL period jitter		—	180	—	ps	7
	• f <sub>VCO</sub> = 48 MHz						
t <sub>fll_acquire</sub>	FLL target frequer	ncy acquisition time	_	—	1	ms	8
		PI	L				
f <sub>vco</sub>	VCO operating fre	quency	48.0	—	100	MHz	
I <sub>pll</sub>	PLL operating cur PLL at 96 M MHz, VDIV	_	1060	_	μA	9	
I <sub>pll</sub>	PLL operating current • PLL at 48 MHz (f <sub>osc_hi_1</sub> = 8 MHz, f <sub>pll_ref</sub> = 2 MHz, VDIV multiplier = 24)		_	600	_	μΑ	9
f <sub>pll_ref</sub>	PLL reference free	quency range	2.0	—	4.0	MHz	
J <sub>cyc_pll</sub>	PLL period jitter (F	RMS)					10
	• f <sub>vco</sub> = 48 MH	lz	—	120	-	ps	
	• f <sub>vco</sub> = 100 M	Hz	—	50	_	ps	
J <sub>acc_pll</sub>	PLL accumulated	jitter over 1µs (RMS)					10
	• f <sub>vco</sub> = 48 MH	lz	—	1350	_	ps	
	• f <sub>vco</sub> = 100 M	Hz	—	600	_	ps	
D <sub>lock</sub>	Lock entry frequer	ncy tolerance	± 1.49	—	± 2.98	%	
D <sub>unl</sub>	Lock exit frequence	y tolerance	± 4.47	—	± 5.97	%	
t <sub>pll_lock</sub>	Lock detector dete	ection time			150 × 10 <sup>-6</sup> + 1075(1/ f <sub>pll_ref</sub> )	S	11

### Table 12. MCG specifications (continued)

- 1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
- 2. The deviation is relative to the factory trimmed frequency at nominal  $V_{DD}$  and 25 °C,  $f_{ints_{t}}$ .
- 3. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32 = 0.
- The resulting system clock frequencies must not exceed their maximum specified values. The DCO frequency deviation (Δf<sub>dco t</sub>) over voltage and temperature must be considered.
- 5. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32 = 1.
- 6. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
- 7. This specification is based on standard deviation (RMS) of period or frequency.
- 8. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

9. Excludes any oscillator currents that are also consuming power while PLL is in operation.

- 10. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
- 11. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

## 6.3.2 Oscillator electrical specifications

This section provides the electrical characteristics of the module.

## 6.3.2.1 Oscillator DC electrical specifications Table 13. Oscillator DC electrical specifications

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
V <sub>DD</sub>	Supply voltage	1.71	—	3.6	V	
I <sub>DDOSC</sub>	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	-	500	—	nA	
	• 4 MHz	_	200	_	μA	
	• 8 MHz (RANGE=01)	_	300	_	μA	
	• 16 MHz	_	950	_	μA	
	• 24 MHz	_	1.2	_	mA	
	• 32 MHz	_	1.5	_	mA	
IDDOSC	Supply current — high gain mode (HGO=1)					1
	• 32 kHz	-	25	—	μA	
	• 4 MHz	-	400	—	μA	
	• 8 MHz (RANGE=01)	_	500	_	μA	
	• 16 MHz	_	2.5	_	mA	
	• 24 MHz	_	3	_	mA	
	• 32 MHz	-	4	_	mA	
C <sub>x</sub>	EXTAL load capacitance	—	—			2, 3
Cy	XTAL load capacitance	—	—	_		2, 3
R <sub>F</sub>	Feedback resistor — low-frequency, low-power mode (HGO=0)	_	_	_	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	_	MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	_	MΩ	

Table continues on the next page ...

KL15 Sub-Family Data Sheet Data Sheet, Rev. 3, 9/19/2012.

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
R <sub>S</sub>	Series resistor — low-frequency, low-power mode (HGO=0)	_	_	_	kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)					
		_	0	_	kΩ	
V <sub>pp</sub> <sup>5</sup>	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	_	0.6	_	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	_	V <sub>DD</sub>	_	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	_	0.6	_	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)		V <sub>DD</sub>		V	

### Table 13. Oscillator DC electrical specifications (continued)

- 1.  $V_{DD}$ =3.3 V, Temperature =25 °C
- 2. See crystal or resonator manufacturer's recommendation
- 3. C<sub>x</sub>,C<sub>y</sub> can be provided by using the integrated capacitors when the low frequency oscillator (RANGE = 00) is used. For all other cases external capacitors must be used.
- 4. When low power mode is selected,  $R_F$  is integrated and must not be attached externally.
- 5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

### 6.3.2.2 Oscillator frequency specifications Table 14. Oscillator frequency specifications

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
f <sub>osc_lo</sub>	Oscillator crystal or resonator frequency — low frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
f <sub>osc_hi_1</sub>	Oscillator crystal or resonator frequency — high frequency mode (low range) (MCG_C2[RANGE]=01)	3	_	8	MHz	
f <sub>osc_hi_2</sub>	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	_	32	MHz	
f <sub>ec_extal</sub>	Input clock frequency (external clock mode)	—	_	48	MHz	1, 2
t <sub>dc_extal</sub>	Input clock duty cycle (external clock mode)	40	50	60	%	

Table continues on the next page...

Symbol	Description	Conditions <sup>1</sup>	Min.	Typ. <sup>2</sup>	Max.	Unit	Notes
E <sub>IL</sub>	Input leakage error			I <sub>In</sub> × R <sub>AS</sub>		mV	I <sub>In</sub> = leakage current (refer to the MCU's voltage and current operating ratinge)
	Temp sensor slope	Across the full temperature range of the device		1.715	_	mV/°C	
V <sub>TEMP25</sub>	Temp sensor voltage	25 °C	_	719	—	mV	

### Table 20. 16-bit ADC characteristics ( $V_{REFH} = V_{DDA}$ , $V_{REFL} = V_{SSA}$ ) (continued)

- 1. All accuracy numbers assume the ADC is calibrated with  $V_{\mathsf{REFH}}$  =  $V_{\mathsf{DDA}}$
- Typical values assume V<sub>DDA</sub> = 3.0 V, Temp = 25°C, f<sub>ADCK</sub> = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
- The ADC supply current depends on the ADC conversion clock speed, conversion rate and the ADLPC bit (low power). For lowest power operation the ADLPC bit must be set, the HSC bit must be clear with 1 MHz ADC conversion clock speed.
- 4. 1 LSB =  $(V_{REFH} V_{REFL})/2^N$
- 5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
- 6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
- 7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.







### Peripheral operating requirements and behaviors

Table 21.	Comparator	and 6-bit DAC	electrical s	pecifications	(continued)	)
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Symbol	Description	Min.	Тур.	Max.	Unit
	Analog comparator initialization delay <sup>2</sup>	—	—	40	μs
I <sub>DAC6b</sub>	6-bit DAC current adder (enabled)	_	7	—	μA
INL	6-bit DAC integral non-linearity	-0.5	—	0.5	LSB <sup>3</sup>
DNL	6-bit DAC differential non-linearity	-0.3	_	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.7 to  $V_{DD}$  – 0.7 V.

- 2. Comparator initialization delay is defined as the time between software writes to change control inputs (writes to DACEN,
- VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
- 3. 1 LSB = V<sub>reference</sub>/64



Figure 9. Typical hysteresis vs. Vin level ( $V_{DD}$  = 3.3 V, PMODE = 0)



Figure 10. Typical hysteresis vs. Vin level (V<sub>DD</sub> = 3.3 V, PMODE = 1)

## 6.6.3 12-bit DAC electrical characteristics



Figure 12. Offset at half scale vs. temperature

# 6.7 Timers

See General switching specifications.

# 6.8 Communication interfaces

## 6.8.1 SPI switching specifications

The Serial Peripheral Interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. See the SPI chapter of the chip's Reference Manual for information about the modified transfer formats used for communicating with slower peripheral devices.

Peripheral operating requirements and behaviors



1. If configured as an output.

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.





1.If configured as output

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

### Figure 14. SPI master mode timing (CPHA = 1)

Table 26.	SPI slave mode	e timing on	slew rate	disabled	pads
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Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f <sub>op</sub>	Frequency of operation	0	f <sub>periph</sub> /4	Hz	1
2	t <sub>SPSCK</sub>	SPSCK period	4 x t <sub>periph</sub>	_	ns	2
3	t <sub>Lead</sub>	Enable lead time	1	_	t <sub>periph</sub>	
4	t <sub>Lag</sub>	Enable lag time	1	—	t <sub>periph</sub>	_
5	t <sub>WSPSCK</sub>	Clock (SPSCK) high or low time	t <sub>periph</sub> - 30		ns	_

Table continues on the next page...

#### Peripheral operating requirements and behaviors

Num.	Symbol	Description	Min.	Max.	Unit	Note
6	t <sub>SU</sub>	Data setup time (inputs)	2	—	ns	—
7	t <sub>HI</sub>	Data hold time (inputs)	7	—	ns	_
8	t <sub>a</sub>	Slave access time	—	t <sub>periph</sub>	ns	3
9	t <sub>dis</sub>	Slave MISO disable time	_	t <sub>periph</sub>	ns	4
10	t <sub>v</sub>	Data valid (after SPSCK edge)	—	22	ns	
11	t <sub>HO</sub>	Data hold time (outputs)	0	—	ns	
12	t <sub>RI</sub>	Rise time input	_	t <sub>periph</sub> - 25	ns	
	t <sub>FI</sub>	Fall time input				
13	t <sub>RO</sub>	Rise time output	—	25	ns	
	t <sub>FO</sub>	Fall time output				

### Table 26. SPI slave mode timing on slew rate disabled pads (continued)

1. For SPI0  $f_{periph}$  is the bus clock ( $f_{BUS}$ ). For SPI1  $f_{periph}$  is the system clock ( $f_{SYS}$ ).

- 2.  $t_{periph} = 1/f_{periph}$
- 3. Time to data active from high-impedance state
- 4. Hold time to high-impedance state

### Table 27. SPI slave mode timing on slew rate enabled pads

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f <sub>op</sub>	Frequency of operation	0	f <sub>periph</sub> /4	Hz	1
2	t <sub>SPSCK</sub>	SPSCK period	4 x t <sub>periph</sub>	_	ns	2
3	t <sub>Lead</sub>	Enable lead time	1	_	t <sub>periph</sub>	
4	t <sub>Lag</sub>	Enable lag time	1		t <sub>periph</sub>	
5	t <sub>WSPSCK</sub>	Clock (SPSCK) high or low time	t <sub>periph</sub> - 30	—	ns	—
6	t <sub>SU</sub>	Data setup time (inputs)	2	—	ns	
7	t <sub>HI</sub>	Data hold time (inputs)	7		ns	
8	t <sub>a</sub>	Slave access time	—	t <sub>periph</sub>	ns	3
9	t <sub>dis</sub>	Slave MISO disable time	—	t <sub>periph</sub>	ns	4
10	t <sub>v</sub>	Data valid (after SPSCK edge)	—	122	ns	
11	t <sub>HO</sub>	Data hold time (outputs)	0	—	ns	
12	t <sub>RI</sub>	Rise time input	—	t <sub>periph</sub> - 25	ns	—
	t <sub>FI</sub>	Fall time input				
13	t <sub>RO</sub>	Rise time output	—	36	ns	_
	t <sub>FO</sub>	Fall time output	]			

1. For SPI0  $f_{periph}$  is the bus clock ( $f_{BUS}$ ). For SPI1  $f_{periph}$  is the system clock ( $f_{SYS}$ ).

- 2.  $t_{periph} = 1/f_{periph}$
- 3. Time to data active from high-impedance state
- 4. Hold time to high-impedance state

# 8.1 KL15 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

80 LQFP	64 LQFP	48 QFN	32 QFN	Pin Name	Default	ALTO	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
1	1	_	1	PTE0	DISABLED		PTE0		UART1_TX	RTC_CLKOUT	CMP0_OUT	I2C1_SDA	
2	2	-	2	PTE1	DISABLED		PTE1	SPI1_MOSI	UART1_RX		SPI1_MISO	I2C1_SCL	
3	_	-	_	PTE2	DISABLED		PTE2	SPI1_SCK					
4	_	-	_	PTE3	DISABLED		PTE3	SPI1_MISO			SPI1_MOSI		
5	-	-	_	PTE4	DISABLED		PTE4	SPI1_PCS0					
6	-	-	-	PTE5	DISABLED		PTE5						
7	3	1	-	VDD	VDD	VDD							
8	4	2	-	VSS	VSS	VSS							
9	5	3	3	PTE16	ADC0_DP1/ ADC0_SE1	ADC0_DP1/ ADC0_SE1	PTE16	SPI0_PCS0	UART2_TX	TPM_CLKIN0			
10	6	4	4	PTE17	ADC0_DM1/ ADC0_SE5a	ADC0_DM1/ ADC0_SE5a	PTE17	SPI0_SCK	UART2_RX	TPM_CLKIN1		LPTMR0_ ALT3	
11	7	5	5	PTE18	ADC0_DP2/ ADC0_SE2	ADC0_DP2/ ADC0_SE2	PTE18	SPI0_MOSI		I2C0_SDA	SPI0_MISO		
12	8	6	6	PTE19	ADC0_DM2/ ADC0_SE6a	ADC0_DM2/ ADC0_SE6a	PTE19	SPI0_MISO		I2C0_SCL	SPI0_MOSI		
13	9	7	_	PTE20	ADC0_DP0/ ADC0_SE0	ADC0_DP0/ ADC0_SE0	PTE20		TPM1_CH0	UART0_TX			
14	10	8	-	PTE21	ADC0_DM0/ ADC0_SE4a	ADC0_DM0/ ADC0_SE4a	PTE21		TPM1_CH1	UART0_RX			
15	11	-	-	PTE22	ADC0_DP3/ ADC0_SE3	ADC0_DP3/ ADC0_SE3	PTE22		TPM2_CH0	UART2_TX			
16	12	_	-	PTE23	ADC0_DM3/ ADC0_SE7a	ADC0_DM3/ ADC0_SE7a	PTE23		TPM2_CH1	UART2_RX			
17	13	9	7	VDDA	VDDA	VDDA							
18	14	10	-	VREFH	VREFH	VREFH							
19	15	11	-	VREFL	VREFL	VREFL							
20	16	12	8	VSSA	VSSA	VSSA							
21	17	13	-	PTE29	CMP0_IN5/ ADC0_SE4b	CMP0_IN5/ ADC0_SE4b	PTE29		TPM0_CH2	TPM_CLKIN0			
22	18	14	9	PTE30	DAC0_OUT/ ADC0_SE23/ CMP0_IN4	DAC0_OUT/ ADC0_SE23/ CMP0_IN4	PTE30		TPM0_CH3	TPM_CLKIN1			
23	19	-	_	PTE31	DISABLED		PTE31		TPM0_CH4				
24	20	15	-	PTE24	DISABLED		PTE24		TPM0_CH0		I2C0_SCL		
25	21	16	_	PTE25	DISABLED		PTE25		TPM0_CH1		I2C0_SDA		
26	22	17	10	PTA0	SWD_CLK	TSI0_CH1	PTA0		TPM0_CH5				SWD_CLK
27	23	18	11	PTA1	DISABLED	TSI0_CH2	PTA1	UART0_RX	TPM2_CH0				
28	24	19	12	PTA2	DISABLED	TSI0_CH3	PTA2	UART0_TX	TPM2_CH1				