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Understanding [Embedded - DSP \(Digital Signal Processors\)](#)

[Embedded - DSP \(Digital Signal Processors\)](#) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of [Embedded - DSP \(Digital Signal Processors\)](#)

Details

Product Status	Obsolete
Type	Fixed Point
Interface	Synchronous Serial Port (SSP)
Clock Rate	20MHz
Non-Volatile Memory	External
On-Chip RAM	1.5kB
Voltage - I/O	5.00V
Voltage - Core	5.00V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	68-LCC (J-Lead)
Supplier Device Package	68-PLCC (24.23x24.23)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-2104bpz-80

ADSP-2104/ADSP-2109

The ADSP-2109 is a memory-variant version of the ADSP-2104 and contains factory-programmed on-chip ROM program memory.

The ADSP-2109 eliminates the need for an external boot EPROM in your system, and can also eliminate the need for any external program memory by fitting the entire application program in on-chip ROM. This device provides an excellent option for volume applications where board space and system cost constraints are of critical concern.

Development Tools

The ADSP-2104/ADSP-2109 processors are supported by a complete set of tools for system development. The ADSP-2100 Family Development Software includes C and assembly language tools that allow programmers to write code for any ADSP-21xx processor. The ANSI C compiler generates ADSP-21xx assembly source code, while the runtime C library provides ANSI-standard and custom DSP library routines. The ADSP-21xx assembler produces object code modules which the linker combines into an executable file. The processor simulators provide an interactive instruction-level simulation with a reconfigurable,

windowed user interface. A PROM splitter utility generates PROM programmer compatible files.

EZ-ICE[®] in-circuit emulators allow debugging of ADSP-2104 systems by providing a full range of emulation functions such as modification of memory and register values and execution breakpoints. EZ-LAB[®] demonstration boards are complete DSP systems that execute EPROM-based programs.

The EZ-Kit Lite is a very low cost evaluation/development platform that contains both the hardware and software needed to evaluate the ADSP-21xx architecture.

Additional details and ordering information is available in the *ADSP-2100 Family Software & Hardware Development Tools* data sheet (ADDS-21xx-TOOLS). This data sheet can be requested from any Analog Devices sales office or distributor.

Additional Information

This data sheet provides a general overview of ADSP-2104/ADSP-2109 processor functionality. For detailed design information on the architecture and instruction set, refer to the *ADSP-2100 Family User's Manual*, available from Analog Devices.

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ADSP-2104/ADSP-2109

The ADSP-2104/ADSP-2109 can respond to several different interrupts. There can be up to three external interrupts, configured as edge- or level-sensitive. Internal interrupts can be generated by the timer and serial ports. There is also a master $\overline{\text{RESET}}$ signal.

Booting circuitry provides for loading on-chip program memory automatically from byte-wide external memory. After reset, three wait states are automatically generated. This allows, for example, the ADSP-2104 to use a 150 ns EPROM as external boot memory. Multiple programs can be selected and loaded from the EPROM with no additional hardware.

The data receive and transmit pins on SPORT1 (Serial Port 1) can be alternatively configured as a general-purpose input flag and output flag. You can use these pins for event signalling to and from an external device.

A programmable interval timer can generate periodic interrupts. A 16-bit count register (TCOUNT) is decremented every n cycles, where $n-1$ is a scaling value stored in an 8-bit register (TSCALE). When the value of the count register reaches zero, an interrupt is generated and the count register is reloaded from a 16-bit period register (TPERIOD).

Serial Ports

The ADSP-2104/ADSP-2109 processor includes two synchronous serial ports (“SPORTs”) for serial communications and multiprocessor communication.

The serial ports provide a complete synchronous serial interface with optional companding in hardware. A wide variety of framed or frameless data transmit and receive modes of operation are available. Each SPORT can generate an internal programmable serial clock or accept an external serial clock.

Each serial port has a 5-pin interface consisting of the following signals:

Signal Name	Function
SCLK	Serial Clock (I/O)
RFS	Receive Frame Synchronization (I/O)
TFS	Transmit Frame Synchronization (I/O)
DR	Serial Data Receive
DT	Serial Data Transmit

The serial ports offer the following capabilities:

Bidirectional—Each SPORT has a separate, double-buffered transmit and receive function.

Flexible Clocking—Each SPORT can use an external serial clock or generate its own clock internally.

Flexible Framing—The SPORTs have independent framing for the transmit and receive functions; each function can run in a frameless mode or with frame synchronization signals internally generated or externally generated; frame sync signals may be active high or inverted, with either of two pulse widths and timings.

Different Word Lengths—Each SPORT supports serial data word lengths from 3 to 16 bits.

Companding in Hardware—Each SPORT provides optional A-law and μ -law companding according to CCITT recommendation G.711.

Flexible Interrupt Scheme—Receive and transmit functions can generate a unique interrupt upon completion of a data word transfer.

Autobuffering with Single-Cycle Overhead—Each SPORT can automatically receive or transmit the contents of an entire circular data buffer with only one overhead cycle per data word; an interrupt is generated after the transfer of the entire buffer is completed.

Multichannel Capability (SPORT0 Only)—SPORT0 provides a multichannel interface to selectively receive or transmit a 24-word or 32-word, time-division multiplexed serial bit stream; this feature is especially useful for T1 or CEPT interfaces, or as a network communication scheme for multiple processors.

Alternate Configuration—SPORT1 can be alternatively configured as two external interrupt inputs ($\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$) and the Flag In and Flag Out signals (FI, FO).

Interrupts

The interrupt controller lets the processor respond to interrupts with a minimum of overhead. Up to three external interrupt input pins, $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, and $\overline{\text{IRQ2}}$, are provided. $\overline{\text{IRQ2}}$ is always available as a dedicated pin; $\overline{\text{IRQ1}}$ and $\overline{\text{IRQ0}}$ may be alternately configured as part of Serial Port 1. The ADSP-2104/ADSP-2109 also supports internal interrupts from the timer, and serial ports. The interrupts are internally prioritized and individually maskable (except for $\overline{\text{RESET}}$ which is nonmaskable). The $\overline{\text{IRQx}}$ input pins can be programmed for either level- or edge-sensitivity. The interrupt priorities are shown in Table I.

Table I. Interrupt Vector Addresses & Priority

ADSP-2104/ADSP-2109 Interrupt Source	Interrupt Vector Address
$\overline{\text{RESET}}$ Startup	0x0000
$\overline{\text{IRQ2}}$	0x0004 (<i>High Priority</i>)
SPORT0 Transmit	0x0008
SPORT0 Receive	0x000C
SPORT1 Transmit <i>or</i> $\overline{\text{IRQ1}}$	0x0010
SPORT1 Receive <i>or</i> $\overline{\text{IRQ0}}$	0x0014
Timer	0x0018 (<i>Low Priority</i>)

The ADSP-2104/ADSP-2109 uses a vectored interrupt scheme: when an interrupt is acknowledged, the processor shifts program control to the interrupt vector address corresponding to the interrupt received. Interrupts can be optionally nested so that a higher priority interrupt can preempt the currently executing interrupt service routine. Each interrupt vector location is four instructions in length so that simple service routines can be coded entirely in this space. Longer service routines require an additional JUMP or CALL instruction.

Individual interrupt requests are logically ANDed with the bits in the IMASK register; the highest-priority unmasked interrupt is then selected.

The interrupt control register, ICNTL, allows the external interrupts to be set as either edge- or level-sensitive. Depending on bit 4 in ICNTL, interrupt service routines can either be nested (with higher priority interrupts taking precedence) or be processed sequentially (with only one interrupt service active at a time).

The interrupt force and clear register, IFC, is a write-only register that contains a force bit and a clear bit for each interrupt.

When responding to an interrupt, the ASTAT, MSTAT, and IMASK status registers are pushed onto the status stack and the PC counter is loaded with the appropriate vector address. The status stack is seven levels deep to allow interrupt nesting. The stack is automatically popped when a return from the interrupt instruction is executed.

Pin Definitions

Table II shows pin definitions for the ADSP-2104/ADSP-2109 processors. Any inputs not used must be tied to V_{DD} .

SYSTEM INTERFACE

Figure 3 shows a typical system for the ADSP-2104/ADSP-2109, with two serial I/O devices, a boot EPROM, and optional external program and data memory. A total of 14.25K words of data memory and 14.5K words of program memory is addressable.

Programmable wait-state generation allows the processors to easily interface to slow external memories.

The ADSP-2104/ADSP-2109 also provides either: one external interrupt ($\overline{IRQ2}$) and two serial ports (SPORT0, SPORT1), or three external interrupts ($\overline{IRQ2}$, $\overline{IRQ1}$, $\overline{IRQ0}$) and one serial port (SPORT0).

Clock Signals

The ADSP-2104/ADSP-2109's CLKIN input may be driven by a crystal or by a TTL-compatible external clock signal. The CLKIN input may not be halted or changed in frequency during operation, nor operated below the specified low frequency limit.

If an external clock is used, it should be a TTL-compatible signal running at the instruction rate. The signal should be connected to the processor's CLKIN input; in this case, the XTAL input must be left unconnected.

Because the processor includes an on-chip oscillator circuit, an external crystal may also be used. The crystal should be connected across the CLKIN and XTAL pins, with two capacitors connected as shown in Figure 2. A parallel-resonant, fundamental frequency, microprocessor-grade crystal should be used.

Table II. ADSP-2104/ADSP-2109 Pin Definitions

Pin Name(s)	# of Pins	Input / Output	Function
Address	14	O	Address outputs for program, data and boot memory.
Data ¹	24	I/O	Data I/O pins for program and data memories. Input only for boot memory, with two MSBs used for boot memory addresses. Unused data lines may be left floating.
\overline{RESET}	1	I	Processor Reset Input
$\overline{IRQ2}$	1	I	External Interrupt Request #2
\overline{BR}^2	1	I	External Bus Request Input
\overline{BG}	1	O	External Bus Grant Output
\overline{PMS}	1	O	External Program Memory Select
\overline{DMS}	1	O	External Data Memory Select
\overline{BMS}	1	O	Boot Memory Select
\overline{RD}	1	O	External Memory Read Enable
\overline{WR}	1	O	External Memory Write Enable
MMAP	1	I	Memory Map Select Input
CLKIN, XTAL	2	I	External Clock or Quartz Crystal Input
CLKOUT	1	O	Processor Clock Output
V_{DD}			Power Supply Pins
GND			Ground Pins
SPORT0	5	I/O	Serial Port 0 Pins (<i>TFS0, RFS0, DT0, DR0, SCLK0</i>)
SPORT1	5	I/O	Serial Port 1 Pins (<i>TFS1, RFS1, DT1, DR1, SCLK1</i>)
<i>or Interrupts & Flags:</i>			
$\overline{IRQ0}$ (<i>RFS1</i>)	1	I	External Interrupt Request #0
$\overline{IRQ1}$ (<i>TFS1</i>)	1	I	External Interrupt Request #1
FI (<i>DR1</i>)	1	I	Flag Input Pin
FO (<i>DT1</i>)	1	O	Flag Output Pin

NOTES

¹Unused data bus lines may be left floating.

²BR must be tied high (to V_{DD}) if not used.

ADSP-2104/ADSP-2109

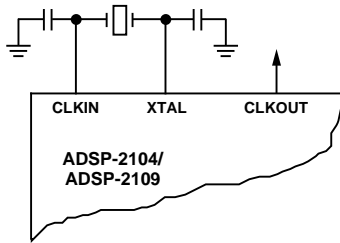


Figure 2. External Crystal Connections

A clock output signal (CLKOUT) is generated by the processor, synchronized to the processor's internal cycles.

Reset

The $\overline{\text{RESET}}$ signal initiates a complete reset of the processor. The $\overline{\text{RESET}}$ signal must be asserted when the chip is powered up to assure proper initialization. If the $\overline{\text{RESET}}$ signal is applied during initial power-up, it must be held long enough to allow the processor's internal clock to stabilize. If $\overline{\text{RESET}}$ is activated at any time after power-up and the input clock frequency does not change, the processor's internal clock continues and does not require this stabilization time.

The power-up sequence is defined as the total time required for the crystal oscillator circuit to stabilize after a valid V_{DD} is applied to the processor and for the internal phase-locked loop (PLL) to lock onto the specific crystal frequency. A minimum of 2000 t_{CK} cycles will ensure that the PLL has locked (this does not, however, include the crystal oscillator start-up time). During this power-up sequence the $\overline{\text{RESET}}$ signal should be held low. On any subsequent resets, the $\overline{\text{RESET}}$ signal must meet the minimum pulse width specification, t_{RSP} .

To generate the $\overline{\text{RESET}}$ signal, use either an RC circuit with an external Schmidt trigger or a commercially available reset IC. (Do not use only an RC circuit.)

The $\overline{\text{RESET}}$ input resets all internal stack pointers to the empty stack condition, masks all interrupts, and clears the MSTAT register. When $\overline{\text{RESET}}$ is released, the boot loading sequence is performed (provided there is no pending bus request and the chip is configured for booting, with $\text{MMAP} = 0$). The first instruction is then fetched from internal program memory location 0x0000.

Program Memory Interface

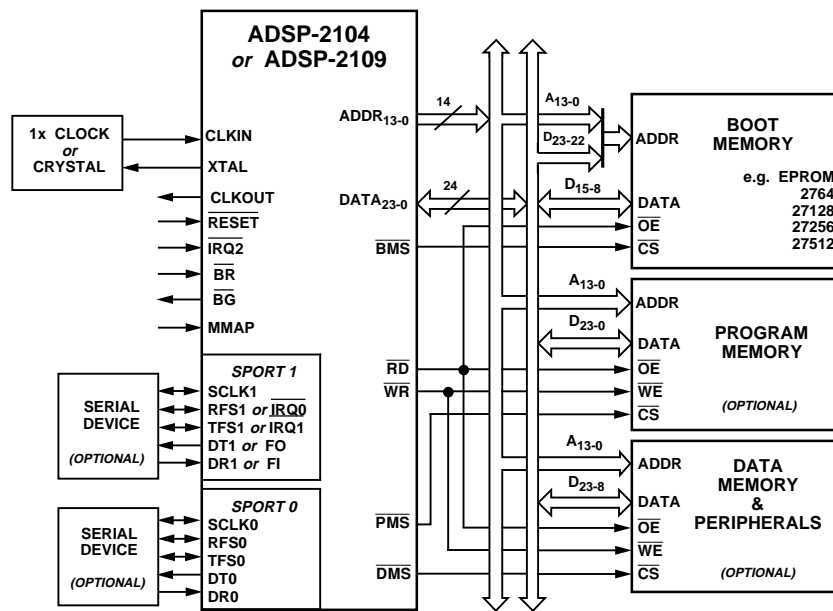
The on-chip program memory address bus (PMA) and on-chip program memory data bus (PMD) are multiplexed with the on-chip data memory buses (DMA, DMD), creating a single external data bus and a single external address bus. The external data bus is bidirectional and is 24 bits wide to allow instruction fetches from external program memory. Program memory may contain code and data.

The external address bus is 14 bits wide.

The data lines are bidirectional. The program memory select ($\overline{\text{PMS}}$) signal indicates accesses to program memory and can be used as a chip select signal. The write ($\overline{\text{WR}}$) signal indicates a write operation and is used as a write strobe. The read ($\overline{\text{RD}}$) signal indicates a read operation and is used as a read strobe or output enable signal.

The processor writes data from the 16-bit registers to 24-bit program memory using the PX register to provide the lower eight bits. When the processor reads 16-bit data from 24-bit program memory to a 16-bit data register, the lower eight bits are placed in the PX register.

The program memory interface can generate 0 to 7 wait states for external memory devices; default is to 7 wait states after $\overline{\text{RESET}}$.



THE TWO MSBs OF THE DATA BUS (D_{23-22}) ARE USED TO SUPPLY THE TWO MSBs OF THE BOOT MEMORY EPROM ADDRESS. THIS IS ONLY REQUIRED FOR THE 27256 AND 27512.

Figure 3. ADSP-2104/ADSP-2109 System

Program Memory Maps

Program memory can be mapped in two ways, depending on the state of the MMAP pin. Figure 4 shows the ADSP-2104 program memory maps. Figure 5 shows the program memory maps for the ADSP-2109.

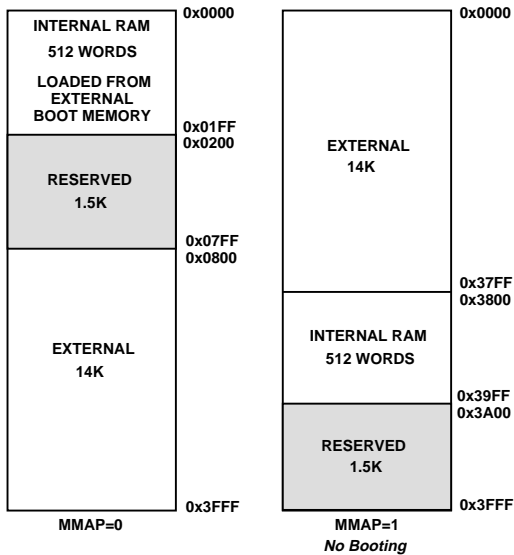


Figure 4. ADSP-2104 Program Memory Maps

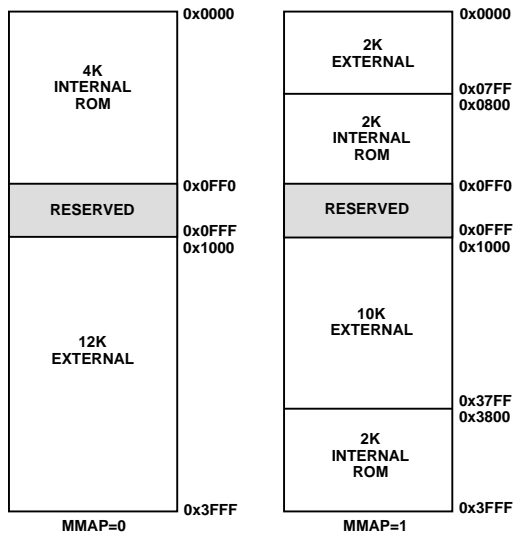


Figure 5. ADSP-2109 Program Memory Maps

ADSP-2104

When MMAP = 0, on-chip program memory RAM occupies 512 words beginning at address 0x0000. Off-chip program memory uses the remaining 14K words beginning at address 0x0800. In this configuration—when MMAP = 0—the boot loading sequence (described below in “Boot Memory Interface”) is automatically initiated when RESET is released.

When MMAP = 1, 14K words of off-chip program memory begin at address 0x0000 and on-chip program memory RAM is located in the 512 words between addresses 0x3800–0x39FF. In this configuration, program memory is not booted although it can be written to and read under program control.

Data Memory Interface

The data memory address bus (DMA) is 14 bits wide. The bidirectional external data bus is 24 bits wide, with the upper 16 bits used for data memory data (DMD) transfers.

The data memory select (\overline{DMS}) signal indicates access to data memory and can be used as a chip select signal. The write (\overline{WR}) signal indicates a write operation and can be used as a write strobe. The read (\overline{RD}) signal indicates a read operation and can be used as a read strobe or output enable signal.

The ADSP-2104/ADSP-2109 processors support memory-mapped I/O, with the peripherals memory-mapped into the data memory address space and accessed by the processor in the same manner as data memory.

Data Memory Map ADSP-2104

On-chip data memory RAM resides in the 256 words beginning at address 0x3800, also shown in Figure 6. Data memory locations from 0x3900 to the end of data memory at 0x3FFF are reserved. Control and status registers for the system, timer, wait-state configuration, and serial port operations are located in this region of memory.

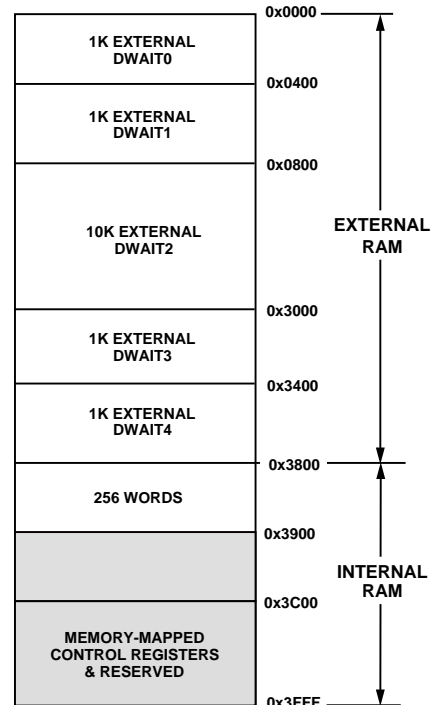


Figure 6. Data Memory Map

The remaining 14K of data memory is located off-chip. This external data memory is divided into five zones, each associated with its own wait-state generator. This allows slower peripherals to be memory-mapped into data memory for which wait states are specified. By mapping peripherals into different zones, you can accommodate peripherals with different wait-state requirements. All zones default to seven wait states after RESET.

ADSP-2109 Prototyping

You can prototype your ADSP-2109 system with the ADSP-2104 RAM-based processor. When code is fully developed and debugged, it can be submitted to Analog Devices for conversion into a ADSP-2109 ROM product.

The ADSP-2101 EZ-ICE emulator can be used for development of ADSP-2109 systems. For the 3.3 V ADSP-2109, a voltage converter interface board provides 3.3 V emulation.

Additional overlay memory is used for emulation of ADSP-2109 systems. It should be noted that due to the use of off-chip overlay memory to emulate the ADSP-2109, a performance loss may be experienced when both executing instructions and fetching program memory data from the off-chip overlay memory in the same cycle. This can be overcome by locating program memory data in on-chip memory.

Ordering Procedure for ADSP-2109 ROM Processor

To place an order for a custom ROM-coded ADSP-2109, you must:

1. Complete the following forms contained in the *ADSP ROM Ordering Package*, available from your Analog Devices sales representative:
 - ADSP-2109 ROM Specification Form
 - ROM Release Agreement
 - ROM NRE Agreement & Minimum Quantity Order (MQO)
 - Acceptance Agreement for Pre-Production ROM Products
2. Return the forms to Analog Devices along with two copies of the Memory Image File (.EXE file) of your ROM code. The files must be supplied on two 3.5" or 5.25" floppy disks for the IBM PC (DOS 2.01 or higher).
3. Place a purchase order with Analog Devices for nonrecurring engineering changes (NRE) associated with ROM product development.

After this information is received, it is entered into Analog Devices' ROM Manager System which assigns a custom ROM model number to the product. This model number will be branded on all prototype and production units manufactured to these specifications.

To minimize the risk of code being altered during this process, Analog Devices verifies that the .EXE files on both floppy disks are identical, and recalculates the checksums for the .EXE file entered into the ROM Manager System. The checksum data, in the form of a ROM Memory Map, a hard copy of the .EXE file, and a ROM Data Verification form are returned to you for inspection.

A signed ROM Verification Form and a purchase order for production units are required prior to any product being manufactured. Prototype units may be applied toward the minimum order quantity.

Upon completion of prototype manufacture, Analog Devices will ship prototype units and a delivery schedule update for production units. An invoice against your purchase order for the NRE charges is issued at this time.

There is a charge for each ROM mask generated and a minimum order quantity. Consult your sales representative for details. A separate order must be placed for parts of a specific package type, temperature range, and speed grade.

ADSP-2104/ADSP-2109

Instruction Set

The ADSP-2104/ADSP-2109 assembly language uses an algebraic syntax for ease of coding and readability. The sources and destinations of computations and data movements are written explicitly in each assembly statement, eliminating cryptic assembler mnemonics.

Every instruction assembles into a single 24-bit word and executes in a single cycle. The instructions encompass a wide variety of instruction types along with a high degree of

operational parallelism. There are five basic categories of instructions: data move instructions, computational instructions, multifunction instructions, program flow control instructions and miscellaneous instructions. Multifunction instructions perform one or two data moves and a computation.

The instruction set is summarized below. The *ADSP-2100 Family Users Manual* contains a complete reference to the instruction set.

ALU Instructions

[IF cond] AR AF = xop + yop [+ C];	<i>Add/Add with Carry</i>
= xop - yop [+ C - 1];	<i>Subtract X - Y/Subtract X - Y with Borrow</i>
= yop - xop [+ C - 1];	<i>Subtract Y - X/Subtract Y - X with Borrow</i>
= xop AND yop;	<i>AND</i>
= xop OR yop;	<i>OR</i>
= xop XOR yop;	<i>XOR</i>
= PASS xop;	<i>Pass, Clear</i>
= - xop;	<i>Negate</i>
= NOT xop;	<i>NOT</i>
= ABS xop;	<i>Absolute Value</i>
= yop + 1;	<i>Increment</i>
= yop - 1;	<i>Decrement</i>
= DIVS yop, xop;	<i>Divide</i>
= DIVQ xop;	

MAC Instructions

[IF cond] MR MF = xop * yop;	<i>Multiply</i>
= MR + xop * yop;	<i>Multiply/Accumulate</i>
= MR - xop * yop;	<i>Multiply/Subtract</i>
= MR;	<i>Transfer MR</i>
= 0;	<i>Clear</i>
IF MV SAT MR;	<i>Conditional MR Saturation</i>

Shifter Instructions

[IF cond] SR = [SR OR] ASHIFT xop;	<i>Arithmetic Shift</i>
[IF cond] SR = [SR OR] LSHIFT xop;	<i>Logical Shift</i>
SR = [SR OR] ASHIFT xop BY <exp>;	<i>Arithmetic Shift Immediate</i>
SR = [SR OR] LSHIFT xop BY <exp>;	<i>Logical Shift Immediate</i>
[IF cond] SE = EXP xop;	<i>Derive Exponent</i>
[IF cond] SB = EXPADJ xop;	<i>Block Exponent Adjust</i>
[IF cond] SR = [SR OR] NORM xop;	<i>Normalize</i>

Data Move Instructions

reg = reg;	<i>Register-to-Register Move</i>
reg = <data>;	<i>Load Register Immediate</i>
reg = DM (<addr>;	<i>Data Memory Read (Direct Address)</i>
dreg = DM (Ix, My);	<i>Data Memory Read (Indirect Address)</i>
dreg = PM (Ix, My);	<i>Program Memory Read (Indirect Address)</i>
DM (<addr>) = reg;	<i>Data Memory Write (Direct Address)</i>
DM (Ix, My) = dreg;	<i>Data Memory Write (Indirect Address)</i>
PM (Ix, My) = dreg;	<i>Program Memory Write (Indirect Address)</i>

Multifunction Instructions

<ALU> <MAC> <SHIFT>, dreg = dreg;	<i>Computation with Register-to-Register Move</i>
<ALU> <MAC> <SHIFT>, dreg = DM (Ix, My);	<i>Computation with Memory Read</i>
<ALU> <MAC> <SHIFT>, dreg = PM (Ix, My);	<i>Computation with Memory Read</i>
DM (Ix, My) = dreg, <ALU> <MAC> <SHIFT>;	<i>Computation with Memory Write</i>
PM (Ix, My) = dreg, <ALU> <MAC> <SHIFT>;	<i>Computation with Memory Write</i>
dreg = DM (Ix, My), dreg = PM (Ix, My);	<i>Data & Program Memory Read</i>
<ALU> <MAC>, dreg = DM (Ix, My), dreg = PM (Ix, My);	<i>ALU/MAC with Data & Program Memory Read</i>

ADSP-2104/ADSP-2109—SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter	K Grade		Unit
	Min	Max	
V _{DD} Supply Voltage	4.50	5.50	V
T _{AMB} Ambient Operating Temperature	0	+70	°C

See “Environmental Conditions” for information on thermal specifications.

ELECTRICAL CHARACTERISTICS

Parameter	Test Conditions	Min	Max	Unit
V _{IH} Hi-Level Input Voltage ^{3, 5}	@ V _{DD} = max	2.0		V
V _{IH} Hi-Level CLKIN Voltage	@ V _{DD} = max	2.2		V
V _{IL} Lo-Level Input Voltage ^{1, 3}	@ V _{DD} = min		0.8	V
V _{OH} Hi-Level Output Voltage ^{2, 3, 7}	@ V _{DD} = min, I _{OH} = -0.5 mA	2.4		V
	@ V _{DD} = min, I _{OH} = -100 μA ⁸	V _{DD} - 0.3		V
V _{OL} Lo-Level Output Voltage ^{2, 3, 7}	@ V _{DD} = min, I _{OL} = 2 mA		0.4	V
I _{IH} Hi-Level Input Current ¹	@ V _{DD} = max, V _{IN} = V _{DD} max		10	μA
I _{IL} Lo-Level Input Current ¹	@ V _{DD} = max, V _{IN} = 0 V		10	μA
I _{OZH} Three-State Leakage Current ⁴	@ V _{DD} = max, V _{IN} = V _{DD} max ⁶		10	μA
I _{OZL} Three-State Leakage Current ⁴	@ V _{DD} = max, V _{IN} = 0 V ⁶		10	μA
C _I Input Pin Capacitance ^{1, 8, 9}	@ V _{IN} = 2.5 V, f _{IN} = 1.0 MHz, T _{AMB} = 25°C		8	pF
C _O Output Pin Capacitance ^{4, 8, 9, 10}	@ V _{IN} = 2.5 V, f _{IN} = 1.0 MHz, T _{AMB} = 25°C		8	pF

NOTES

¹Input-only pins: CLKIN, RESET, IRQ2, BR, MMAP, DR1, DR0.

²Output pins: BG, PMS, DMS, BMS, RD, WR, A0-A13, CLKOUT, DT1, DT0.

³Bidirectional pins: D0-D23, SCLK1, RFS1, TFS1, SCLK0, RFS0, TFS0.

⁴Three-state pins: A0-A13, D0-D23, PMS, DMS, BMS, RD, WR, DT1, SCLK1, RSF1, TFS1, DT0, SCLK0, RFS0, TFS0.

⁵Input-only pins: RESET, IRQ2, BR, MMAP, DR1, DR0.

⁶0 V on BR, CLKIN Active (to force three-state condition).

⁷Although specified for TTL outputs, all ADSP-2104/ADSP-2109 outputs are CMOS-compatible and will drive to V_{DD} and GND, assuming no dc loads.

⁸Guaranteed but not tested.

⁹Applies to PGA, PLCC, PQFP package types.

¹⁰Output pin capacitance is the capacitive load for any three-stated output pin.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage	-0.3 V to +7 V
Input Voltage	-0.3 V to V _{DD} + 0.3 V
Output Voltage Swing	-0.3 V to V _{DD} + 0.3 V
Operating Temperature Range (Ambient)	-55°C to +125°C
Storage Temperature Range	-65°C to +125°C
Lead Temperature (10 sec) PGA	+300°C
Lead Temperature (5 sec) PLCC, PQFP, TQFP	+280°C

*Stresses greater than those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADSP-2104/ADSP-2109 processor features proprietary ESD protection circuitry to dissipate high energy electrostatic discharges (Human Body Model), permanent damage may occur to devices subjected to such discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Unused devices must be stored in conductive foam or shunts, and the foam should be discharged to the destination socket before the devices are removed. Per method 3015 of MIL-STD-883, the ADSP-2104/ADSP-2109 processor has been classified as Class 1 device.



SPECIFICATIONS (ADSP-2104/ADSP-2109)

SUPPLY CURRENT & POWER

Parameter	Test Conditions	Min	Max	Unit
I_{DD} Supply Current (Dynamic) ¹	@ $V_{DD} = \text{max}$, $t_{CK} = 50 \text{ ns}^2$		31	mA
I_{DD} Supply Current (Idle) ^{1, 3}	@ $V_{DD} = \text{max}$, $t_{CK} = 72.3 \text{ ns}^2$		24	mA
	@ $V_{DD} = \text{max}$, $t_{CK} = 50 \text{ ns}$		11	mA
	@ $V_{DD} = \text{max}$, $t_{CK} = 72.3 \text{ ns}$		10	mA

NOTES

¹Current reflects device operating with no output loads.

² $V_{IN} = 0.4 \text{ V}$ and 2.4 V .

³Idle refers to ADSP-2104/ADSP-2109 state of operation during execution of IDLE instruction. Deasserted pins are driven to either V_{DD} or GND.

For typical supply current (internal power dissipation) figures, see Figure 7.

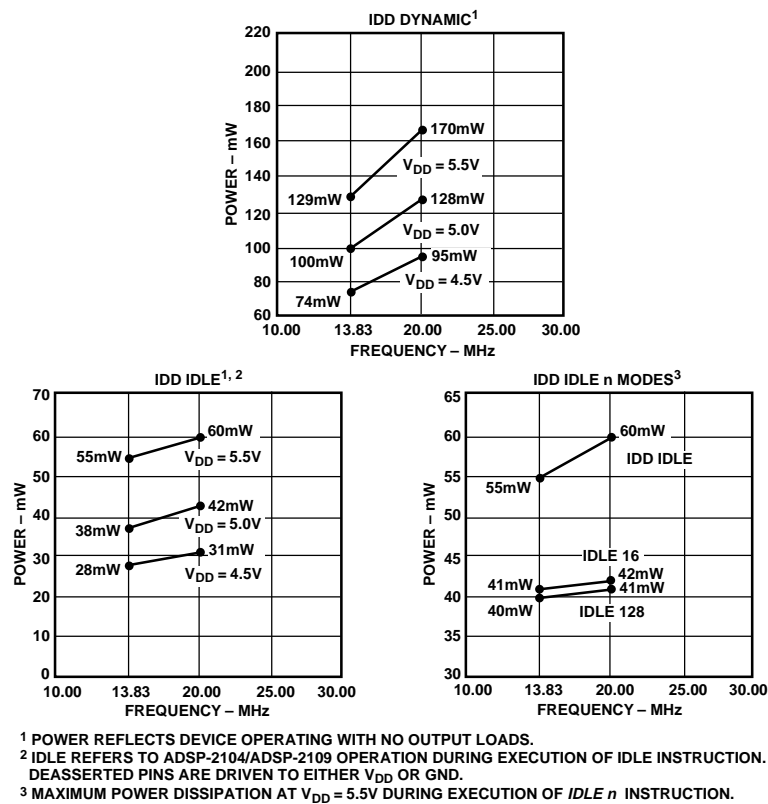


Figure 7. ADSP-2104/ADSP-2109 Power (Typical) vs. Frequency

SPECIFICATIONS (ADSP-2104/ADSP-2109)

TEST CONDITIONS

Figure 10 shows voltage reference levels for ac measurements.

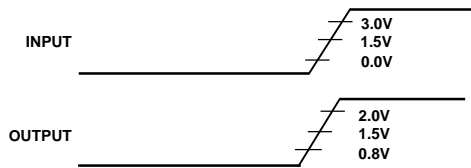


Figure 10. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Disable Time

Output pins are considered to be disabled when they have stopped driving and started a transition from the measured output high or low voltage to a high impedance state. The output disable time (t_{DIS}) is the difference of $t_{MEASURED}$ and t_{DECAY} , as shown in Figure 11. The time $t_{MEASURED}$ is the interval from when a reference signal reaches a high or low voltage level to when the output voltages have changed by 0.5 V from the measured output high or low voltage.

The decay time, t_{DECAY} , is dependent on the capacitive load, C_L , and the current load, i_L , on the output pin. It can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L \times 0.5 V}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. If multiple pins (such as the data bus) are disabled, the measurement value is that of the last pin to stop driving.

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high-impedance state to when they start driving. The output enable time (t_{ENA}) is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in Figure 11. If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

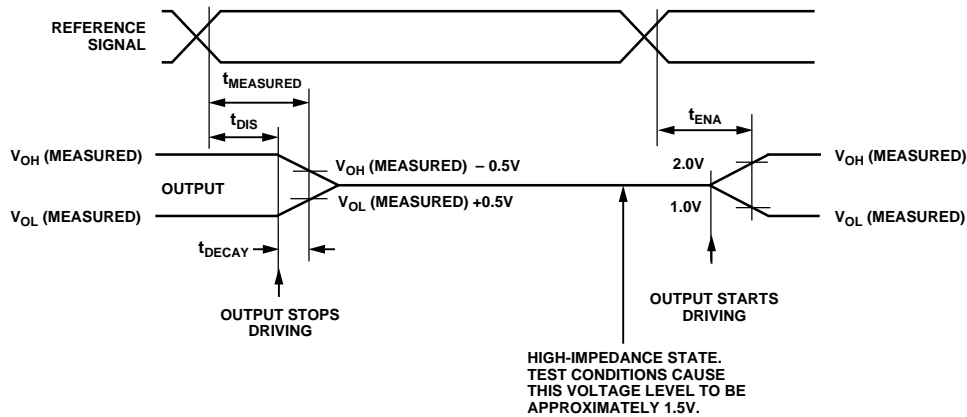


Figure 11. Output Enable/Disable

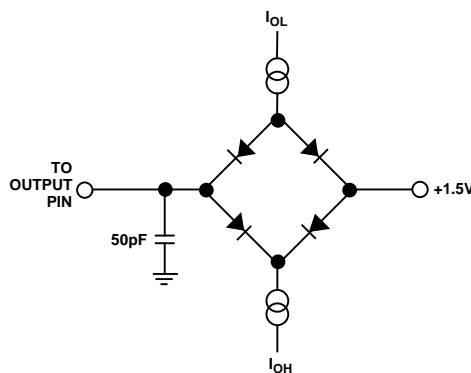


Figure 12. Equivalent Device Loading for AC Measurements (Except Output Enable/Disable)

ADSP-2104L/ADSP-2109L—SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter		K Grade		Unit
		Min	Max	
V _{DD}	Supply Voltage	3.00	3.60	V
T _{AMB}	Ambient Operating Temperature	0	+70	°C

See “Environmental Conditions” for information on thermal specifications.

ELECTRICAL CHARACTERISTICS

Parameter	Test Conditions	Min	Max	Unit
V _{IH}	Hi-Level Input Voltage ^{1, 3}	@ V _{DD} = max	2.0	V
V _{IL}	Lo-Level Input Voltage ^{1, 3}	@ V _{DD} = min		V
V _{OH}	Hi-Level Output Voltage ^{2, 3, 6}	@ V _{DD} = min, I _{OH} = -0.5 mA ⁶	2.4	V
V _{OL}	Lo-Level Output Voltage ^{2, 3, 6}	@ V _{DD} = min, I _{OL} = 2 mA ⁶		V
I _{IH}	Hi-Level Input Current ¹	@ V _{DD} = max, V _{IN} = V _{DD} max	10	μA
I _{IL}	Lo-Level Input Current ¹	@ V _{DD} = max, V _{IN} = 0 V	10	μA
I _{OZH}	Three-State Leakage Current ⁴	@ V _{DD} = max, V _{IN} = V _{DD} max ⁵	10	μA
I _{OZL}	Three-State Leakage Current ⁴	@ V _{DD} = max, V _{IN} = 0 V ⁵	10	μA
C _I	Input Pin Capacitance ^{1, 7, 8}	@ V _{IN} = 2.5 V, f _{IN} = 1.0 MHz, T _{AMB} = 25°C	8	pF
C _O	Output Pin Capacitance ^{4, 7, 8, 9}	@ V _{IN} = 2.5 V, f _{IN} = 1.0 MHz, T _{AMB} = 25°C	8	pF

NOTES

¹Input-only pins: CLKIN, $\overline{\text{RESET}}$, $\overline{\text{IRQ2}}$, $\overline{\text{BR}}$, MMAP, DR1, DR0.

²Output pins: BG, PMS, DMS, BMS, RD, WR, A0–A13, CLKOUT, DT1, DT0.

³Bidirectional pins: D0–D23, SCLK1, RFS1, TFS1, SCLK0, RFS0, TFS0.

⁴Three-stateable pins: A0–A13, D0–D23, PMS, DMS, BMS, RD, WR, DT1, SCLK1, RSF1, TFS1, DT0, SCLK0, RFS0, TFS0.

⁵0 V on $\overline{\text{BR}}$, CLKIN Active (to force three-state condition).

⁶All outputs are CMOS and will drive to V_{DD} and GND with no dc loads.

⁷Guaranteed but not tested.

⁸Applies to PLCC package type.

⁹Output pin capacitance is the capacitive load for any three-stated output pin.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage	–0.3 V to +4.5 V
Input Voltage	–0.3 V to V _{DD} + 0.3 V
Output Voltage Swing	–0.3 V to V _{DD} + 0.3 V
Operating Temperature Range (Ambient)	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (5 sec) PLCC	+280°C

*Stresses greater than those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ADSP-2104/ADSP-2109

SPECIFICATIONS (ADSP-2104L/ADSP-2109L)

POWER DISSIPATION EXAMPLE

To determine total power dissipation in a specific application, the following equation should be applied for each output:

$$C \times V_{DD}^2 \times f$$

C = load capacitance, f = output switching frequency.

Example:

In an ADSP-2104L application where external data memory is used and no other outputs are active, power dissipation is calculated as follows:

Assumptions:

- External data memory is accessed every cycle with 50% of the address pins switching.
- External data memory writes occur every other cycle with 50% of the data pins switching.
- Each address and data pin has a 10 pF total load at the pin.
- The application operates at $V_{DD} = 3.3$ V and $t_{CK} = 100$ ns.

$$\text{Total Power Dissipation} = P_{INT} + (C \times V_{DD}^2 \times f)$$

P_{INT} = internal power dissipation (from Figure 13).

$(C \times V_{DD}^2 \times f)$ is calculated for each output:

Output	# of Pins	$\times C$	$\times V_{DD}^2$	$\times f$
Address, \overline{DMS}	8	$\times 10$ pF	$\times 3.3^2$ V	$\times 10$ MHz = 8.71 mW
Data, \overline{WR}	9	$\times 10$ pF	$\times 3.3^2$ V	$\times 5$ MHz = 4.90 mW
\overline{RD}	1	$\times 10$ pF	$\times 3.3^2$ V	$\times 5$ MHz = 0.55 mW
CLKOUT	1	$\times 10$ pF	$\times 3.3^2$ V	$\times 10$ MHz = 1.09 mW

15.25 mW

Total power dissipation for this example = $P_{INT} + 15.25$ mW.

ENVIRONMENTAL CONDITIONS

Ambient Temperature Rating:

$$T_{AMB} = T_{CASE} - (PD \times \theta_{CA})$$

T_{CASE} = Case Temperature in °C

PD = Power Dissipation in W

θ_{CA} = Thermal Resistance (Case-to-Ambient)

θ_{JA} = Thermal Resistance (Junction-to-Ambient)

θ_{JC} = Thermal Resistance (Junction-to-Case)

Package	θ_{JA}	θ_{JC}	θ_{CA}
PLCC	27°C/W	16°C/W	11°C/W

CAPACITIVE LOADING

Figures 14 and 15 show capacitive loading characteristics.

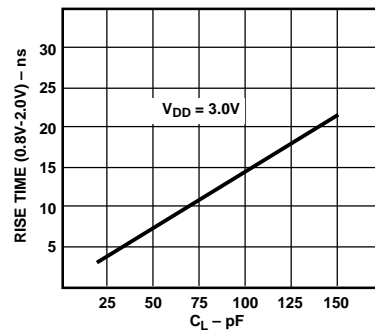


Figure 14. Typical Output Rise Time vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

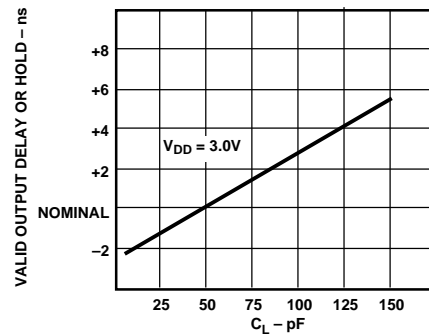


Figure 15. Typical Output Valid Delay or Hold vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

ADSP-2104/ADSP-2109

TIMING PARAMETERS (ADSP-2104/ADSP-2109)

GENERAL NOTES

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, you cannot meaningfully add parameters to derive longer times.

TIMING NOTES

Switching characteristics specify how the processor changes its signals. You have no control over this timing—circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics tell you what the processor will do in a given circumstance. You can also use

switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

MEMORY REQUIREMENTS

The table below shows common memory device specifications and the corresponding ADSP-2104/ADSP-2109 timing parameters, for your convenience.

Memory Device Specification	ADSP-2104/ADSP-2109 Timing Parameter	Timing Parameter Definition
Address Setup to Write Start	t_{ASW}	A0–A13, \overline{DMS} , \overline{PMS} Setup before \overline{WR} Low
Address Setup to Write End	t_{AW}	A0–A13, \overline{DMS} , \overline{PMS} Setup before \overline{WR} Deasserted
Address Hold Time	t_{WRA}	A0–A13, \overline{DMS} , \overline{PMS} Hold after \overline{WR} Deasserted
Data Setup Time	t_{DW}	Data Setup before \overline{WR} High
Data Hold Time	t_{DH}	Data Hold after \overline{WR} High
\overline{OE} to Data Valid	t_{RDD}	\overline{RD} Low to Data Valid
Address Access Time	t_{AA}	A0–A13, \overline{DMS} , \overline{PMS} , \overline{BMS} to Data Valid

TIMING PARAMETERS (ADSP-2104/ADSP-2109)
CLOCK SIGNALS & RESET

Parameter	20 MHz		Frequency Dependency		Unit
	Min	Max	Min	Max	
<i>Timing Requirement:</i>					
t_{CK} CLKIN Period	50	150			ns
t_{CKL} CLKIN Width Low	20		20		ns
t_{CKH} CLKIN Width High	20		20		ns
t_{RSP} RESET Width Low	250		$5t_{CK}^1$		ns
<i>Switching Characteristic:</i>					
t_{CPL} CLKOUT Width Low	15		$0.5t_{CK} - 10$		ns
t_{CPH} CLKOUT Width High	15		$0.5t_{CK} - 10$		ns
t_{CKOH} CLKIN High to CLKOUT High	0	20			ns

NOTE

¹Applies after powerup sequence is complete. Internal phase lock loop requires no more than 2000 CLKIN cycles, assuming stable CLKIN (not including crystal oscillator startup time).

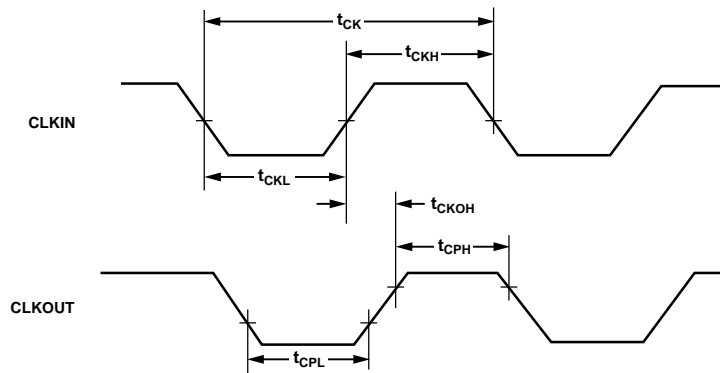


Figure 19. Clock Signals

ADSP-2104/ADSP-2109

TIMING PARAMETERS (ADSP-2104/ADSP-2109)

MEMORY READ

Parameter	20 MHz		Unit
	Min	Max	
<i>Timing Requirement:</i>			
t_{RDD}	RD Low to Data Valid		ns
t_{AA}	A0–A13, \overline{PMS} , \overline{DMS} , \overline{BMS} to Data Valid		ns
t_{RDH}	Data Hold from \overline{RD} High		0
<i>Switching Characteristic:</i>			
t_{RP}	RD Pulse Width		ns
t_{CRD}	CLKOUT High to \overline{RD} Low		ns
t_{ASR}	A0–A13, \overline{PMS} , \overline{DMS} , \overline{BMS} Setup before \overline{RD} Low		ns
t_{RDA}	A0–A13, \overline{PMS} , \overline{DMS} , \overline{BMS} Hold after \overline{RD} Deasserted		ns
t_{RWR}	RD High to \overline{RD} or \overline{WR} Low		ns

Parameter	Frequency Dependency (CLKIN ≤ 20 MHz)		Unit
	Min	Max	
<i>Timing Requirement:</i>			
t_{RDD}	RD Low to Data Valid		ns
t_{AA}	A0–A13, \overline{PMS} , \overline{DMS} , \overline{BMS} to Data Valid		ns
t_{RDH}	Data Hold from \overline{RD} High		0
<i>Switching Characteristic:</i>			
t_{RP}	RD Pulse Width		ns
t_{CRD}	CLKOUT High to \overline{RD} Low		ns
t_{ASR}	A0–A13, \overline{PMS} , \overline{DMS} , \overline{BMS} Setup before \overline{RD} Low		ns
t_{RDA}	A0–A13, \overline{PMS} , \overline{DMS} , \overline{BMS} Hold after \overline{RD} Deasserted		ns
t_{RWR}	RD High to \overline{RD} or \overline{WR} Low		ns

NOTE
w = wait states × t_{CK} .

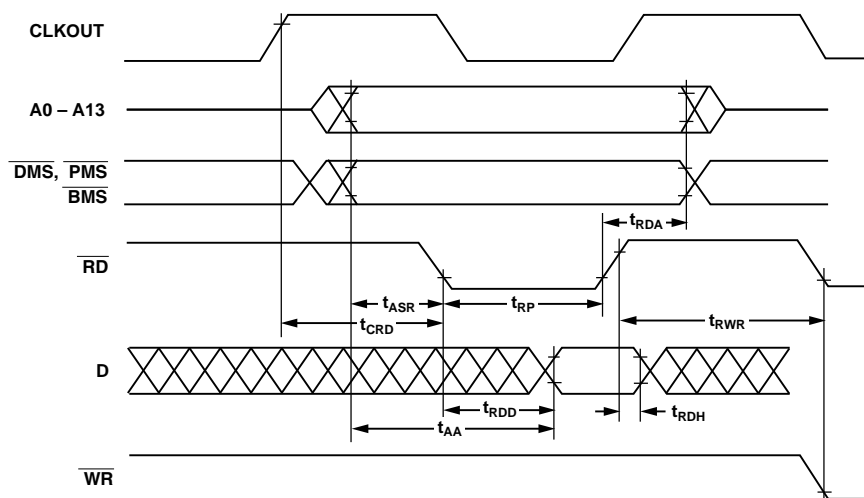


Figure 22. Memory Read

ADSP-2104/ADSP-2109

TIMING PARAMETERS (ADSP-2104/ADSP-2109)

SERIAL PORTS

Parameter	13.824 MHz*		Frequency Dependency		Unit
	Min	Max	Min	Max	
<i>Timing Requirement:</i>					
t_{SCK} SCLK Period	72.3				ns
t_{SCS} DR/TFS/RFS Setup before SCLK Low	8				ns
t_{SCH} DR/TFS/RFS Hold after SCLK Low	10				ns
t_{SCP} SCLK _{IN} Width	28				ns
<i>Switching Characteristic:</i>					
t_{CC} CLKOUT High to SCLK _{OUT}	18.1	33.1	$0.25t_{CK}$	$0.25t_{CK} + 15$	ns
t_{SCDE} SCLK High to DT Enable	0				ns
t_{SCDV} SCLK High to DT Valid		20			ns
t_{RH} TFS/RFS _{OUT} Hold after SCLK High					ns
t_{RD} TFS/RFS _{OUT} Delay from SCLK High		20			ns </td
t_{SCDH} DT Hold after SCLK High					ns
t_{TDE} TFS (Alt) to DT Enable					ns
t_{TDV} TFS (Alt) to DT Valid		18			ns
t_{SCDD} SCLK High to DT Disable		25			ns
t_{RDV} RFS (Multichannel, Frame Delay Zero) to DT Valid		20			ns

*Maximum serial port operating frequency is 13.824 MHz.

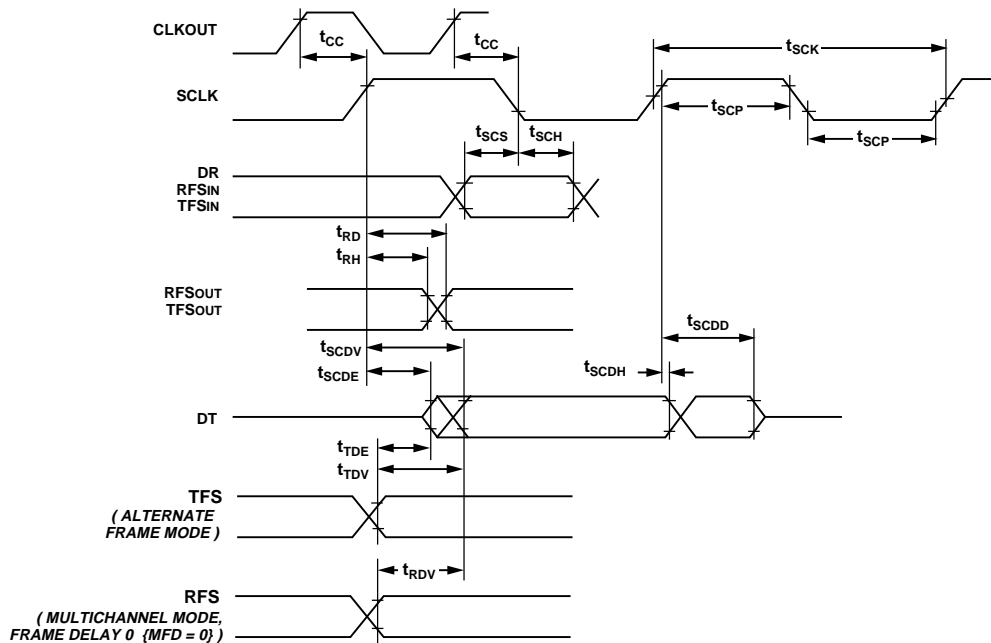


Figure 24. Serial Ports

ADSP-2104/ADSP-2109

TIMING PARAMETERS (ADSP-2104L/ADSP-2109L)

CLOCK SIGNALS & RESET

Parameter	13.824 MHz		Frequency Dependency		Unit
	Min	Max	Min	Max	
<i>Timing Requirement:</i>					
t_{CK} CLKIN Period	72.3	150			ns
t_{CKL} CLKIN Width Low	20		20		ns
t_{CKH} CLKIN Width High	20		20		ns
t_{RSP} RESET Width Low	361.5		$5t_{CK}^1$		ns
<i>Switching Characteristic:</i>					
t_{CPL} CLKOUT Width Low	26.2		$0.5t_{CK} - 10$		ns
t_{CPH} CLKOUT Width High	26.2		$0.5t_{CK} - 10$		ns
t_{CKOH} CLKIN High to CLKOUT High	0	20			ns

NOTE

¹Applies after powerup sequence is complete. Internal phase lock loop requires no more than 2000 CLKIN cycles assuming stable CLKIN (not including crystal oscillator startup time).

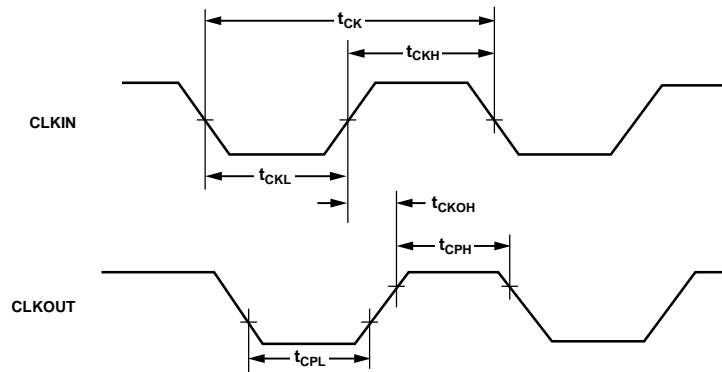


Figure 25. Clock Signals

ADSP-2104/ADSP-2109

TIMING PARAMETERS (ADSP-2104L/ADSP-2109L)

BUS REQUEST/GRANT

Parameter	13.824 MHz		Frequency Dependency		Unit
	Min	Max	Min	Max	
<i>Timing Requirement:</i>					
t_{BH}	BR Hold after CLKOUT High ¹		0.25 $t_{CK} + 5$		ns
t_{BS}	BR Setup before CLKOUT Low ¹		0.25 $t_{CK} + 20$		ns
<i>Switching Characteristic:</i>					
t_{SD}	CLKOUT High to \overline{DMS} , \overline{PMS} , \overline{BMS} , \overline{RD} , \overline{WR} Disable		38.1		ns
t_{SDB}	\overline{DMS} , \overline{PMS} , \overline{BMS} , \overline{RD} , \overline{WR} Disable to \overline{BG} Low		0		ns
t_{SE}	\overline{BG} High to \overline{DMS} , \overline{PMS} , \overline{BMS} , \overline{RD} , \overline{WR} Enable		0		ns
t_{SEC}	\overline{DMS} , \overline{PMS} , \overline{BMS} , \overline{RD} , \overline{WR} Enable to CLKOUT High		0.25 $t_{CK} - 10$		ns

NOTES

¹If \overline{BR} meets the t_{BS} and t_{BH} setup/hold requirements, it will be recognized in the current processor cycle; otherwise it is recognized in the following cycle. \overline{BR} requires a pulse width greater than 10 ns.

Note: \overline{BG} is asserted in the cycle after \overline{BR} is recognized. No external synchronization circuit is needed when \overline{BR} is generated as an asynchronous signal.

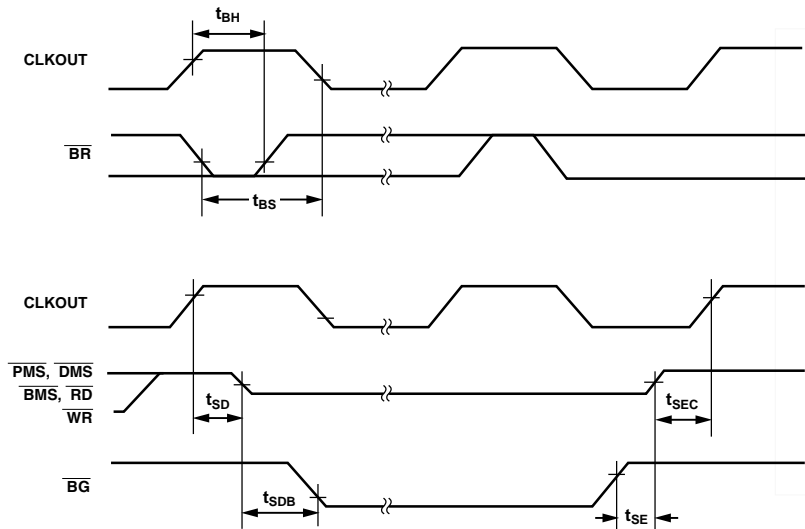
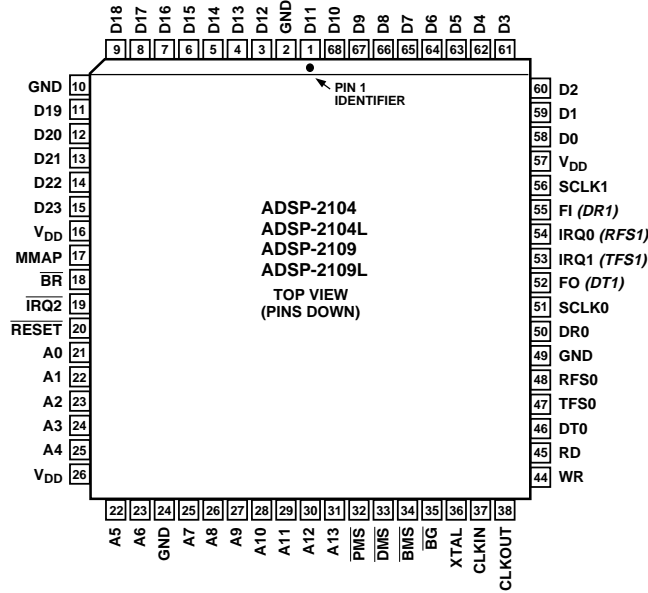


Figure 27. Bus Request/Grant

ADSP-2104/ADSP-2109

PIN CONFIGURATIONS

68-Lead PLCC



PLCC Number	Pin Name
1	D11
2	GND
3	D12
4	D13
5	D14
6	D15
7	D16
8	D17
9	D18
10	GND
11	D19
12	D20
13	D21
14	D22
15	D23
16	V _{DD}
17	MMAP

PLCC Number	Pin Name
18	$\overline{\text{BR}}$
19	$\overline{\text{IRQ2}}$
20	$\overline{\text{RESET}}$
21	A0
22	A1
23	A2
24	A3
25	A4
26	V _{DD}
27	A5
28	A6
29	GND
30	A7
31	A8
32	A9
33	A10
34	A11

PLCC Number	Pin Name
35	A12
36	A13
37	PMS
38	DMS
39	BMS
40	BG
41	XTAL
42	CLKIN
43	CLKOUT
44	$\overline{\text{WR}}$
45	$\overline{\text{RD}}$
46	DT0
47	TFS0
48	RFS0
49	GND
50	DR0
51	SCLK0

PLCC Number	Pin Name
52	FO (DT1)
53	$\overline{\text{IRQ1}}$ (TFS1)
54	$\overline{\text{IRQ0}}$ (RFS1)
55	FI (DR1)
56	SCLK1
57	V _{DD}
58	D0
59	D1
60	D2
61	D3
62	D4
63	D5
64	D6
65	D7
66	D8
67	D9
68	D10

ADSP-2104/ADSP-2109

ORDERING GUIDE

Part Number*	Ambient Temperature Range	Instruction Rate	Package Description	Package Option
ADSP-2104KP-80	0°C to +70°C	20.0 MHz	68-Lead PLCC	P-68A
ADSP-2109KP-80	0°C to +70°C	20.0 MHz	68-Lead PLCC	P-68A
ADSP-2104LKP-55	0°C to +70°C	13.824 MHz	68-Lead PLCC	P-68A
ADSP-2109LKP-55	0°C to +70°C	13.824 MHz	68-Lead PLCC	P-68A

*K = Commercial Temperature Range (0°C to +70°C).
P = PLCC (Plastic Leaded Chip Carrier).

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