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Details	
Product Status	Obsolete
Core Processor	eZ80
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	24
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/ez80f92az020sc00tr

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Table 1. 100-Pin LQFP Pin Identification of the eZ80F92 Device (Continued)

Pin No	Symbol	Function	Signal Direction	Description
82	PC6	GPIO Port C	Bidirectional	This pin can be used for general-purpose I/O. It can be individually programmed as input or output and can also be used individually as an interrupt input. Each Port C pin, when programmed as output, can be selected to be an open-drain or open-source output. Port C is multiplexed with one UART.
	$\overline{DCD1}$	Data Carrier Detect	Input, Active Low	Modem status signal to the UART. This signal is multiplexed with PC6.
83	PC7	GPIO Port C	Bidirectional	This pin can be used for general-purpose I/O. It can be individually programmed as input or output and can also be used individually as an interrupt input. Each Port C pin, when programmed as output, can be selected to be an open-drain or open-source output. Port C is multiplexed with one UART.
	$\overline{RI1}$	Ring Indicator	Input, Active Low	Modem status signal to the UART. This signal is multiplexed with PC7.
84	V_{SS}	Ground		Ground.
85	X_{IN}	System Clock Oscillator Input	Input	This pin is the input to the onboard crystal oscillator for the primary system clock. If an external oscillator is used, its clock output should be connected to this pin. When a crystal is used, it should be connected between X_{IN} and X_{OUT}.
86	X_{OUT}	System Clock Oscillator Output	Output	This pin is the output of the onboard crystal oscillator. When used, a crystal should be connected between X_{IN} and X_{OUT}.
87	V_{DD}	Power Supply		Power Supply.

Table 1. 100-Pin LQFP Pin Identification of the eZ80F92 Device (Continued)

Pin No	Symbol	Function	Signal Direction	Description
96	V_{DD}	Power Supply		Power Supply.
97	V_{SS}	Ground		Ground.
98	SDA	I^2C Serial Data	Bidirectional	This pin carries the I^2C data signal.
99	SCL	I^2C Serial Clock	Bidirectional	This pin is used to receive and transmit the I^2C clock.
100	PHI	System Clock	Output	This pin is an output driven by the internal system clock.

Pin Characteristics

Table 2 lists the characteristics of each pin in the eZ80F92 device's 100-pin LQFP package.

Table 2. Pin Characteristics of the eZ80F92 Device

Pin No	Symbol	Direction	Reset Direction	Active Low/High	Tristate Output	Pull Up/Down	Schmitt Trigger Input	Open Drain/ Source
1	ADDR0	I/O	O	N/A	Yes	No	No	No
2	ADDR1	I/O	O	N/A	Yes	No	No	No
3	ADDR2	I/O	O	N/A	Yes	No	No	No
4	ADDR3	I/O	O	N/A	Yes	No	No	No
5	ADDR4	I/O	O	N/A	Yes	No	No	No
6	ADDR5	I/O	O	N/A	Yes	No	No	No
7	V_{DD}							
8	V_{SS}							
9	ADDR6	I/O	O	N/A	Yes	No	No	No
10	ADDR7	I/O	O	N/A	Yes	No	No	No
11	ADDR8	I/O	O	N/A	Yes	No	No	No
12	ADDR9	I/O	O	N/A	Yes	No	No	No
13	ADDR10	I/O	O	N/A	Yes	No	No	No
14	ADDR11	I/O	O	N/A	Yes	No	No	No
15	ADDR12	I/O	O	N/A	Yes	No	No	No

Table 2. Pin Characteristics of the eZ80F92 Device (Continued)

Pin No	Symbol	Direction	Reset Direction	Active Low/High	Tristate Output	Pull Up/Down	Schmitt Trigger Input	Open Drain/ Source
99	SCL	I/O	I	N/A	Yes	Up	No	OD
100	PHI	O	O	N/A	Yes	No	No	No

Note: I = Input, O = Output, I/O = Input and Output, U = Undefined.

Table 3. Register Map (Continued)

Address (hex)	Mnemonic	Name	Reset (hex)	CPU Access	Page No
00A4	PD_ALT1	Port D Alternate Register 1	00	R/W	44
00A5	PD_ALT2	Port D Alternate Register 2	00	R/W	44
Chip Select/Wait State Generator					
00A8	CS0_LBR	Chip Select 0 Lower Bound Register	00	R/W	67
00A9	CS0_UBR	Chip Select 0 Upper Bound Register	FF	R/W	68
00AA	CS0_CTL	Chip Select 0 Control Register	E8	R/W	69
00AB	CS1_LBR	Chip Select 1 Lower Bound Register	00	R/W	67
00AC	CS1_UBR	Chip Select 1 Upper Bound Register	00	R/W	68
00AD	CS1_CTL	Chip Select 1 Control Register	00	R/W	69
00AE	CS2_LBR	Chip Select 2 Lower Bound Register	00	R/W	67
00AF	CS2_UBR	Chip Select 2 Upper Bound Register	00	R/W	68
00B0	CS2_CTL	Chip Select 2 Control Register	00	R/W	69
00B1	CS3_LBR	Chip Select 3 Lower Bound Register	00	R/W	67
00B2	CS3_UBR	Chip Select 3 Upper Bound Register	00	R/W	68
00B3	CS3_CTL	Chip Select 3 Control Register	00	R/W	69
On-Chip RAM Control					
00B4	RAM_CTL	RAM Control Register	80	R/W	192
00B5	RAM_ADDR_U	RAM Address Upper Byte Register	FF	R/W	192
Serial Peripheral Interface (SPI) Block					
00B8	SPI_BRG_L	SPI Baud Rate Generator Register—Low Byte	02	R/W	136
00B9	SPI_BRG_H	SPI Baud Rate Generator Register—High Byte	00	R/W	136
00BA	SPI_CTL	SPI Control Register	04	R/W	137
00BB	SPI_SR	SPI Status Register	00	R	137
00BC	SPI_TSR	SPI Transmit Shift Register	XX	W	139
	SPI_RBR	SPI Receive Buffer Register	XX	R	139
Infrared Encoder/Decoder Block					
00BF	IR_CTL	Infrared Encoder/Decoder Control	00	R/W	129

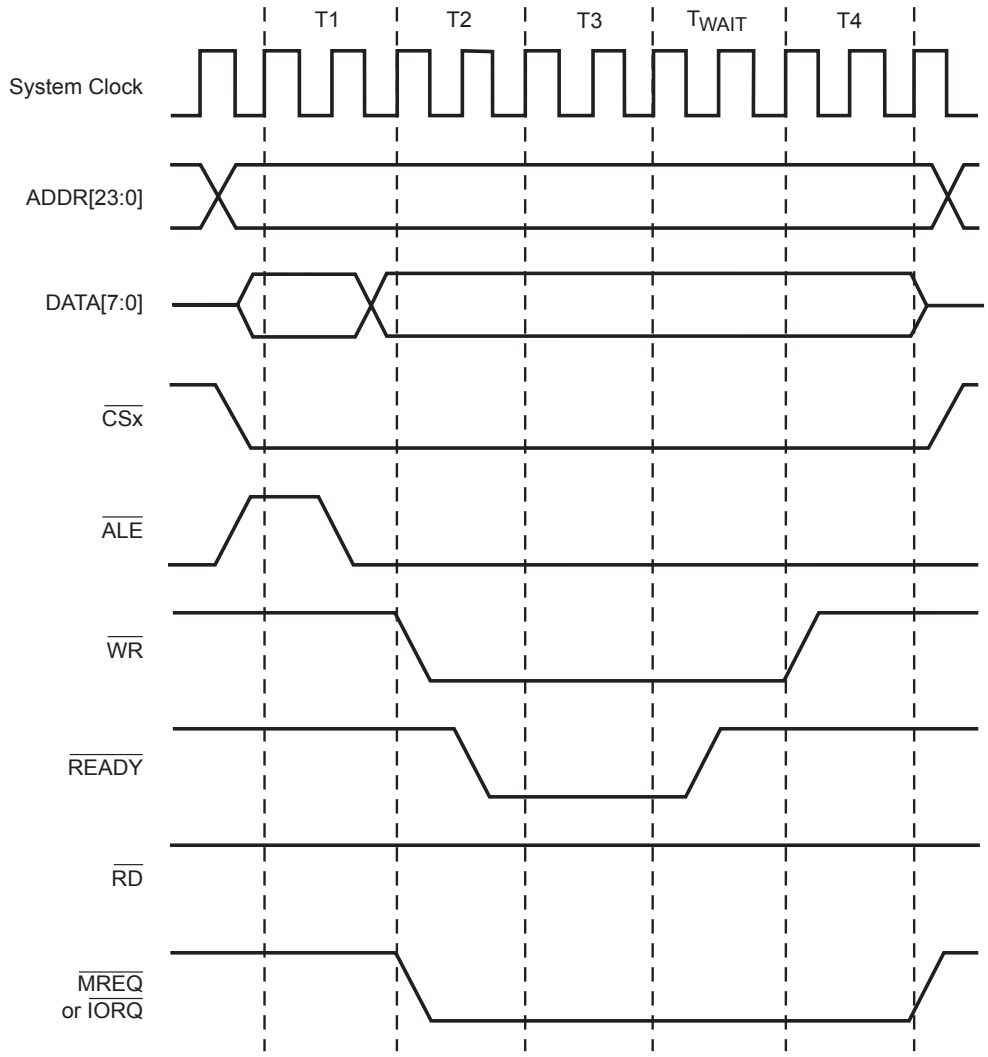


Figure 15. Example: Intel™ Bus Mode Write Timing—Multiplexed Address and Data Bus

Table 34. Timer Data Register—High Byte(TMR0_DR_H = 0082h, TMR1_DR_H = 0085h, TMR2_DR_H = 0088h, TMR3_DR_H = 008Bh, TMR4_DR_H = 008Eh, or TMR5_DR_H = 0091h)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
CPU Access	R	R	R	R	R	R	R	R
Note: R = Read only.								

Bit Position	Value	Description
[7:0] TMRx_DR_H	00h–FFh	These bits represent the High byte of the 2-byte timer data value, {TMRx_DR_H[7:0], TMRx_DR_L[7:0]}. Bit 7 is bit 15 (msb) of the 16-bit timer data value. Bit 0 is bit 8 of the 16-bit timer data value.

Timer Reload Register—Low Byte

The Timer Reload Register—Low Byte, listed in Table 35, stores the least-significant byte (LSB) of the 2-byte timer reload value. In CONTINUOUS mode, the timer reload value is reloaded into the timer upon end-of-count. When RST_EN (TMRx_CTL[1]) is set to 1 to enable the automatic reload and restart function, the timer reload value is written to the timer on the next rising edge of the clock.

Note: *The Timer Data registers and Timer Reload registers share the same address space.*

Table 35. Timer Reload Register—Low Byte(TMR0_RR_L = 0081h, TMR1_RR_L = 0084h, TMR2_RR_L = 0087h, TMR3_RR_L = 008Ah, TMR4_RR_L = 008Dh, or TMR5_RR_L = 0090h)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
CPU Access	W	W	W	W	W	W	W	W
Note: W = Write only.								

Bit Position	Value	Description
[7:0] TMRx_RR_L	00h–FFh	These bits represent the Low byte of the 2-byte timer reload value, {TMRx_RR_H[7:0], TMRx_RR_L[7:0]}. Bit 7 is bit 7 of the 16-bit timer reload value. Bit 0 is bit 0 (lsb) of the 16-bit timer reload value.

Real-Time Clock Hours Register

This register contains the current hours count. See Table 40.

Table 40. Real-Time Clock Hours Register; (RTC_HRS = 00E2h)

Bit	7	6	5	4	3	2	1	0
Reset	X	X	X	X	X	X	X	X
CPU Access	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*
Note: X = Unchanged by RESET; R/W* = Read Only if RTC locked, Read/Write if RTC unlocked.								

Binary-Coded-Decimal Operation (BCD_EN = 1)		
Bit Position	**Value**	**Description**
[7:4] TEN_HRS	0–2	The tens digit of the current hours count.
[3:0] HRS	0–9	The ones digit of the current hours count.

Binary Operation (BCD_EN = 0)		
Bit Position	**Value**	**Description**
[7:0] HRS	00h–17h	The current hours count.

then can discard the byte or take other appropriate action. If the interrupt is caused by a receive-data-ready condition, the application alternately reads the UARTx_LSR and UARTx_RBR registers and removes all of the received data bytes. It reads the UARTx_LSR register before reading the UARTx_RBR register to determine that there is no error in the received data.

To control and check modem status, the application sets up the modem by writing to the UARTx_MCTL register and reading the UARTx_MSR register before starting the process mentioned above.

Poll Mode Transfers. When interrupts are disabled, all data transfers are referred to as poll mode transfers. In poll mode transfers, the application must continually poll the UARTx_LSR register to transmit or receive data without enabling the interrupts. The same is true for the UARTx_MSR register. If the interrupts are not enabled, the data in the UARTx_IIR register cannot be used to determine the cause of an interrupt.

Baud Rate Generator

The Baud Rate Generator consists of a 16-bit downcounter, two registers, and associated decoding logic. The initial value of the Baud Rate Generator is defined by the two BRG Divisor Latch registers, {UARTx_BRG_H, UARTx_BRG_L}. At the rising edge of each system clock, the BRG decrements until it reaches the value 0001h. On the next system clock rising edge, the BRG reloads the initial value from {UARTx_BRG_H, UARTx_BRG_L) and outputs a pulse to indicate the end-of-count. Calculate the UART data rate with the following equation:

$$\text{UART Data Rate (bps)} = \frac{\text{System Clock Frequency}}{\text{16 X (UART Baud Rate Generator Divisor)}}$$

Upon RESET, the 16-bit BRG divisor value resets to 0002h. A minimum BRG divisor value of 0001h is also valid, and effectively bypasses the BRG. A software Write to either the Low- or High-byte registers for the BRG Divisor Latch causes both the Low and High bytes to load into the BRG counter, and causes the count to restart.

The divisor registers can only be accessed if bit 7 of the UART Line Control register (UART*x*_LCTL) is set to 1. After reset, this bit is reset to 0.

UART Interrupt Identification Register

The Read Only UARTx_IIR register allows the user to check whether the FIFO is enabled and the status of interrupts. These registers share the same I/O addresses as the UARTx_FCTL registers. See Table 57 and Table 58.

Table 57. UART Interrupt Identification Registers(UART0_IIR = 00C2h, UART1_IIR = 00D2h)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	1
CPU Access	R	R	R	R	R	R	R	R
Note: R = Read only.								

Bit Position	Value	Description
[7:6] FSTS	00	FIFO is disabled.
	10	Receive FIFO is disabled (MULTIDROP mode).
	11	FIFO is enabled.
[5:4]	00	Reserved.
[3:1] INSTS	000–110	**Interrupt Status Code** The code indicated in these three bits is valid only if INTBIT is 1. If two internal interrupt sources are active and their respective enable bits are High, only the higher priority interrupt is seen by the application. The lower-priority interrupt code is indicated only after the higher-priority interrupt is serviced. Table 58 lists the interrupt status codes.
0 INTBIT	0	There is an active interrupt source within the UART.
	1	There is not an active interrupt source within the UART.

Table 58. UART Interrupt Status Codes

INSTS Value	Priority	Interrupt Type
011	Highest	Receiver Line Status
010	Second	Receiver Data Ready or Trigger Level
110	Third	Character Time-out
101	Fourth	Transmission Complete

Bit Position	Value	Description
3 FE	0	No framing error detected for character at the top of the FIFO. This bit is reset to 0 when the UARTx_LSR register is read.
	1	Framing error detected for the character at the top of the FIFO. This bit is set to 1 when the stop bit following the data/parity bit is logic 0.
2 PE	0	The received character at the top of the FIFO does not contain a parity error. In multidrop mode, this indicates that the received character is a data byte. This bit is reset to 0 when the UARTx_LSR register is read.
	1	The received character at the top of the FIFO contains a parity error. In multidrop mode, this indicates that the received character is an address byte.
1 OE	0	The received character at the top of the FIFO does not contain an overrun error. This bit is reset to 0 when the UARTx_LSR register is read.
	1	Overrun error is detected. If the FIFO is not enabled, this indicates that the data in the receive buffer register was not read before the next character was transferred into the receiver buffer register. If the FIFO is enabled, this indicates the FIFO was already full when an additional character was received by the receiver shift register. The character in the receiver shift register is not put into the receiver FIFO.
0 DR	0	This bit is reset to 0 when the UARTx_RBR register is read or all bytes are read from the receiver FIFO.
	1	**Data Ready** If the FIFO is not enabled, this bit is set to 1 when a complete incoming character is transferred into the receiver buffer register from the receiver shift register. If the FIFO is enabled, this bit is set to 1 when a character is received and transferred to the receiver FIFO.

UART Modem Status Register

This register is used to show the status of the UART signals. See Table 65 on page 122.

UART Scratch Pad Register

The UARTx_SPR register can be used by the system as a general-purpose Read/Write register. See Table 66.

Table 66. UART Scratch Pad Registers(UART0_SPR = 00C7h, UART1_SPR = 00D7h)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
CPU Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Note: R/W = Read/Write.								

Bit Position	Value	Description
[7:0] SPR	00h–FFh	The UART scratch pad register is available for use as a general-purpose Read/Write register.

Table 67. IrDA Physical Layer 1.4 Pulse Durations Specifications (Continued)

Baud Rate	Minimum Pulse Width	Maximum Pulse Width
57600	1.41 s	4.34 s
115200	1.41 s	2.23 s

Receiver Frequency Divider

The IrDA receiver uses a 6-bit frequency divider. The value is derived from the system clock to measure IR_RxD pulses. The IrDA endec detects pulses that are within the IrDA Physical Layer specified minimum and maximum ranges, with system clock frequencies from 5 MHz up to 50 MHz.

The upper four bits of the frequency divider factor are set via the FREQ_DIV bit in the IR_CTL register, based on the following equation:

$$\text{Frequency Divider Factor} = \frac{\text{System Clock Frequency (MHz)}}{\text{Target Frequency of 3.33 MHz}}$$

The remaining lower two bits of the divider are set to 03h. The target frequency corresponds to a period of 1.2 seconds. The FREQ_DIV value must be rounded to the nearest integer and the resulting period of the 6-bit frequency divider must not be larger than 1.4 seconds, which is the IrDA defined minimum pulse width. If the period is greater than 1.4 seconds, FREQ_DIV should be rounded to the next lower integer. The receiver frequency divider value versus the system clock frequency is shown in table, below.

Table 68. Frequency Divider Values

System Clock	FREQ_DIV
< 5.0 MHz	00h*
5.0–7.8 MHz	01h
7.8–10.8 MHz	02h
10.8–13.6 MHz	03h
13.6–25 MHz	FLOOR[4-bit Frequency Divider Factor]
25–50 MHz	ROUND[4-bit Frequency Divider Factor]

Note: *The frequency divider is disabled when set to 00h.

can be repeated. Repeated Read or Write operations can occur without requiring a resend of the ZDI command. To initiate a new ZDI command, a START signal must follow. Figure 41 displays the timing for address Writes to ZDI registers.

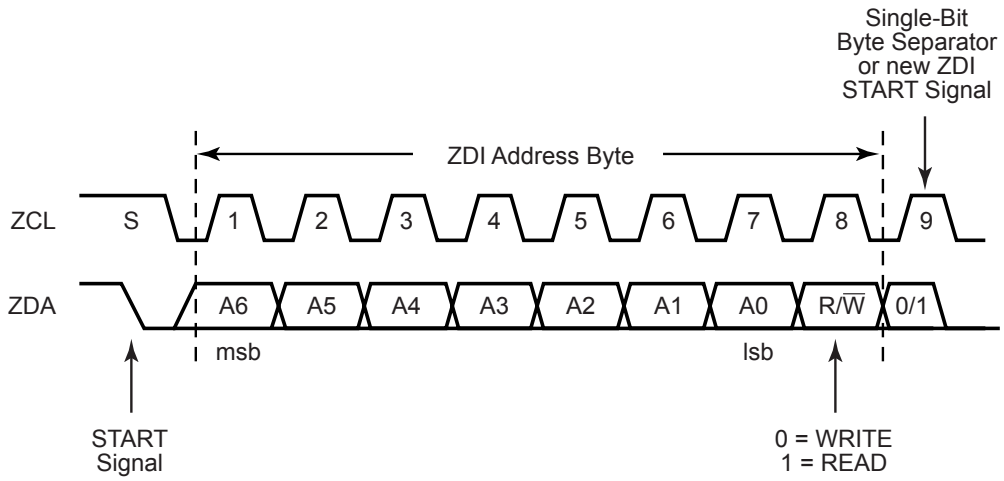


Figure 41.ZDI Address Write Timing

ZDI Write Operations

ZDI Single-Byte Write

For single-byte Write operations, the address and Write control bit are first written to the ZDI block. Following the single-bit byte separator, the data is shifted into the ZDI block on the next eight rising edges of ZCL. The master terminates activity after 8 clock cycles.Figure 42 displays the timing for ZDI single-byte Write operations.

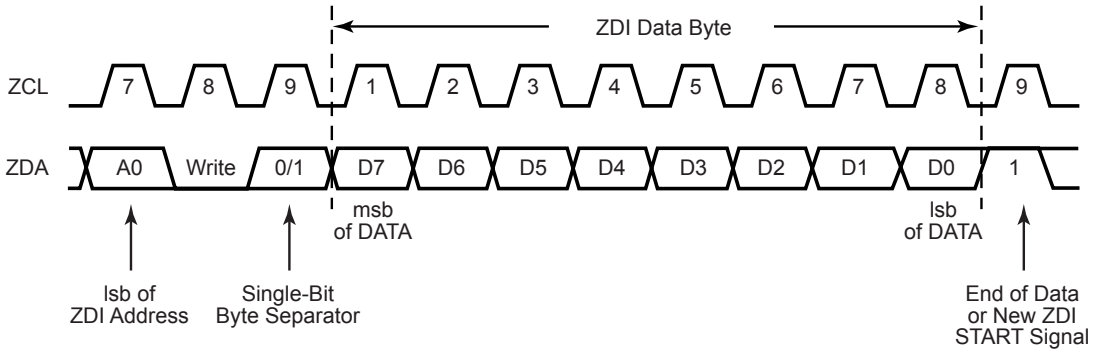


Figure 42.ZDI Single-Byte Data Write Timing

be accessed via the clock (TCK) and data (TDI) pins. See the Zilog Debug Interface section on page 162 for more information about ZDI.

OCI Interface

There are five dedicated pins on the eZ80F92 device for the OCI interface. Four pins—TCK, TMS, TDI, and TDO—are required for IEEE Standard 1149.1-compliant JTAG ports. The TRIGOUT pin provides additional testability features. These five OCI pins are listed in Table 110.

Table 110. OCI Pins

Symbol	Name	Type	Description
TCK	Clock	Input	Asynchronous to the primary CPU system clock. The TCK period must be at least twice the system clock period. During RESET, this pin is sampled to select either OCI or ZDI DEBUG modes. If Low during RESET, the OCI is enabled. If High during RESET, the OCI is powered down and ZDI DEBUG mode is enabled. When ZDI DEBUG mode is active, this pin is the ZDI clock. On-chip pull-up ensures a default value of 1 (High).
TMS	Test Mode Select	Input	This serial test mode input controls JTAG mode selection. On-chip pull-up ensures a default value of 1 (High). The TMS signal is sampled on the rising edge of the TCK signal.
TDI	Data In	Input (OCI enabled)	Serial test data input. On-chip pull-up ensures a default value of 1 (High). This pin is input-only when the OCI is enabled. The input data is sampled on the rising edge of the TCK signal.
		I/O (OCI disabled)	When the OCI is disabled, this pin functions as the ZDA (ZDI Data) I/O pin.
TDO	Data Out	Output	The output data changes on the falling edge of the TCK signal.
TRIGOUT	Trigger Output	Output	Generates an active High trigger pulse when valid OCI trigger events occur. Output is tristate when no data is driven out.

Table 120. Flash Interrupt Control Register; (FLASH_IRQ=00FBh)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
CPU Access	R/W	R/W	R	R	R	R	R	R
Note: R/W = Read/Write, R = Read Only. Read resets bits [5] and [3:0].								

Bit Position	Value	Description
[7] DONE_IEN	0	Flash Erase/Row Program Done Interrupt is disabled
	1	Flash Erase/Row Program Done Interrupt is enabled
[6] ERR_IEN	0	Error Condition Interrupt is disabled
	1	Error Condition Interrupt is enabled
[5] DONE	0	Erase/Row Program Done Flag is not set
	1	Erase/Row Program Done Flag is set
[4]	0	Reserved
[3] WR_VIO	0	The Write Violation Error Flag is not set
	1	The Write Violation Error Flag is set
[2] RP_TMO	0	The Row Program Time-out Error Flag is not set
	1	The Row Program Time-out Error Flag is set
[1] PG_VIO	0	The Page Erase Violation Error Flag is not set
	1	The Page Erase Violation Error Flag is set
[0] MASS_VIO	0	The Mass Erase Violation Error Flag is not set
	1	The Mass Erase Violation Error Flag is set

Flash Page Select Register

The msb of this register is used to select whether all Flash access and Page Erases are directed to the 256-byte Information Page or to the main Flash memory array. When the main array is selected, the lower 7-bits (6 bits in the eZ80F93 device) are used to select one of the 128 pages for Page Erase or I/O Write operations.

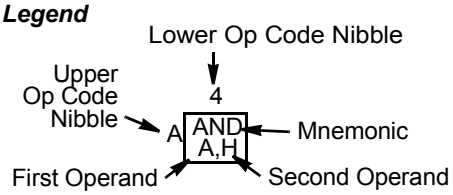
To perform a Page Erase, the software must set the proper page value prior to setting the Page Erase bit in the Flash control register.

Op-Code Map

Table 135 through Table 141 on page 219 list the hex values for each of the eZ80® CPU instructions.

Table 135. Op Code Map—First Op Code

Legend



Upper Nibble (Hex) \ Lower Nibble (Hex)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	LD BC, Mmn	LD (BC),A	INC BC	INC B	DEC B	LD B,n	RLCA	EX AF,AF'	ADD HL,BC	LD A,(BC)	DEC BC	INC C	DEC C	LD C,n	RRCA
1	DJNZ d	LD DE, Mmn	LD (DE),A	INC DE	INC D	DEC D	LD D,n	RLA	JR d	ADD HL,DE	LD A,(DE)	DEC DE	INC E	DEC E	LD E,n	RRA
2	JR NZ,d	LD HL, Mmn	LD (Mmn), HL	INC HL	INC H	DEC H	LD H,n	DAA	JR Z,d	ADD HL,HL	LD HL, (Mmn)	DEC HL	INC L	DEC L	LD L,n	CPL
3	JR NC,d	LD SP, Mmn	LD (Mmn), A	INC SP	INC (HL)	DEC (HL)	LD (HL),n	SCF	JR CF,d	ADD HL,SP	LD A, (Mmn)	DEC SP	INC A	DEC A	LD A,n	CCF
4	.SIS suffix	LD B,C	LD B,D	LD B,E	LD B,H	LD B,L	LD B,(HL)	LD B,A	LD C,B	.LIS suffix	LD C,D	LD C,E	LD C,H	LD C,L	LD C,(HL)	LD C,A
5	LD D,B	LD D,C	.SIL suffix	LD D,E	LD D,H	LD D,L	LD D,(HL)	LD D,A	LD E,B	LD E,C	LD E,D	.LIL suffix	LD E,H	LD E,L	LD E,(HL)	LD E,A
6	LD H,B	LD H,C	LD H,D	LD H,E	LD H,H	LD H,L	LD H,(HL)	LD H,A	LD L,B	LD L,C	LD L,D	LD L,E	LD L,H	LD L,L	LD L,(HL)	LD L,A
7	LD (HL),B	LD (HL),C	LD (HL),D	LD (HL),E	LD (HL),H	LD (HL),L	HALT	LD (HL),A	LD A,B	LD A,C	LD A,D	LD A,E	LD A,H	LD A,L	LD A,(HL)	LD A,A
8	ADD A,B	ADD A,C	ADD A,D	ADD A,E	ADD A,H	ADD A,L	ADD A,(HL)	ADD A,A	ADC A,B	ADC A,C	ADC A,D	ADC A,E	ADC A,H	ADC A,L	ADC A,(HL)	ADC A,A
9	SUB A,B	SUB A,C	SUB A,D	SUB A,E	SUB A,H	SUB A,L	SUB A,(HL)	SUB A,A	SBC A,B	SBC A,C	SBC A,D	SBC A,E	SBC A,H	SBC A,L	SBC A,(HL)	SBC A,A
A	AND A,B	AND A,C	AND A,D	AND A,E	AND A,H	AND A,L	AND A,(HL)	AND A,A	XOR A,B	XOR A,C	XOR A,D	XOR A,E	XOR A,H	XOR A,L	XOR A,(HL)	XOR A,A
B	OR A,B	OR A,C	OR A,D	OR A,E	OR A,H	OR A,L	OR A,(HL)	OR A,A	CP A,B	CP A,C	CP A,D	CP A,E	CP A,H	CP A,L	CP A,(HL)	CP A,A
C	RET NZ	POP BC	JP NZ, Mmn	JP Mmn	CALL NZ, Mmn	PUSH BC	ADD A,n	RST 00h	RET Z	RET	JP Z, Mmn	Table 136	CALL Z, Mmn	CALL Mmn	ADC A,n	RST 08h
D	RET NC	POP DE	JP NC, Mmn	OUT (n),A	CALL NC, Mmn	PUSH DE	SUB A,n	RST 10h	RET CF	EXX	JP CF, Mmn	IN A,(n)	CALL CF, Mmn	Table 137	SBC A,n	RST 18h
E	RET PO	POP HL	JP PO, Mmn	EX (SP),HL	CALL PO, Mmn	PUSH HL	AND A,n	RST 20h	RET PE	JP (HL)	JP PE, Mmn	EX DE,HL	CALL PE, Mmn	Table 138	XOR A,n	RST 28h
F	RET P	POP AF	JP P, Mmn	DI	CALL P, Mmn	PUSH AF	OR A,n	RST 30h	RET M	LD SP,HL	JP M, Mmn	EI	CALL M, Mmn	Table 139	CP A,n	RST 38h

Notes: n = 8-bit data; Mmn = 16- or 24-bit addr or data; d = 8-bit two's-complement displacement.

Table 148. External Read Timing

Parameter	Abbreviation	Delay (ns)	
		Min	Max
T_1	Clock Rise to ADDR Valid Delay	—	13
T_2	Clock Rise to ADDR Hold Time	2.0	—
T_3	Input DATA Valid to Clock Rise Setup Time	1.0	—
T_4	Clock Rise to DATA Hold Time	2.0	—
T_5	Clock Rise to $\overline{CSx}$ Assertion Delay	2.0	19.0
T_6	Clock Rise to $\overline{CSx}$ Deassertion Delay	2.0	18.0
T_7	Clock Rise to $\overline{MREQ}$ Assertion Delay	2.0	16.0
T_8	Clock Rise to $\overline{MREQ}$ Deassertion Delay	2.0	16.0
T_9	Clock Rise to $\overline{RD}$ Assertion Delay	2.0	16.0
T_{10}	Clock Rise to $\overline{RD}$ Deassertion Delay	2.0	16.0

External Memory Write Timing

Figure 59 and Table 149 on page 232 display the timing for external writes.

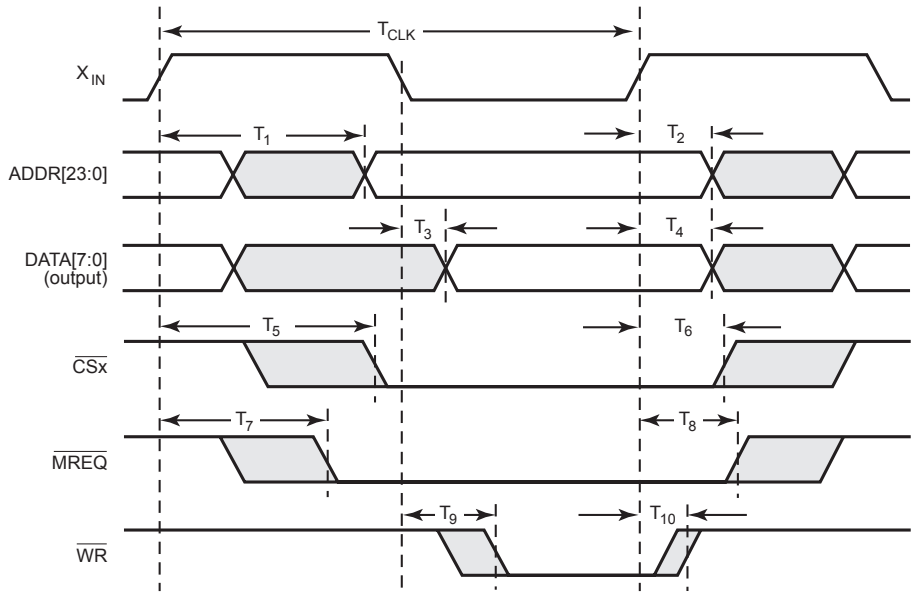


Figure 59.External Memory Write Timing

Table 151. External I/O Write Timing (Continued)

		Delay (ns)	
Parameter	**Abbreviation**	**Min**	**Max**
T_{10}	Clock Rise to $\overline{WR}$ Deassertion Delay*	1.6	6.5
	$\overline{WR}$ Deassertion to ADDR Hold Time	0.25	—
	$\overline{WR}$ Deassertion to DATA Hold Time	0.25	—
	$\overline{WR}$ Deassertion to $\overline{CSx}$ Hold Time	0.25	—
	$\overline{WR}$ Deassertion to $\overline{IORQ}$ Hold Time	0.25	—

Note: *At the conclusion of a Write cycle, deassertion of $\overline{WR}$ always occurs before any change to ADDR, DATA, $\overline{CSx}$, or $\overline{IORQ}$.

Wait State Timing for Read Operations

Figure 62 displays the extension of the memory access signals using a single WAIT state for a Read operation. This WAIT state is generated by setting CS_WAIT to 001h in the Chip Select Control Register.

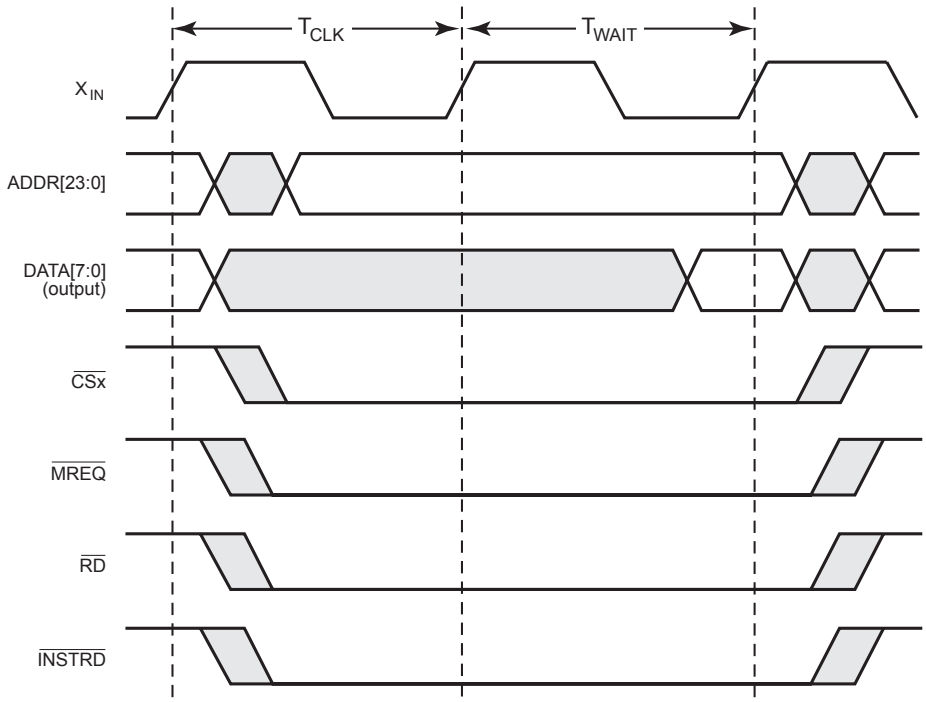


Figure 62.Wait State Timing for Read Operations